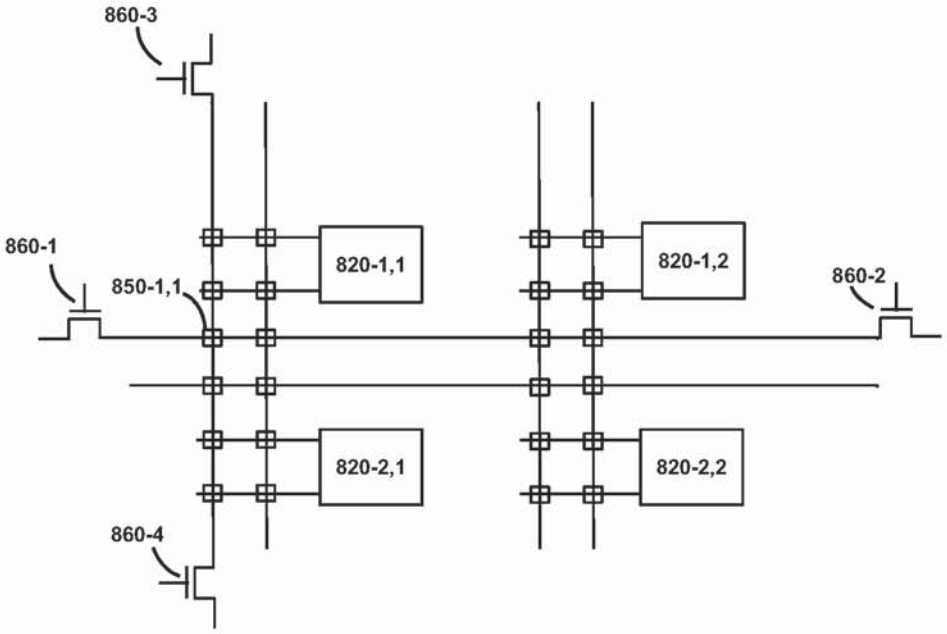


Prior Art

Fig. 1

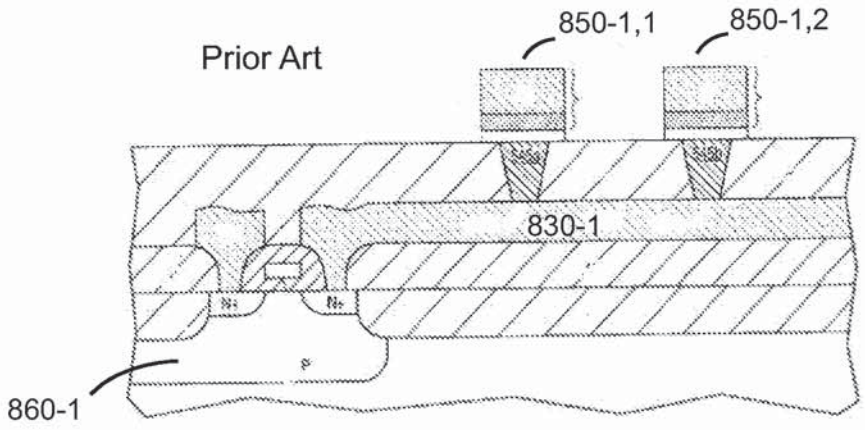


Fig 2 - prior art

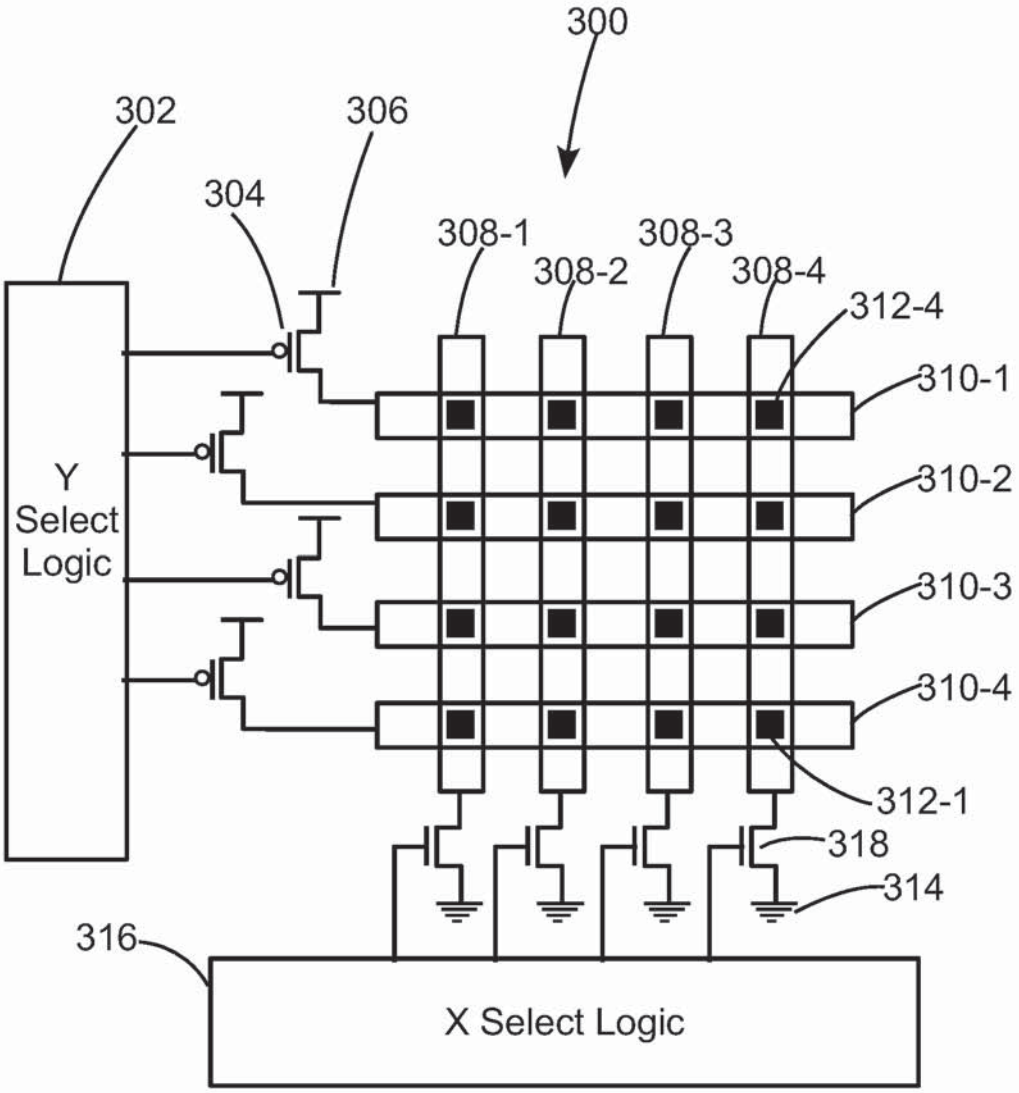

300
302
306
304
308-1
308-3
308-2
308-4
312-4
310-1
310-2
310-3
310-4
312-1
318
314
316
Y
Select
Logic
X Select Logic

Fig. 3A

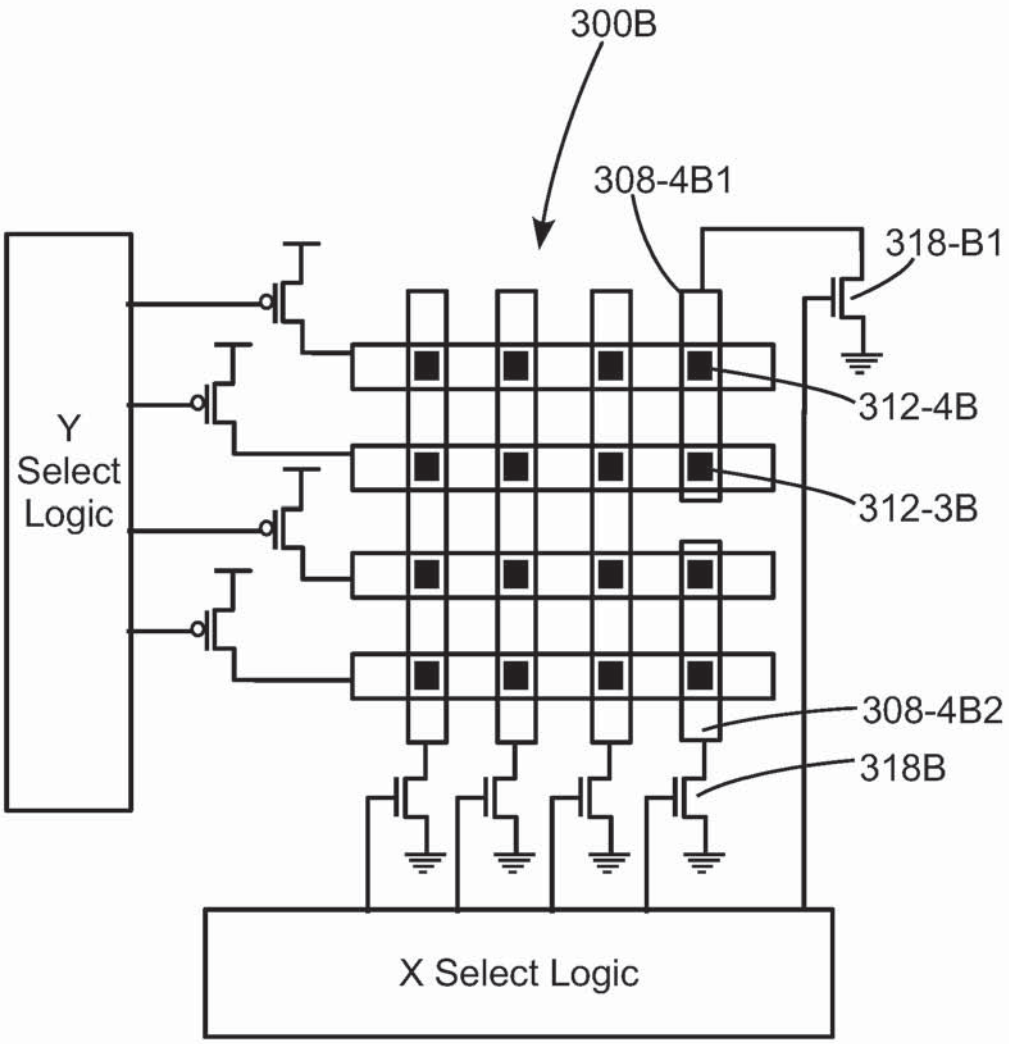

300B
308-4B1
318-B1
312-4B
312-3B
308-4B2
318B
Y
Select
Logic
X Select Logic

Fig. 3B

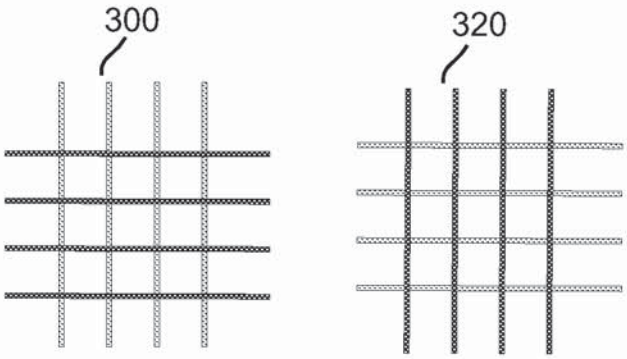


Fig 4A

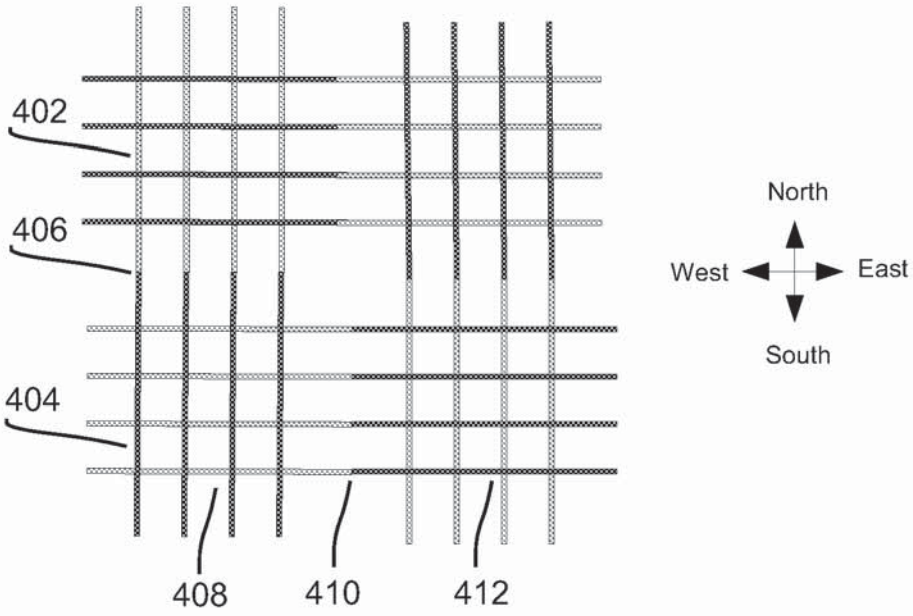


Fig 4B

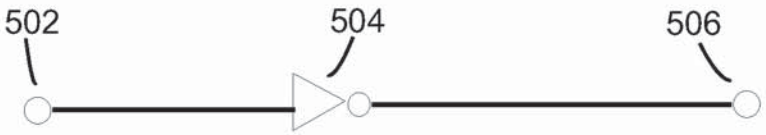


FIG 5A

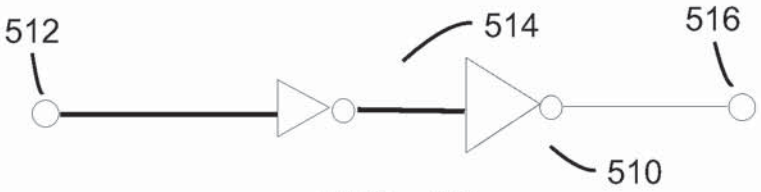


FIG 5B

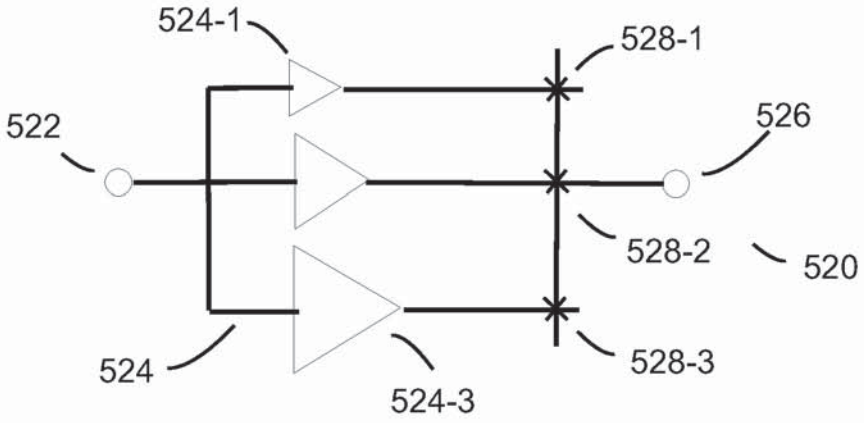


FIG 5C

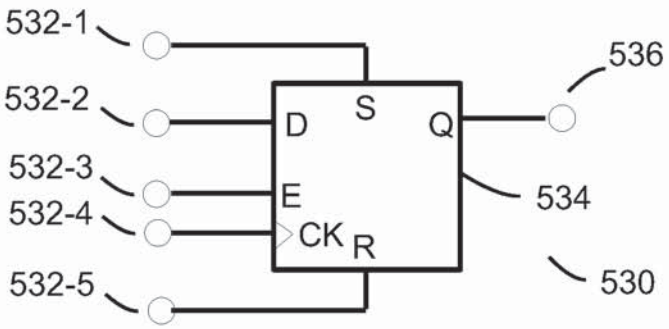


FIG 5D

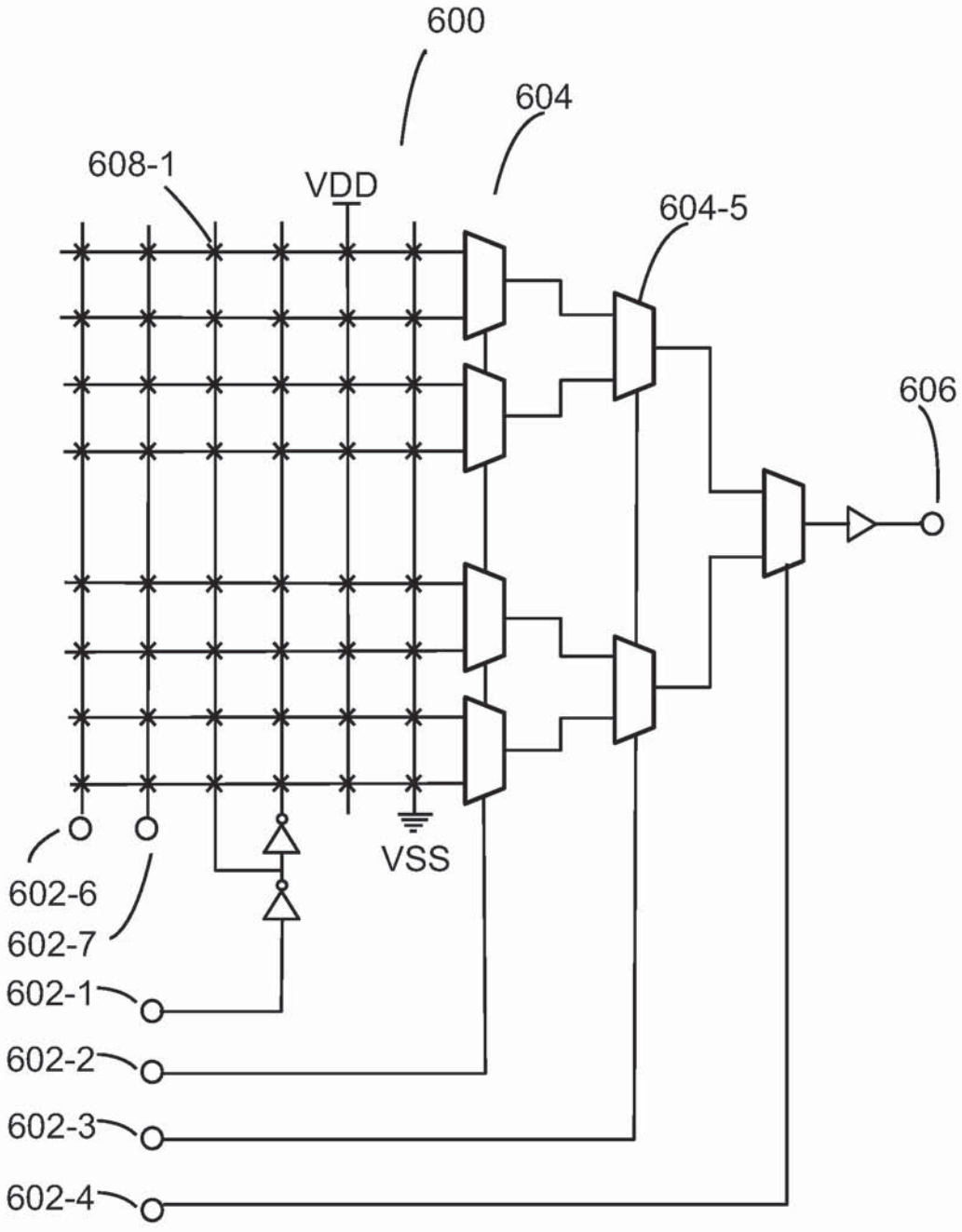


Fig. 6

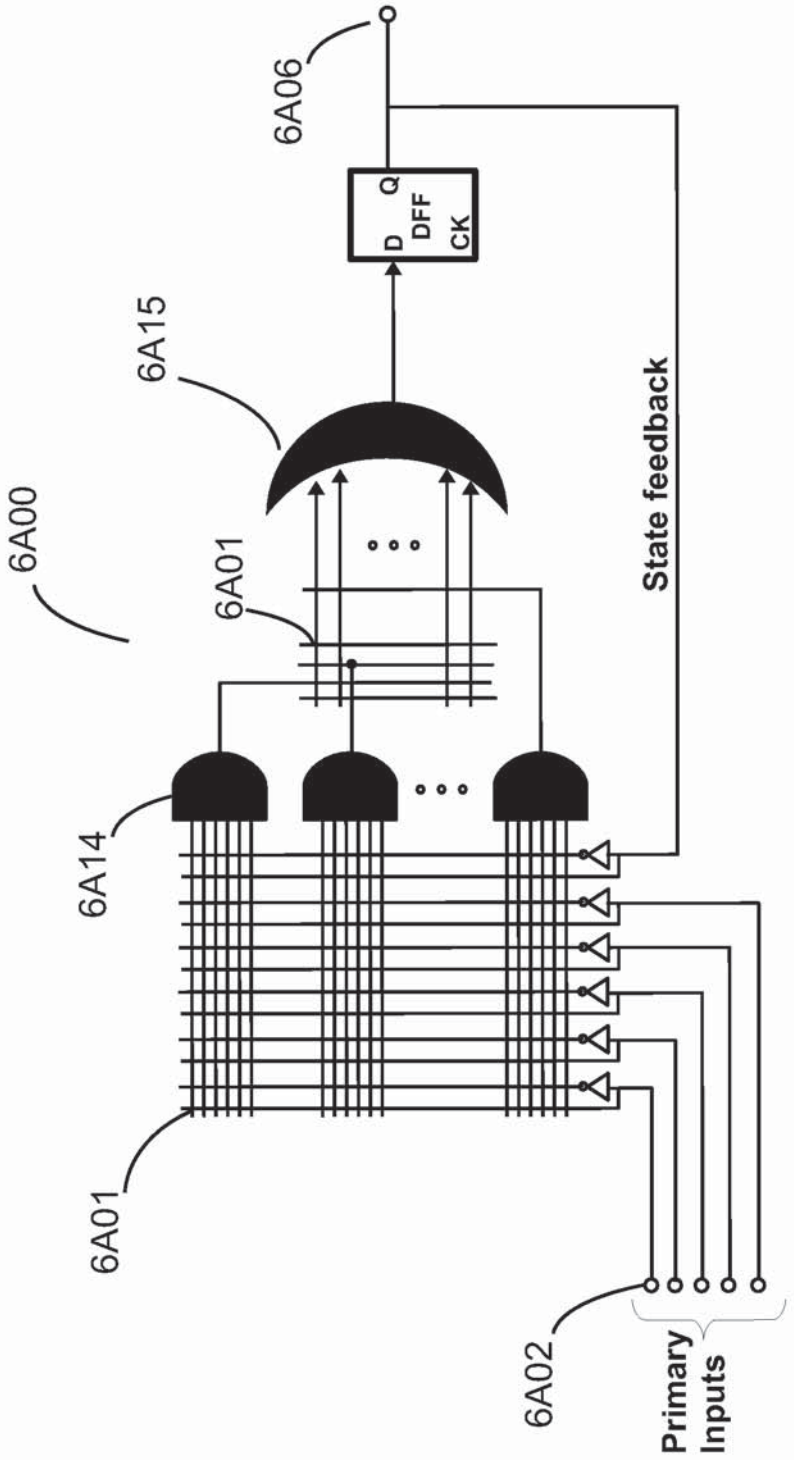

6A06
Q
D
DFF
CK
6A15
6A00
6A01
State feedback
6A14
6A01
6A02
Primary
Inputs

Fig. 6A

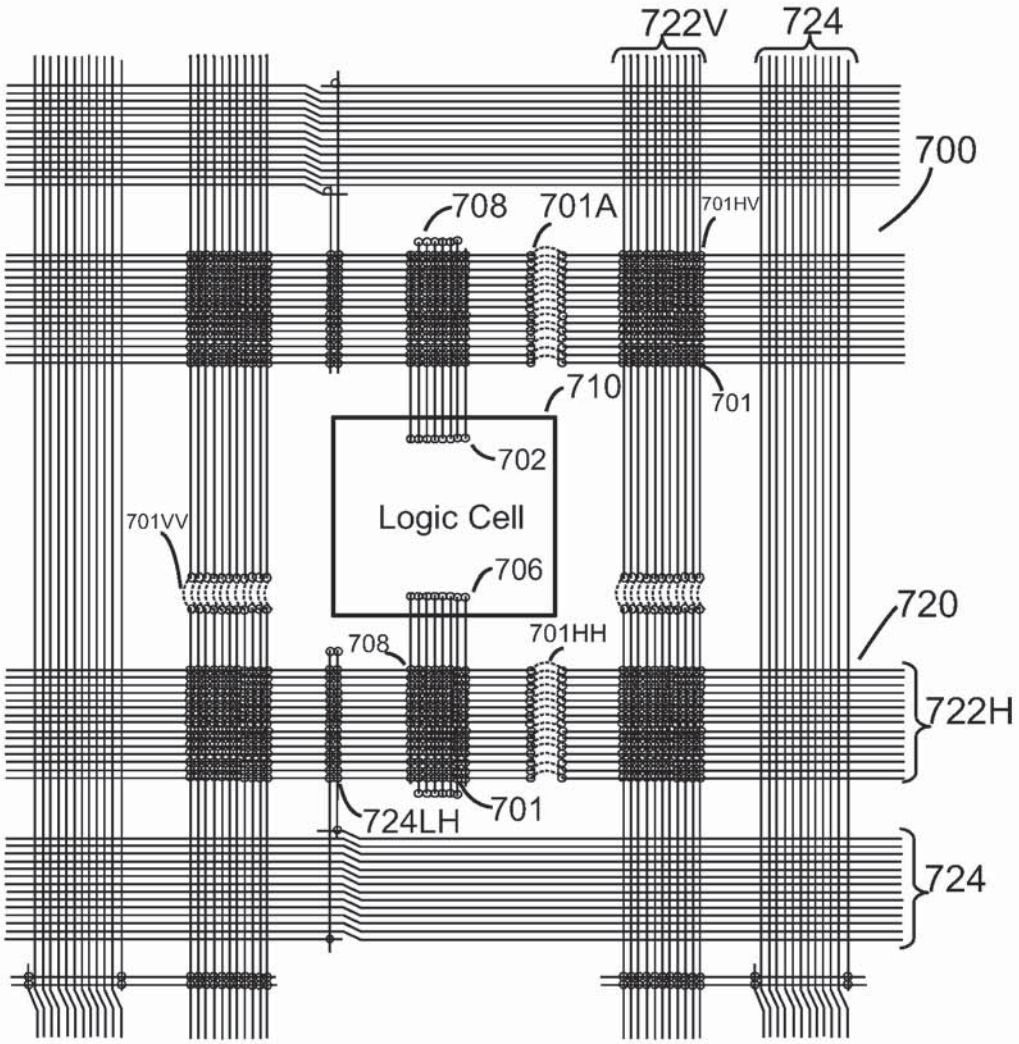

722V
724
700
708
701A
701HV
710
701
702
Logic Cell
701VV
706
720
701HH
708
722H
724LH
701
724

Fig. 7

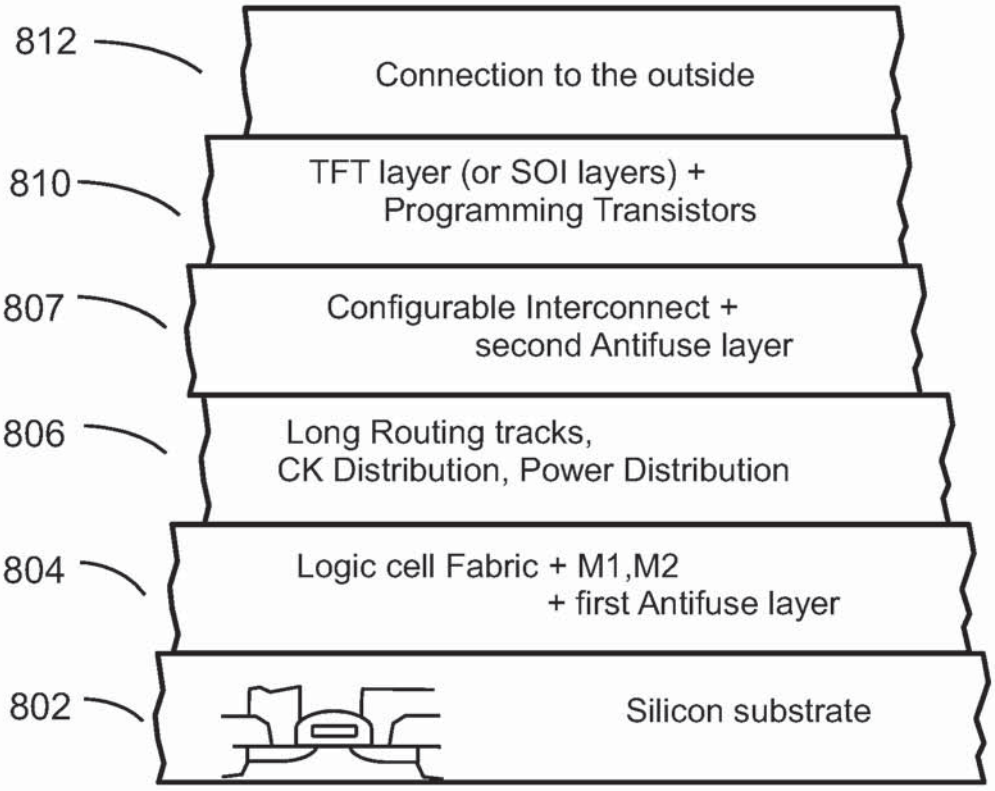

812
Connection to the outside
810
TFT layer (or SOI layers) +
Programming Transistors
807
Configurable Interconnect +
second Antifuse layer
806
Long Routing tracks,
CK Distribution, Power Distribution
804
Logic cell Fabric + M1,M2
+ first Antifuse layer
802
Silicon substrate

Fig. 8

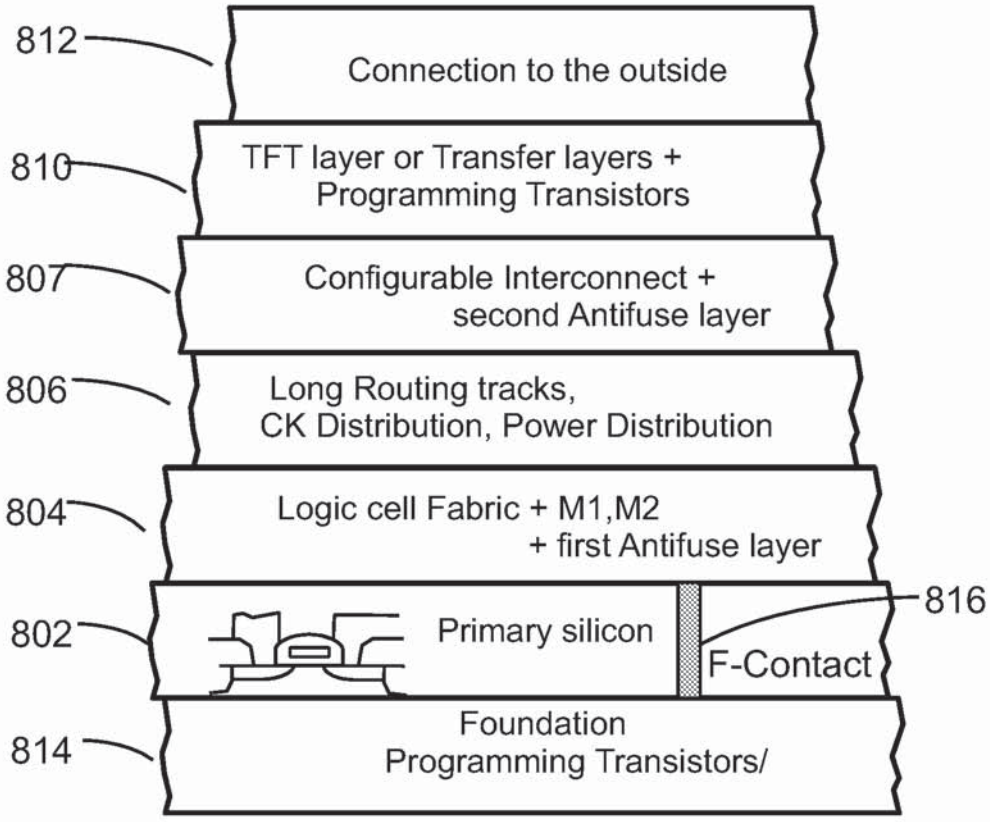

812
Connection to the outside
810
TFT layer or Transfer layers +
Programming Transistors
807
Configurable Interconnect +
second Antifuse layer
806
Long Routing tracks,
CK Distribution, Power Distribution
804
Logic cell Fabric + M1,M2
+ first Antifuse layer
802
Primary silicon
816
F-Contact
814
Foundation
Programming Transistors/

Fig. 8A



Fig. 8B

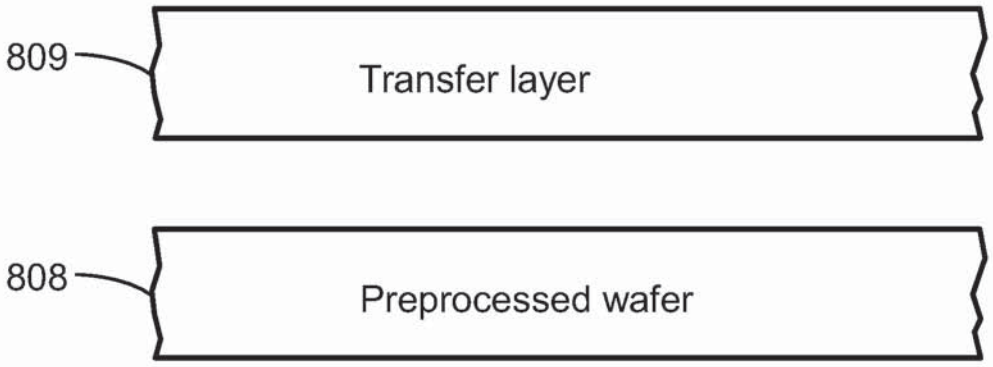


Fig. 8C

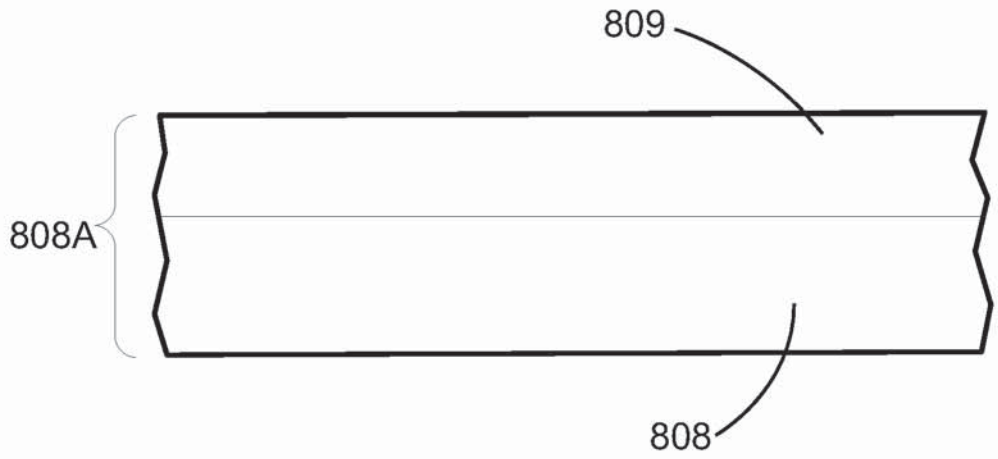


Fig. 8D

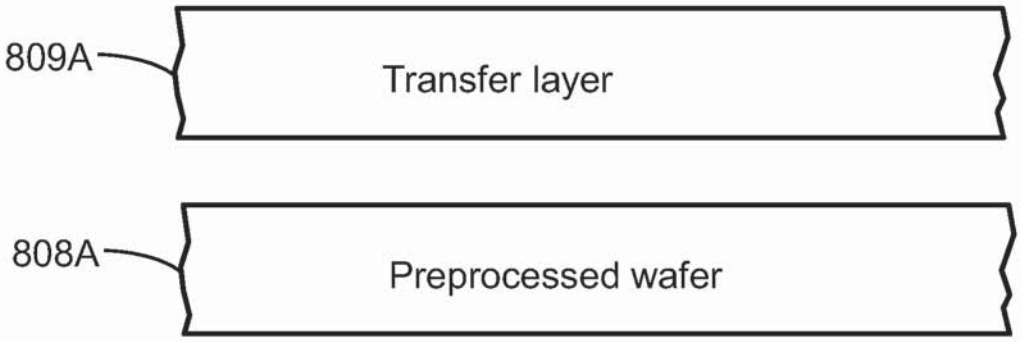


Fig. 8E

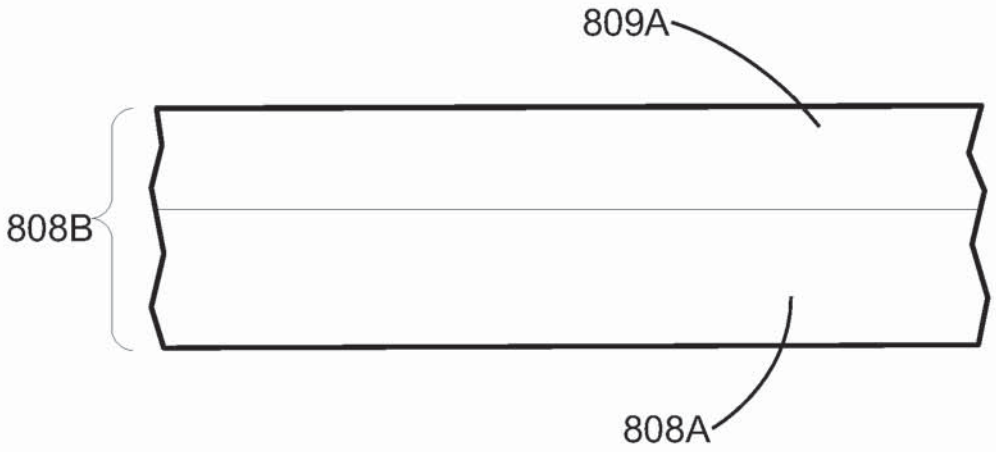


Fig. 8F

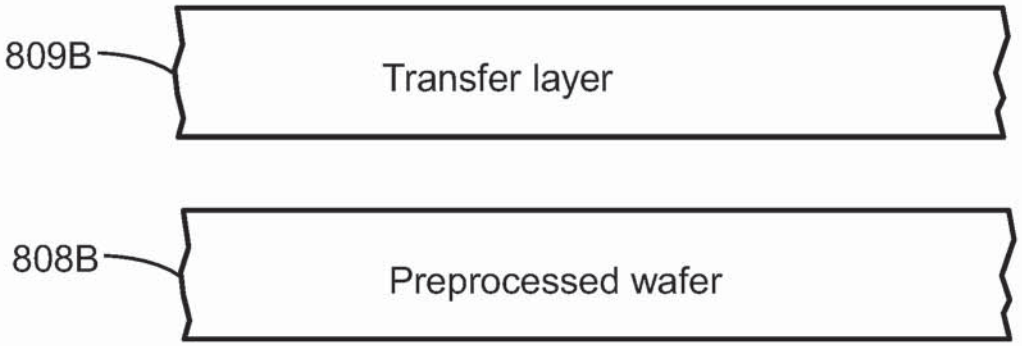


Fig. 8G



Fig. 8H

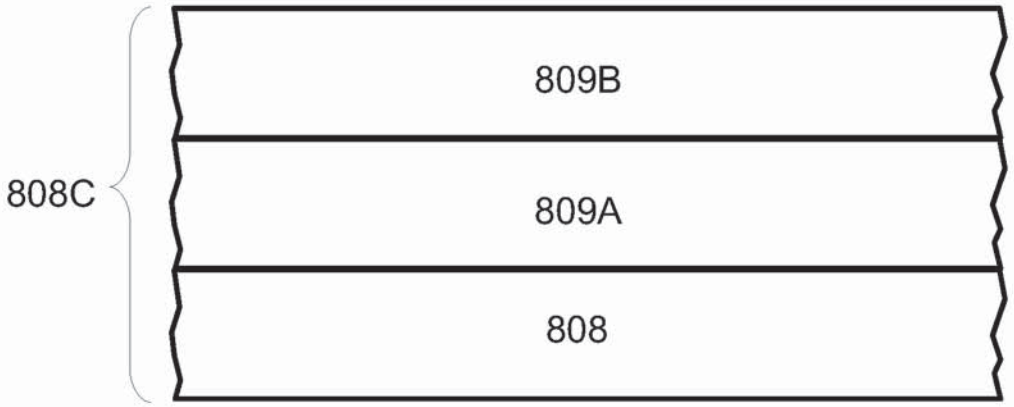


Fig. 8I

Fig. 9A
Prior Art

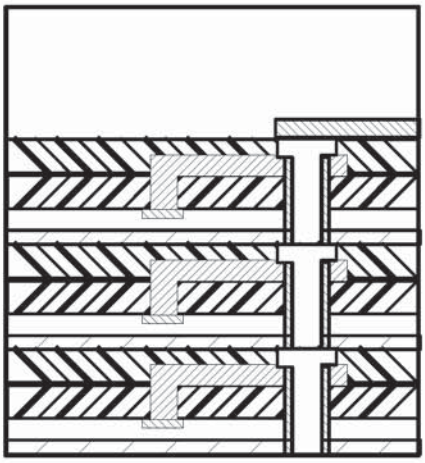


Fig. 9B
Prior Art

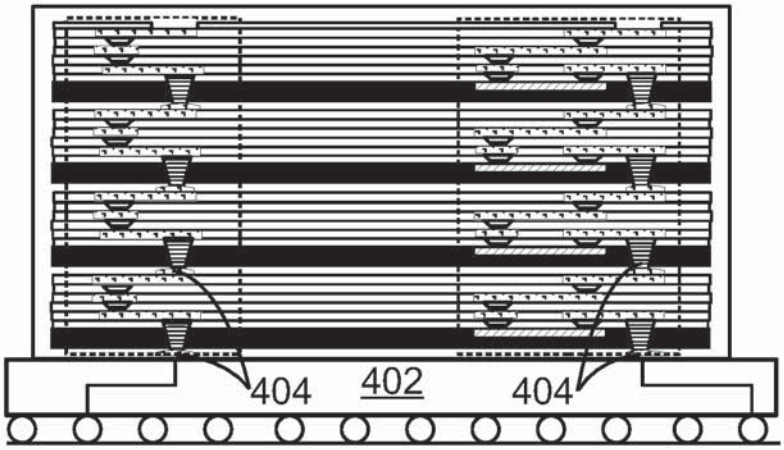
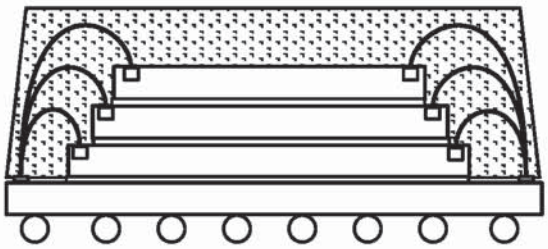


Fig. 9C
Prior Art



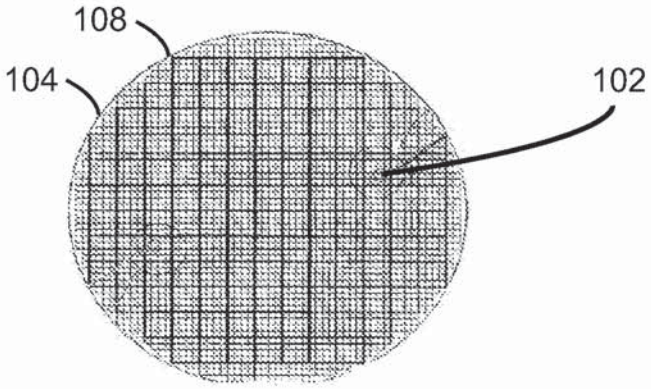


Fig 10A Prior Art

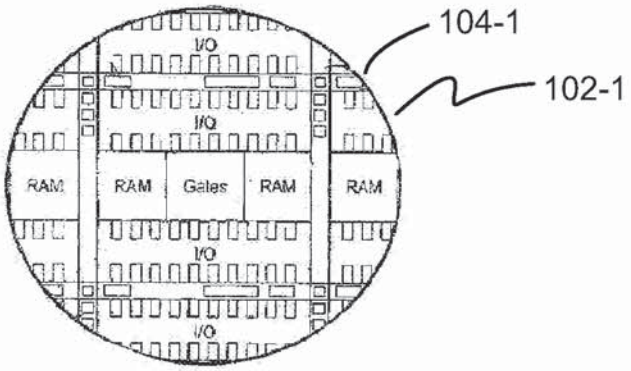


Fig 10B Prior Art

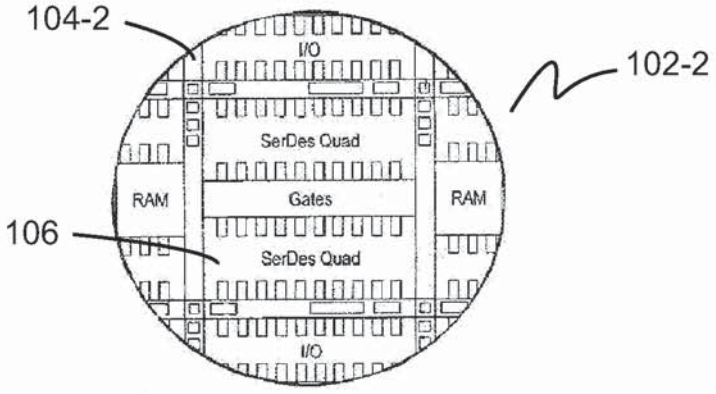


Fig 10C Prior Art

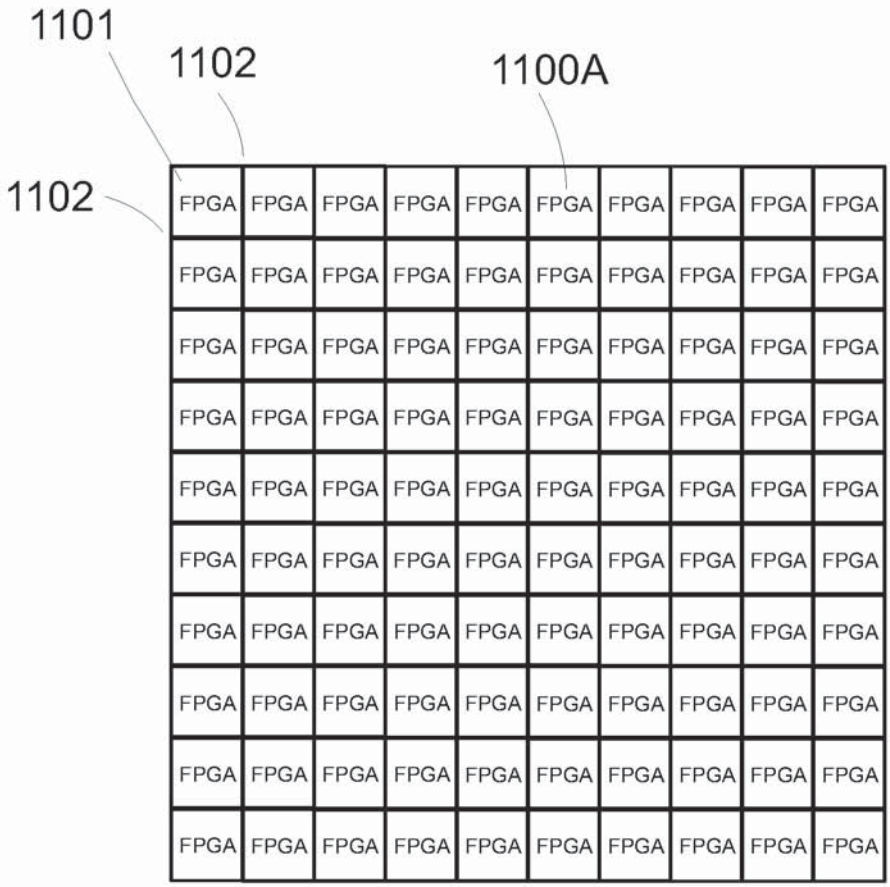


Fig 11A

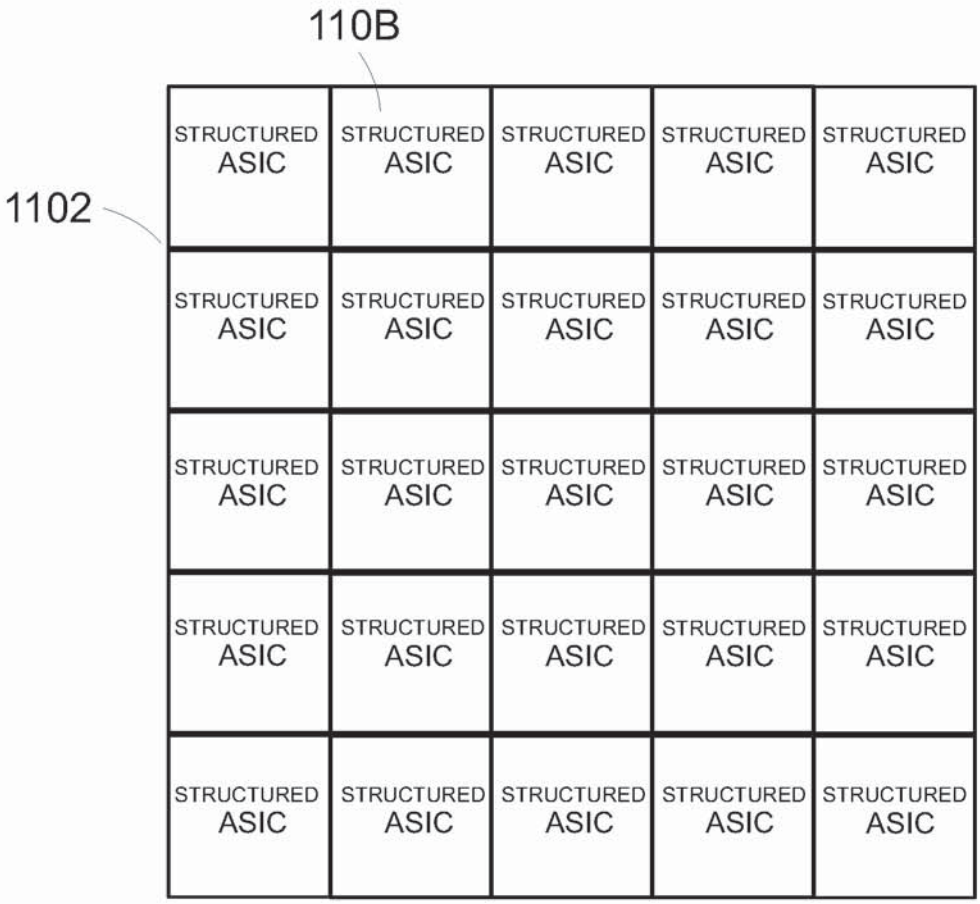


Fig 11B

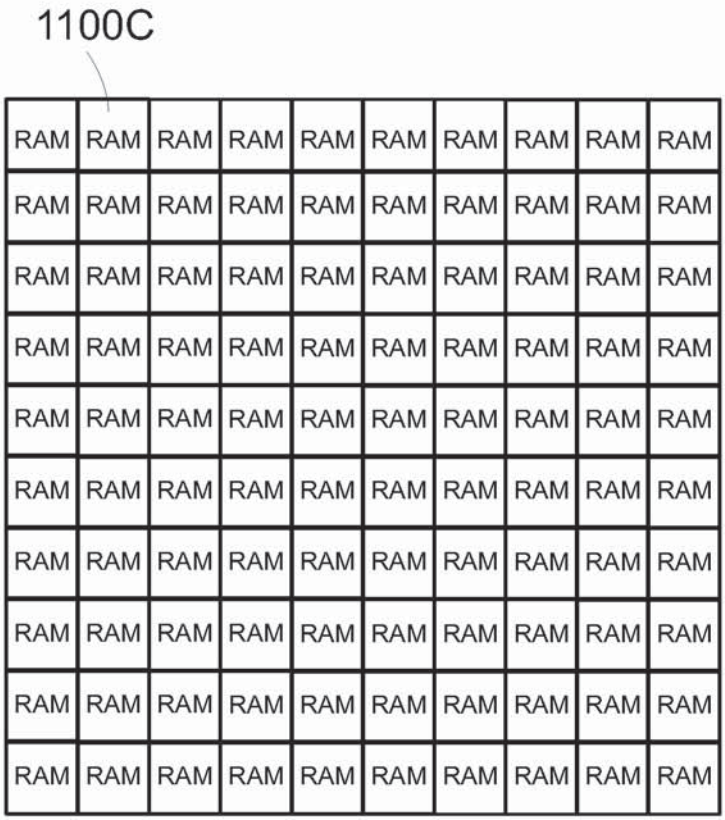


Fig 11C

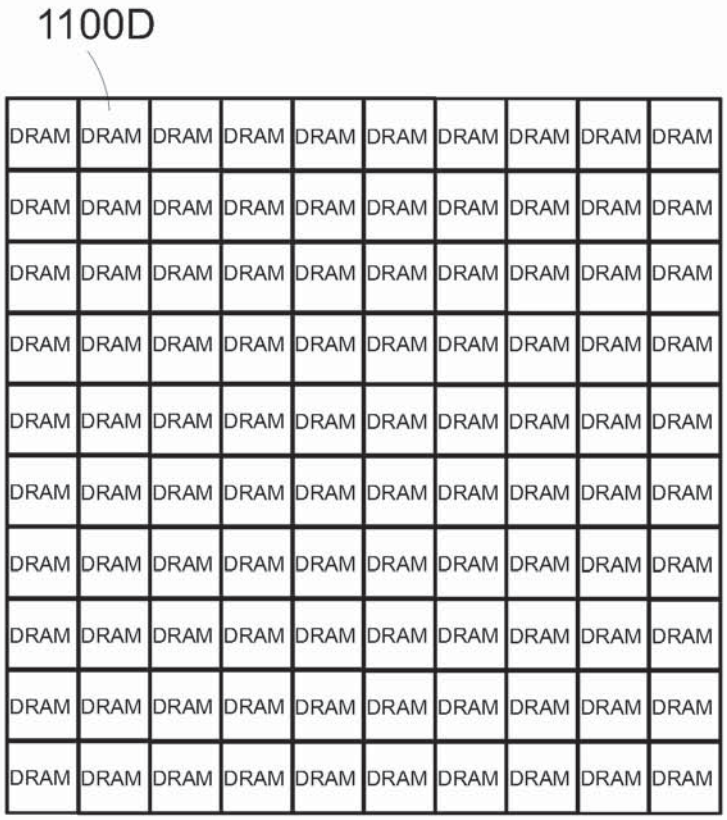


Fig 11D

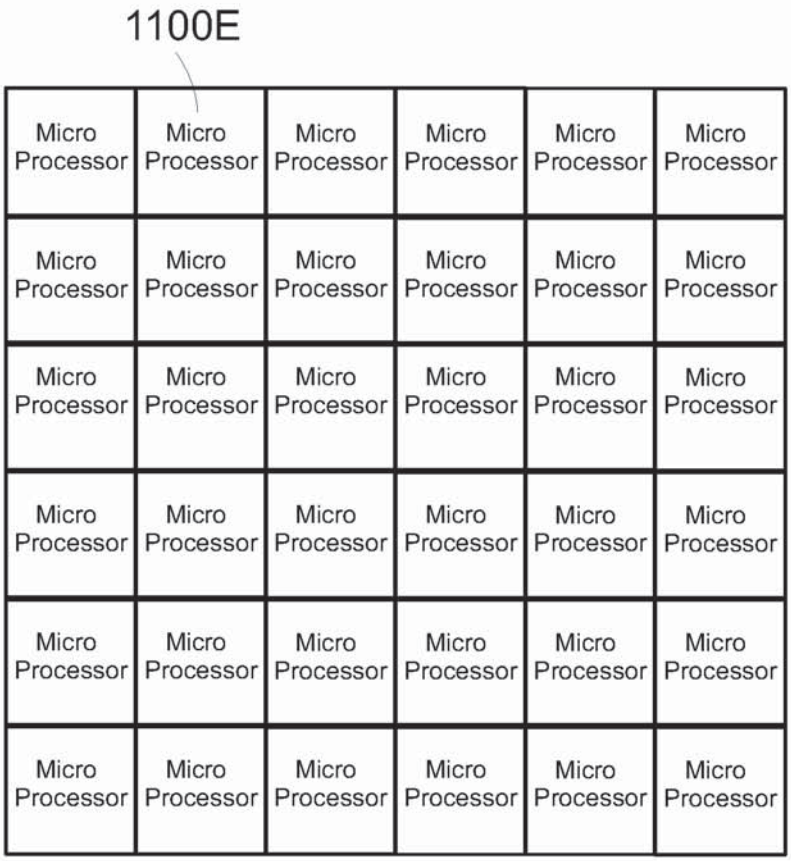


Fig 11E

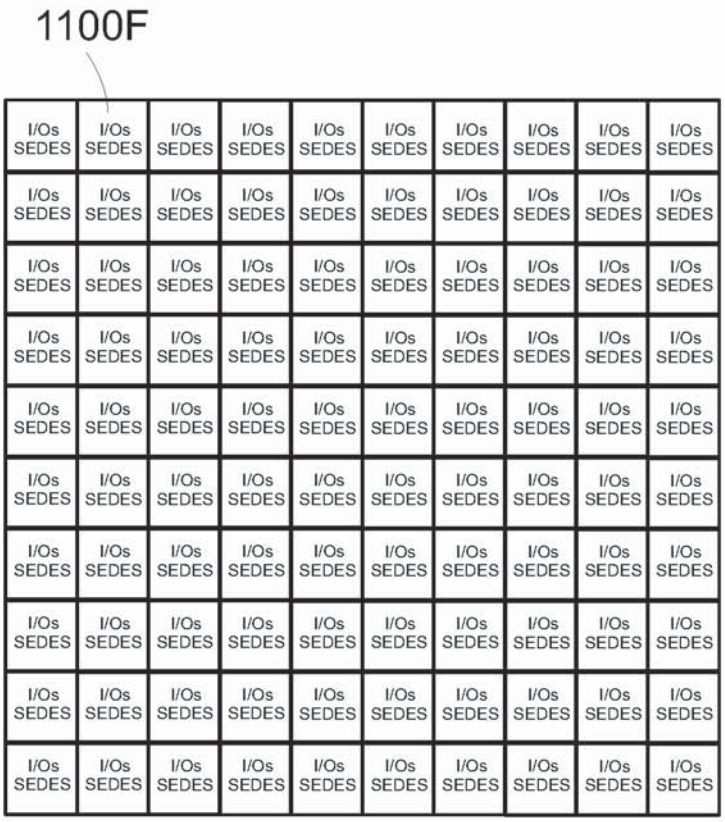


Fig 11F

Fig 12A

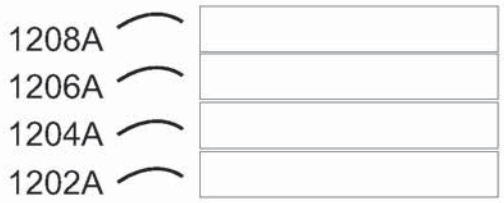


Fig 12B

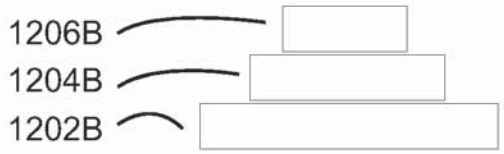


Fig 12C

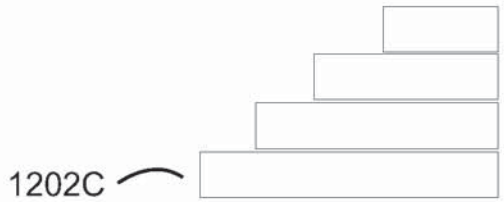


Fig 12D

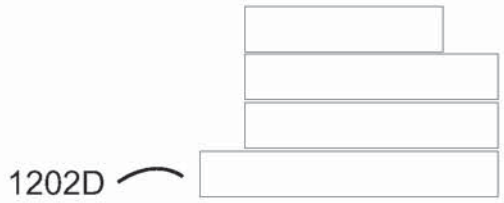
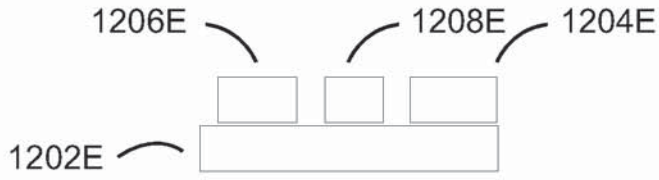


Fig 12E



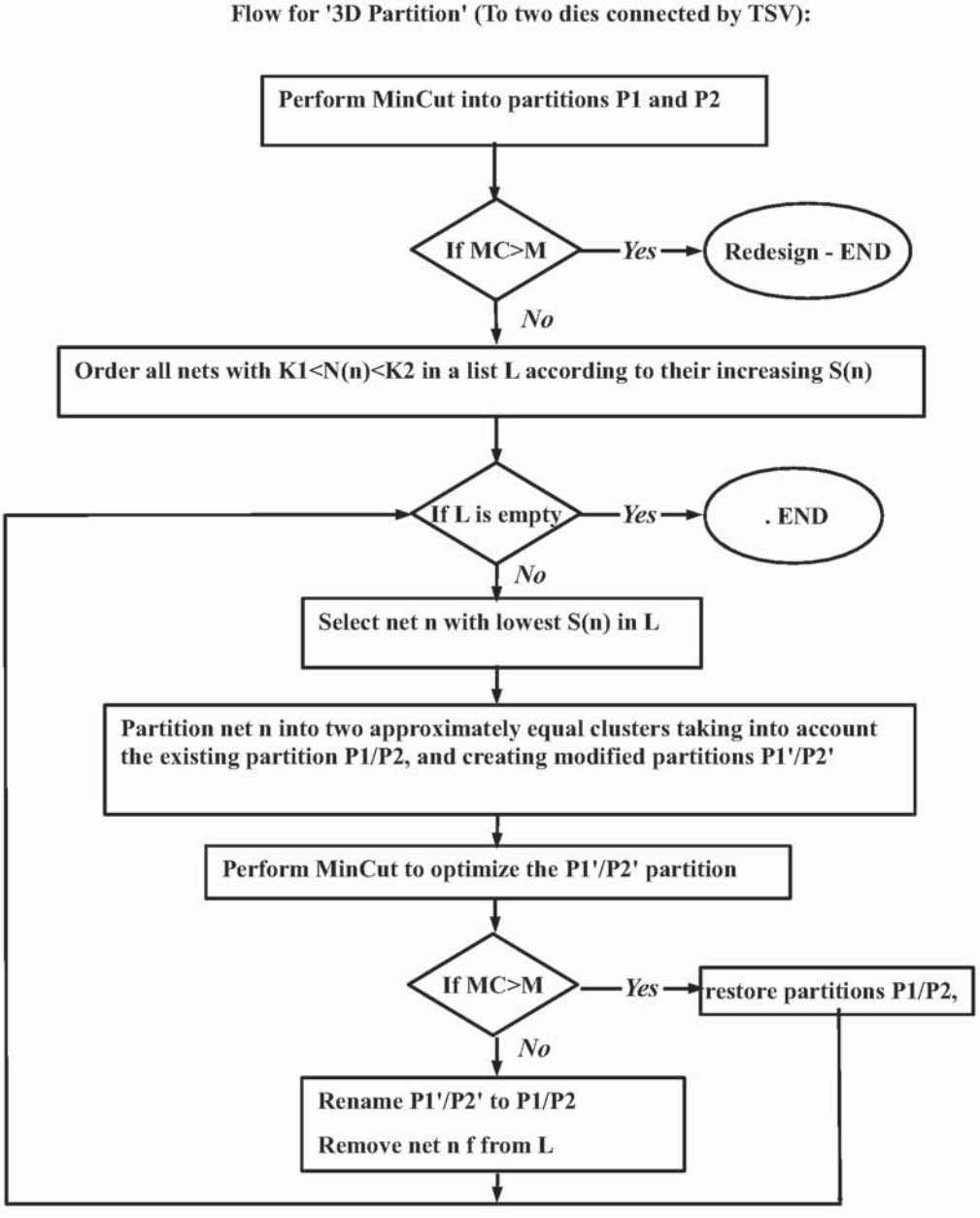

Flow for '3D Partition' (To two dies connected by TSV):
Perform MinCut into partitions P1 and P2
If MC>M
Yes
Redesign - END
No
Order all nets with K1<N(n)<K2 in a list L according to their increasing S(n)
If L is empty
Yes
. END
No
Select net n with lowest S(n) in L
Partition net n into two approximately equal clusters taking into account the existing partition P1/P2, and creating modified partitions P1'/P2'
Perform MinCut to optimize the P1'/P2' partition
If MC>M
Yes
restore partitions P1/P2,
No
Rename P1'/P2' to P1/P2
Remove net n f from L

Fig. 13

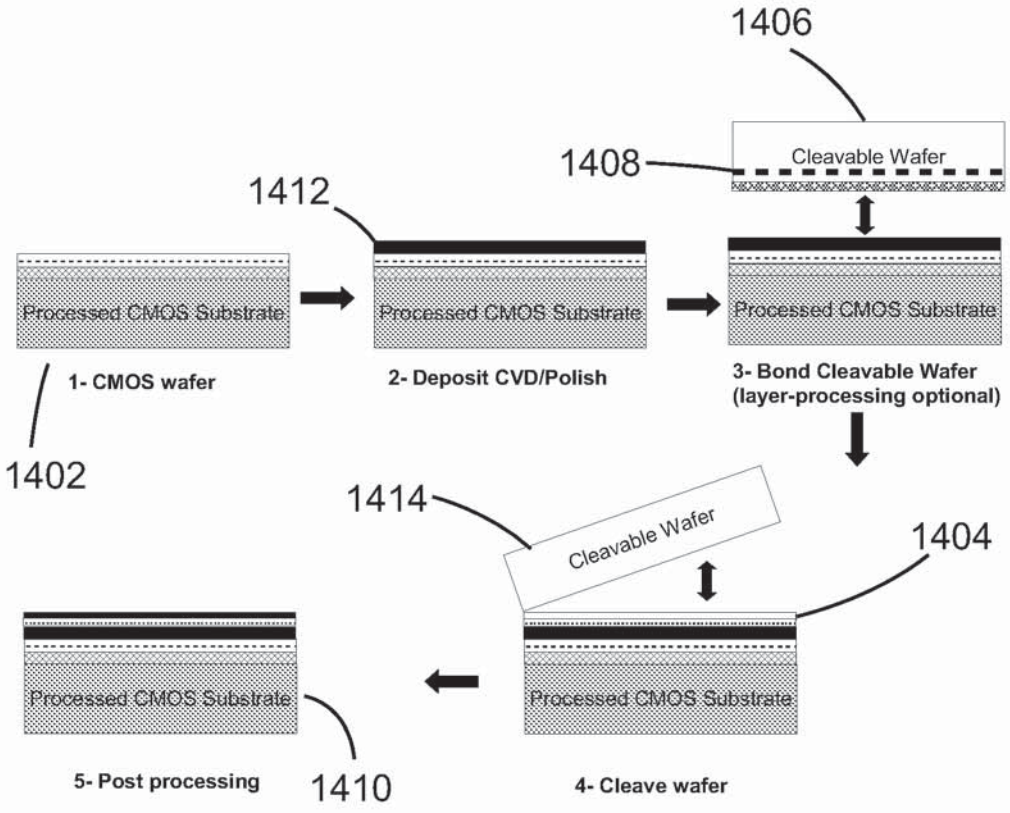

1406
Cleavable Wafer
1408
1412
Processed CMOS Substrate
Processed CMOS Substrate
Processed CMOS Substrate
1- CMOS wafer
2- Deposit CVD/Polish
3- Bond Cleavable Wafer
(layer-processing optional)
1402
1414
Cleavable Wafer
1404
Processed CMOS Substrate
Processed CMOS Substrate
5- Post processing
1410
4- Cleave wafer

Fig 14

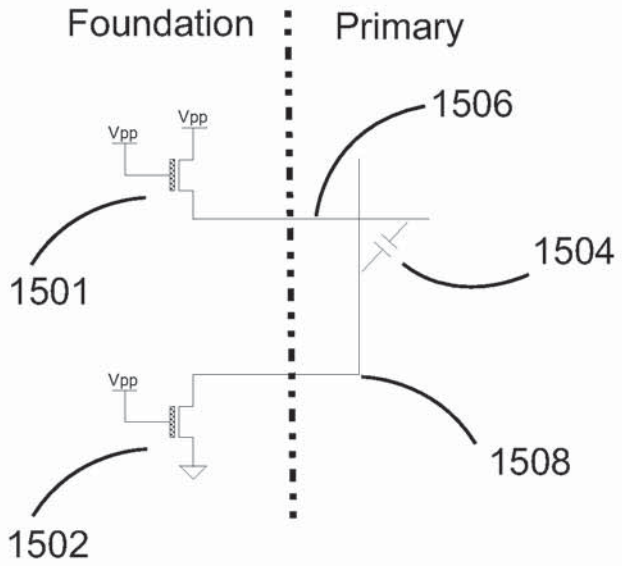


Fig 15

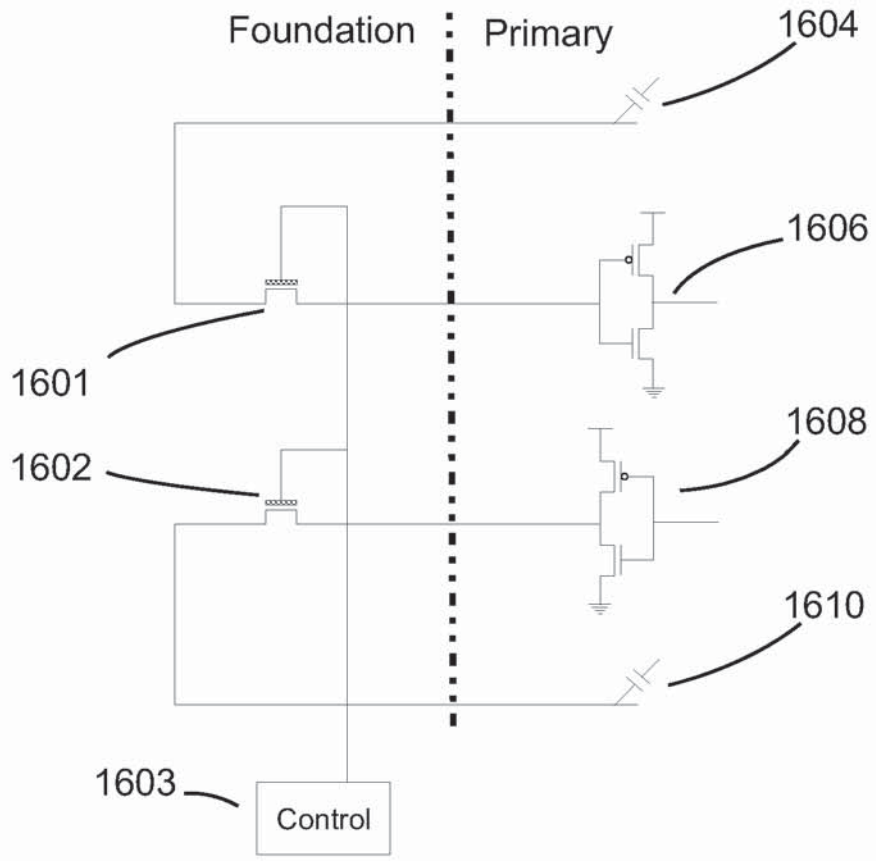

Foundation
Primary
1604
1606
1601
1608
1602
1610
1603
Control

Fig 16

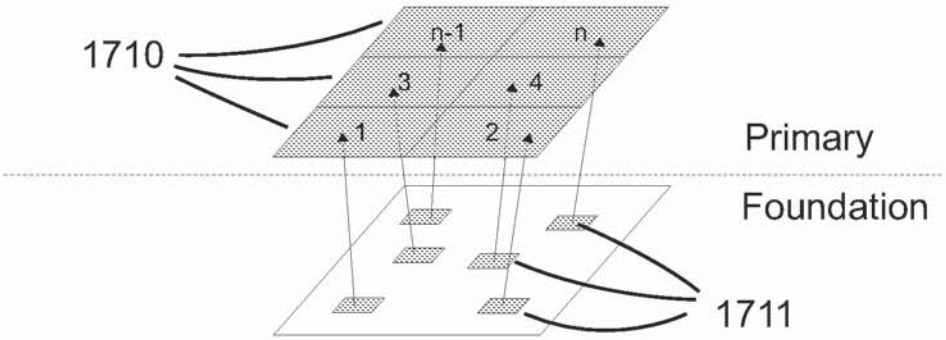


Fig 17A

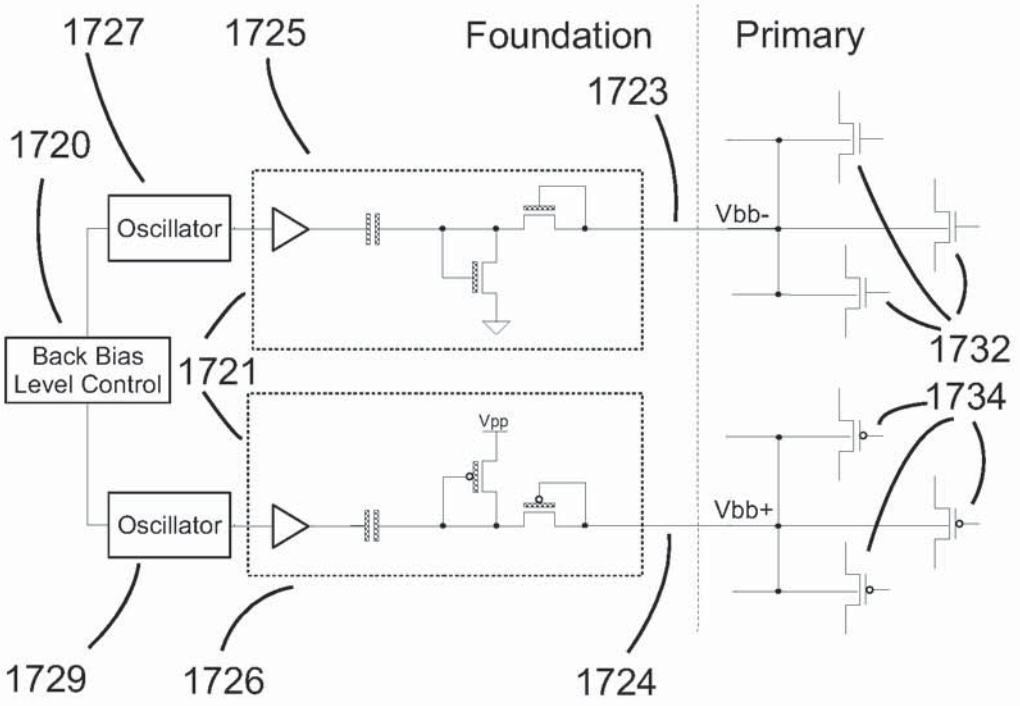


Fig 17B

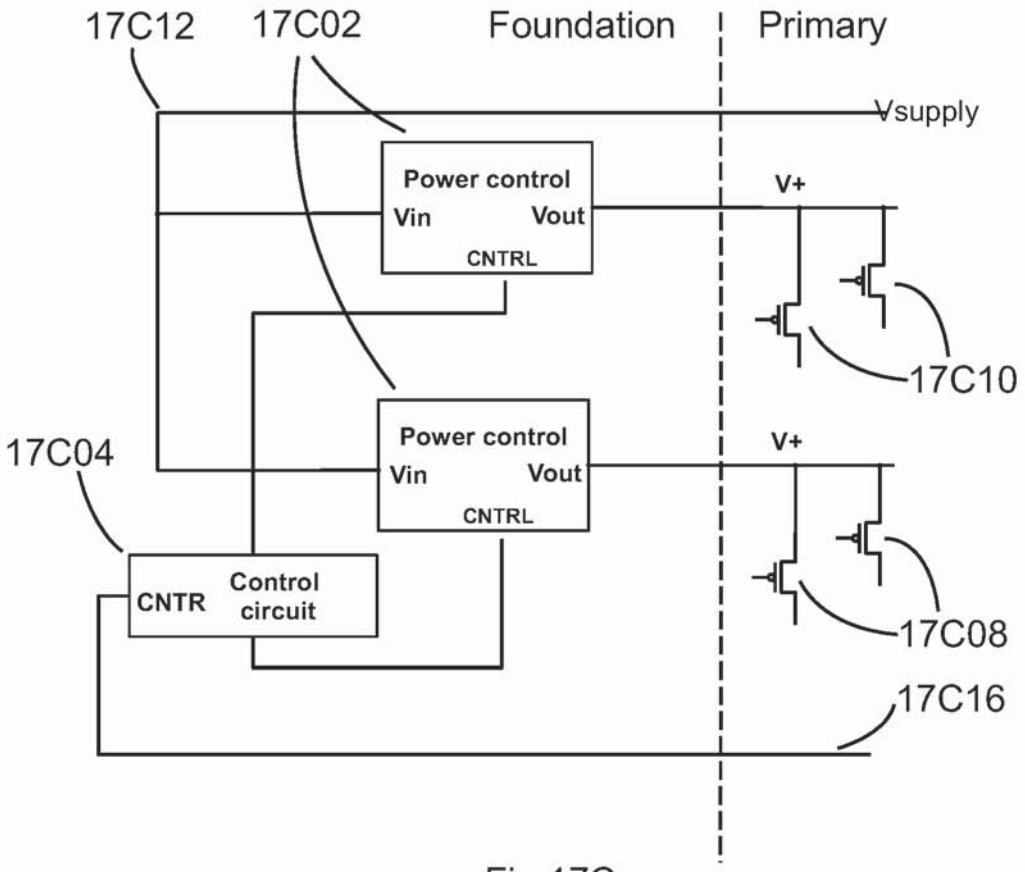

17C12
17C02
Foundation
Primary
Vsupply
Power control
Vin
Vout
CNTRL
V+
17C10
17C04
Power control
Vin
Vout
CNTRL
V+
CNTR
Control circuit
17C08
17C16

Fig 17C

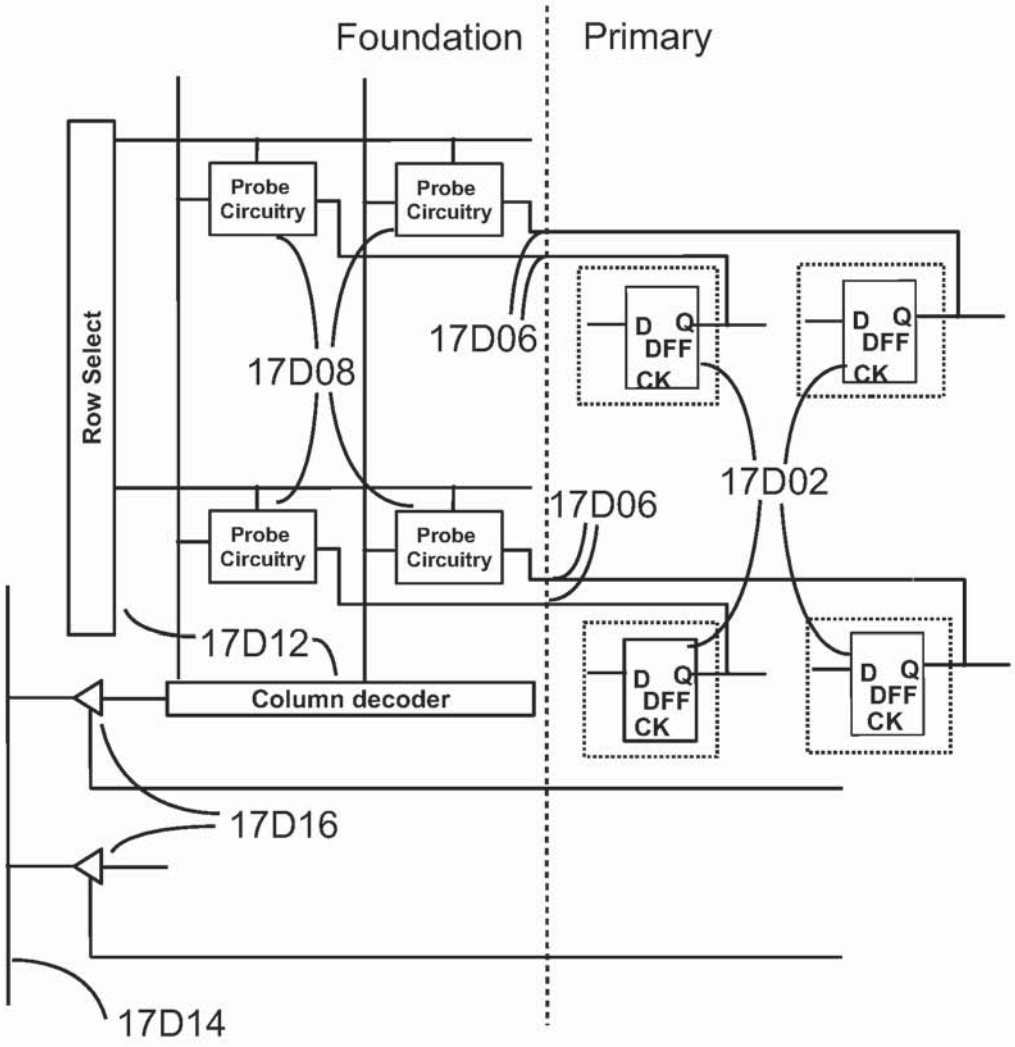

Foundation
Primary
Row Select
Probe Circuitry
Probe Circuitry
Probe Circuitry
Probe Circuitry
17D08
17D06
17D06
17D02
D Q DFF CK
D Q DFF CK
D Q DFF CK
D Q DFF CK
17D12
Column decoder
17D16
17D14

Fig 17D

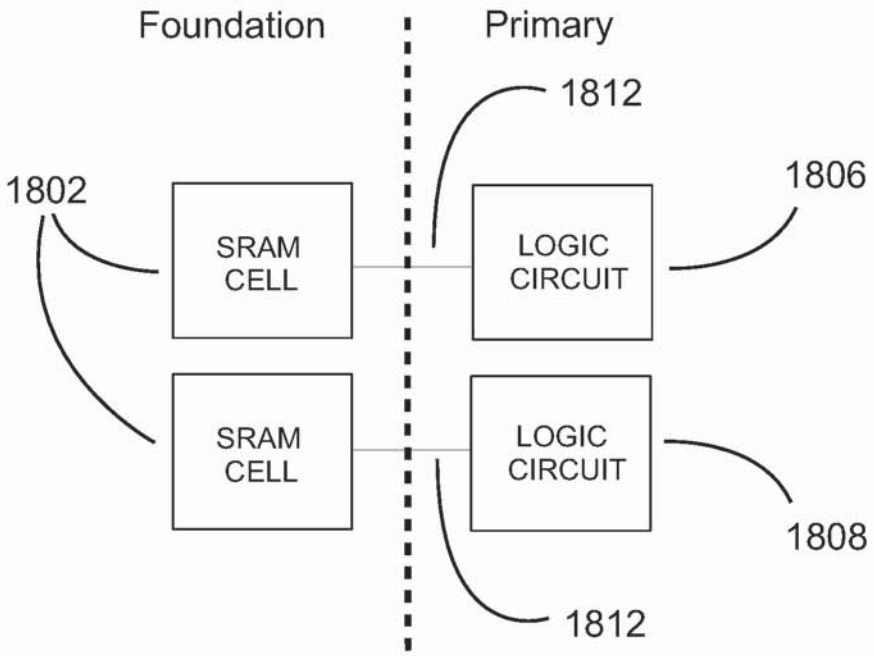

Foundation
Primary
1812
1802
1806
SRAM CELL
LOGIC CIRCUIT
SRAM CELL
LOGIC CIRCUIT
1808
1812

Figure 18

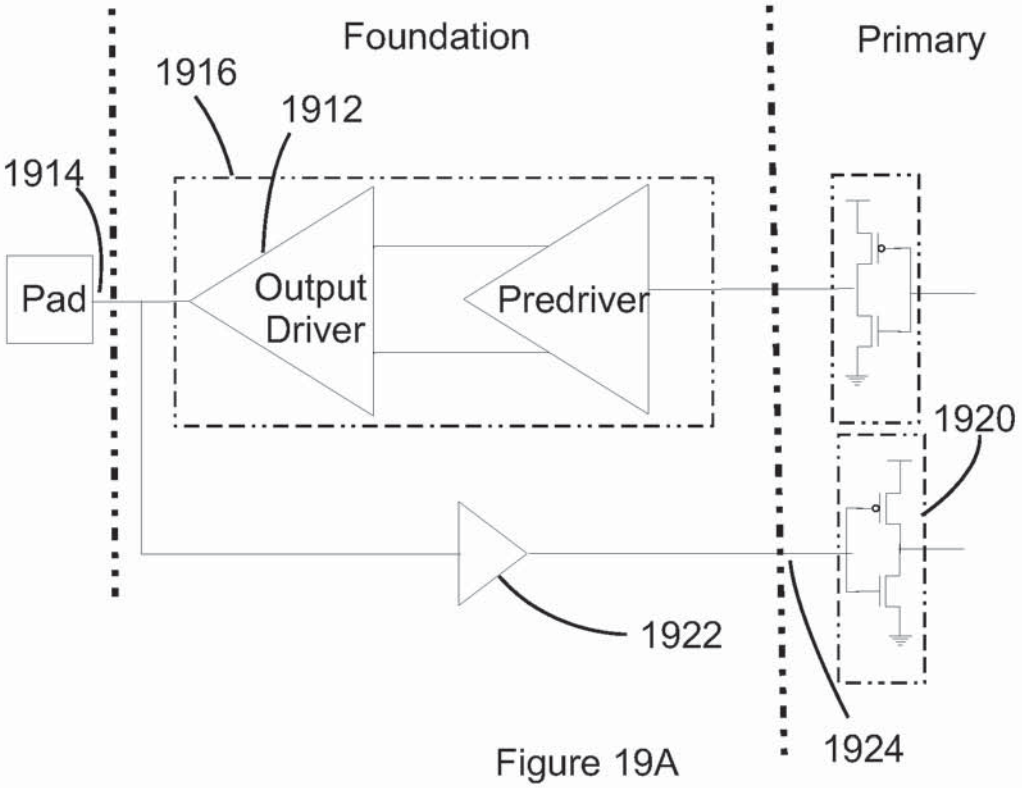


Figure 19A

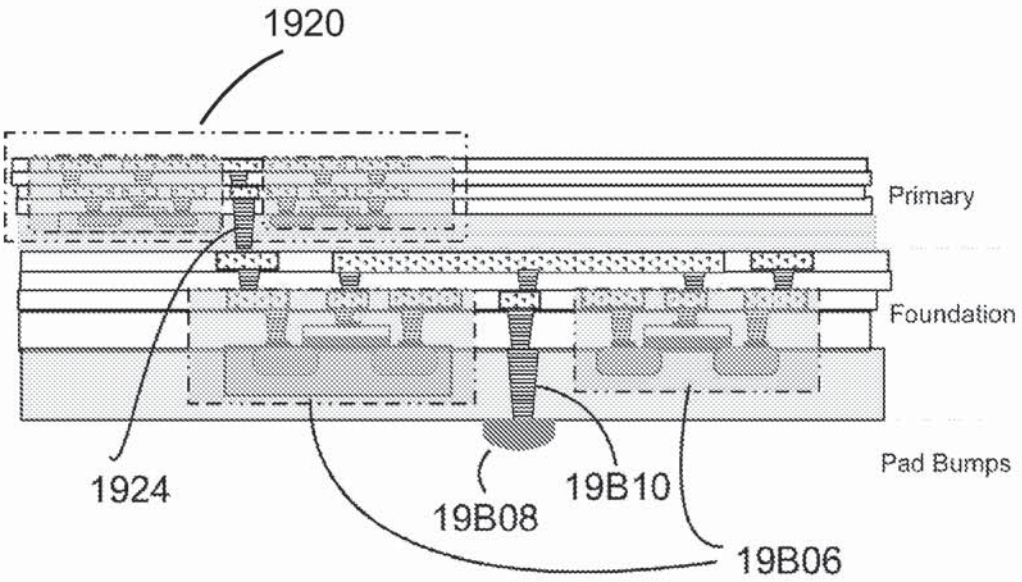


Figure 19B

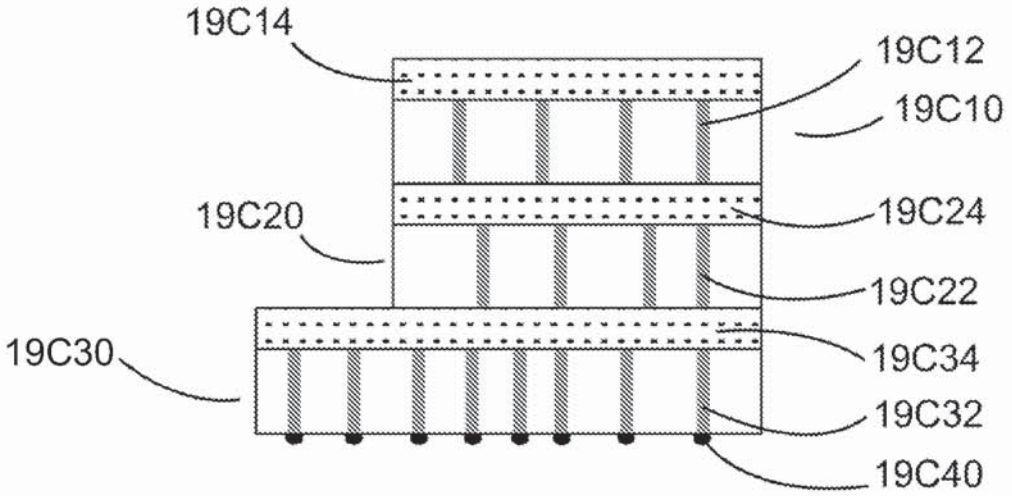

19C14
19C12
19C10
19C20
19C24
19C22
19C30
19C34
19C32
19C40

Fig 19C

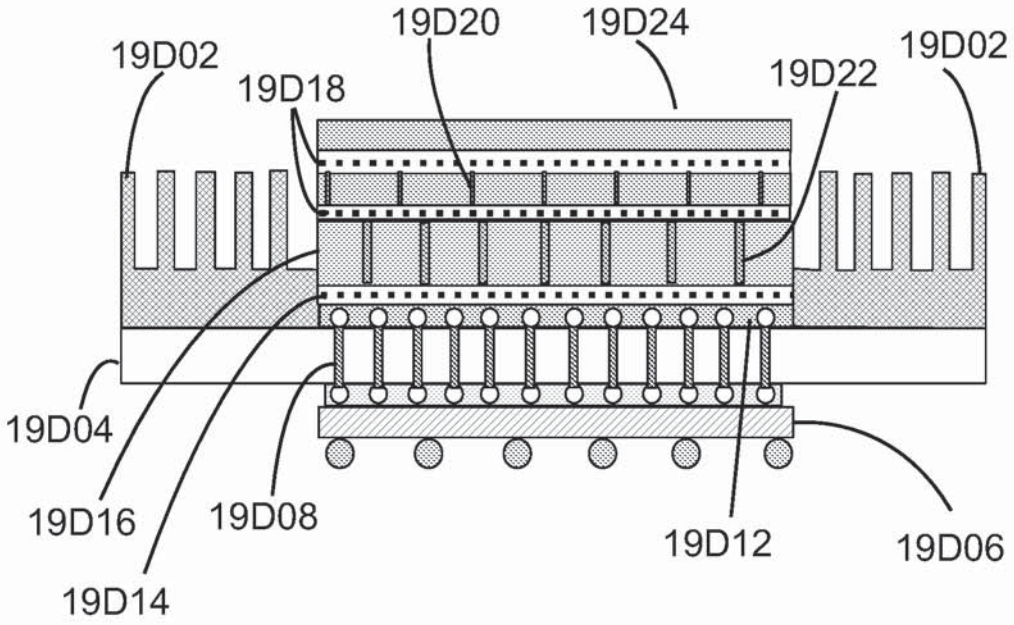


Fig 19D

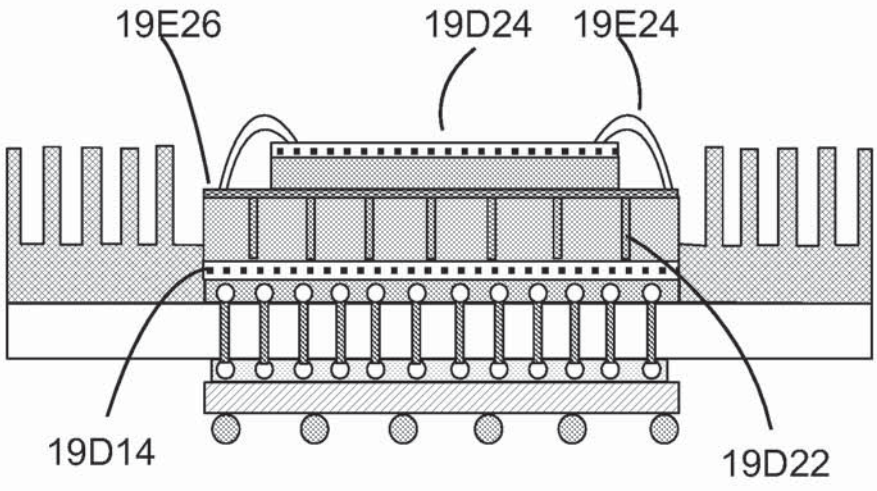


Fig 19E

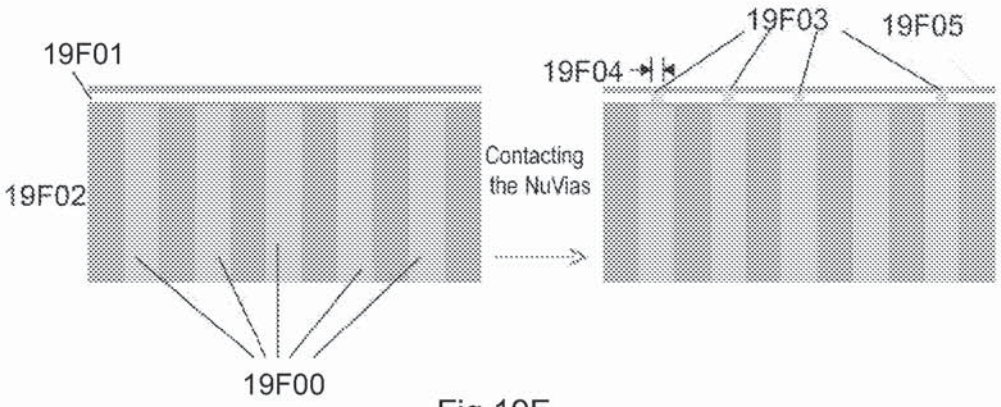


Fig 19F



Prior Art

Fig 19G

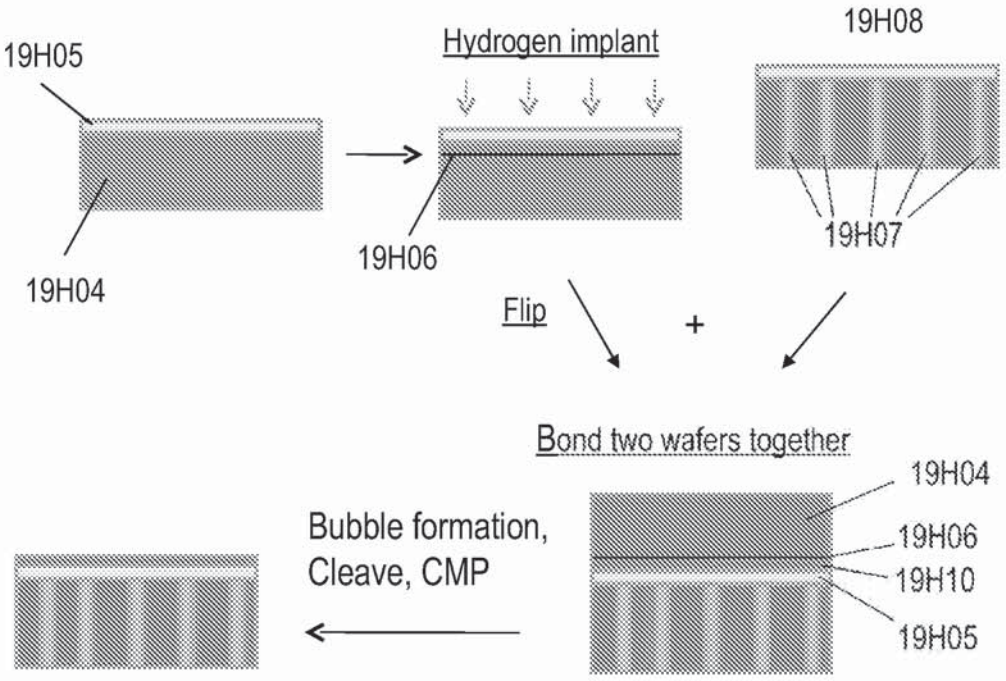

19H05
19H04
Hydrogen implant
19H06
19H08
19H07
Flip
+
Bond two wafers together
19H04
19H06
19H10
19H05
Bubble formation,
Cleave, CMP

Fig 19H

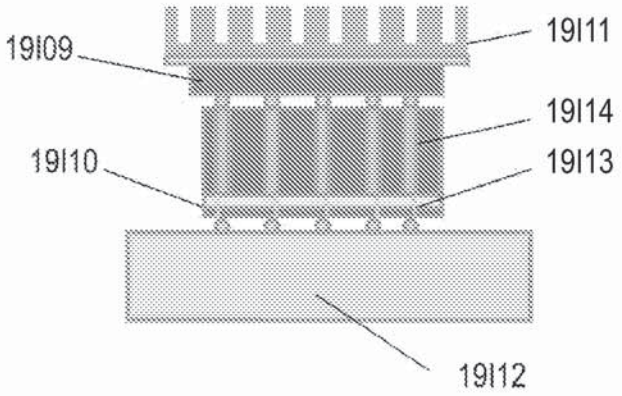


Fig 19I

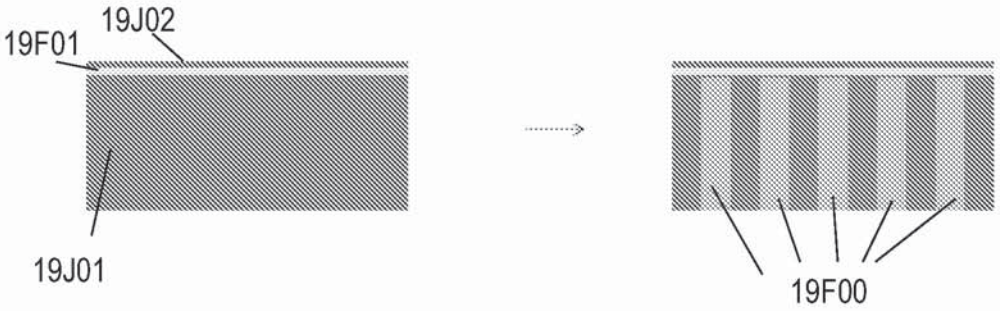


Fig 19J

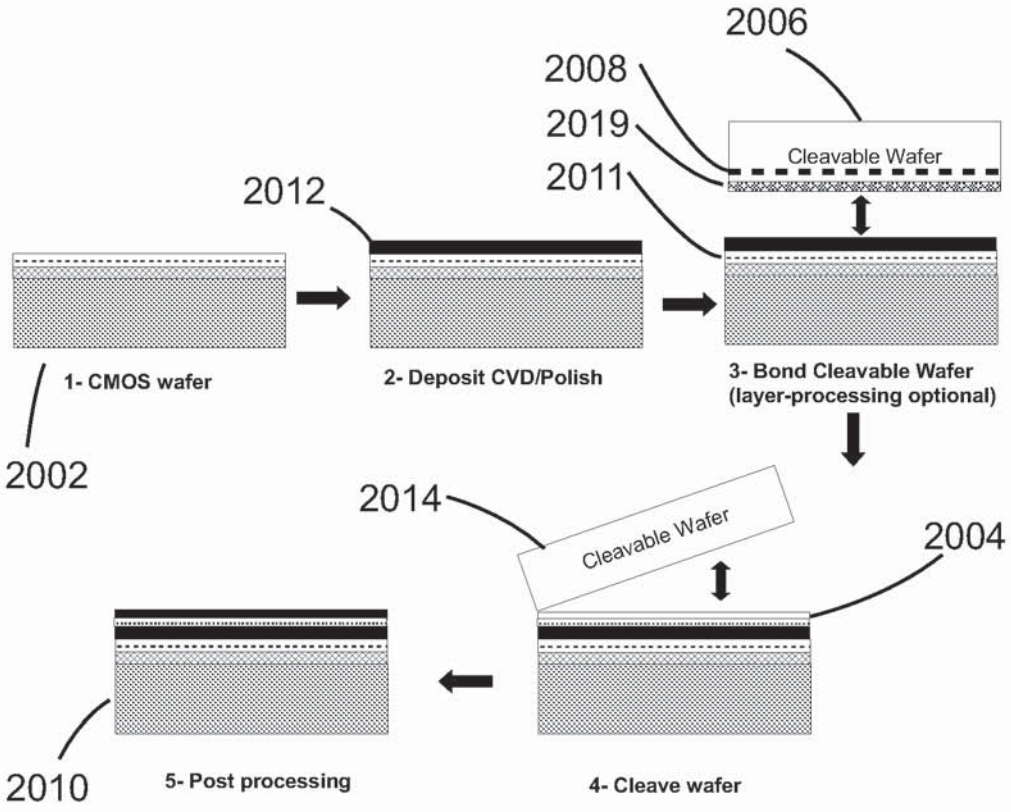

2006
2008
2019
2011
Cleavable Wafer
2012
1- CMOS wafer
2- Deposit CVD/Polish
3- Bond Cleavable Wafer
(layer-processing optional)
2002
2014
Cleavable Wafer
2004
2010
5- Post processing
4- Cleave wafer

Fig 20

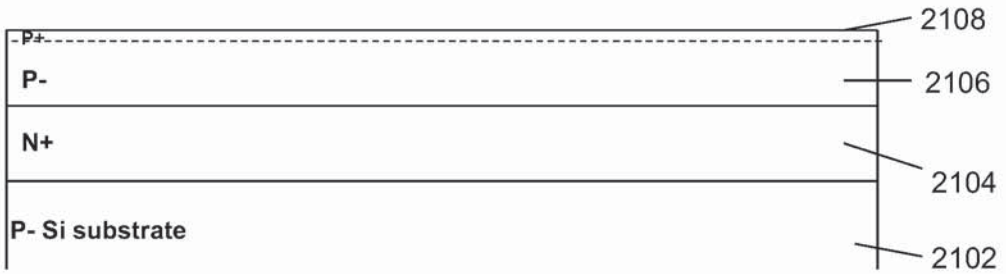


Fig 21A

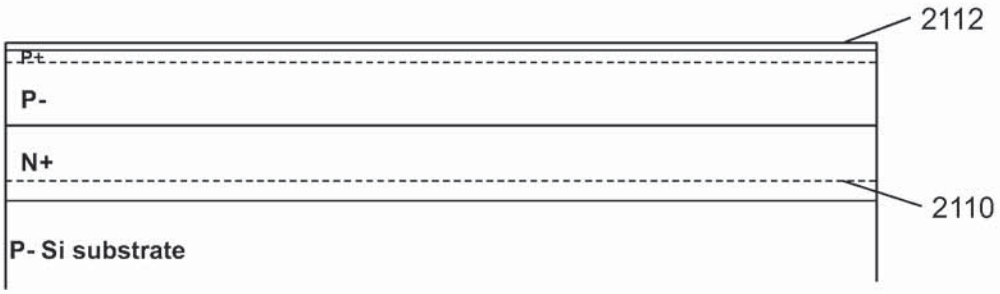


Fig 21B

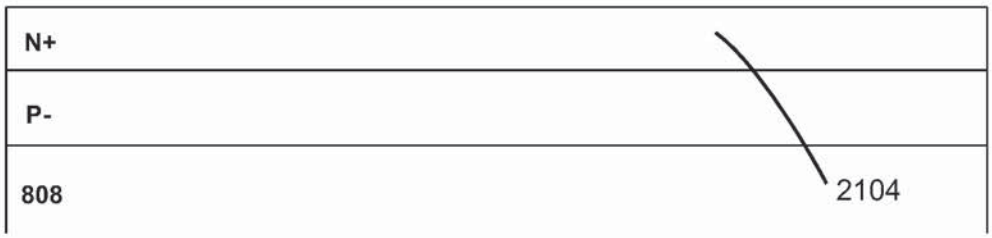


Fig 22A

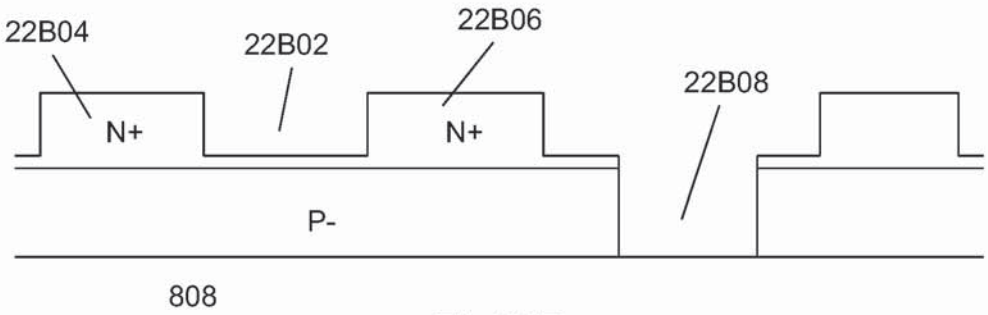


Fig 22B

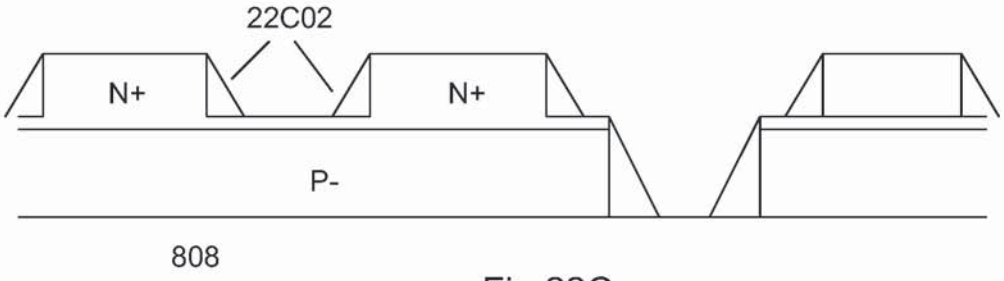


Fig 22C

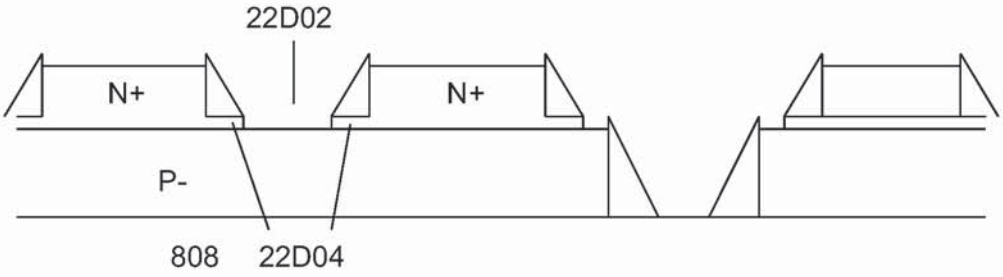


Fig 22D

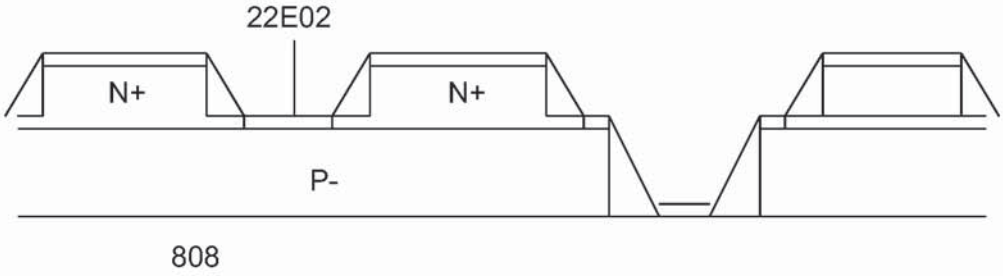


Fig 22E

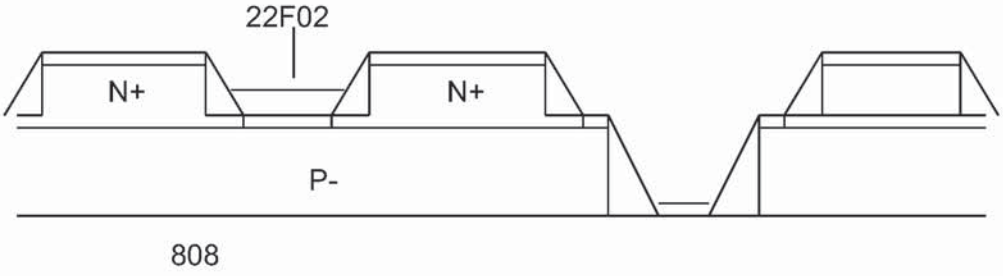


Fig 22F

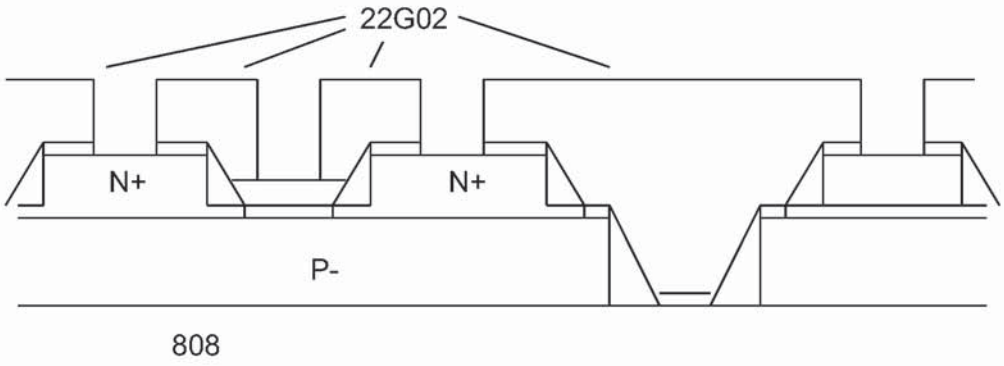


Fig 22G

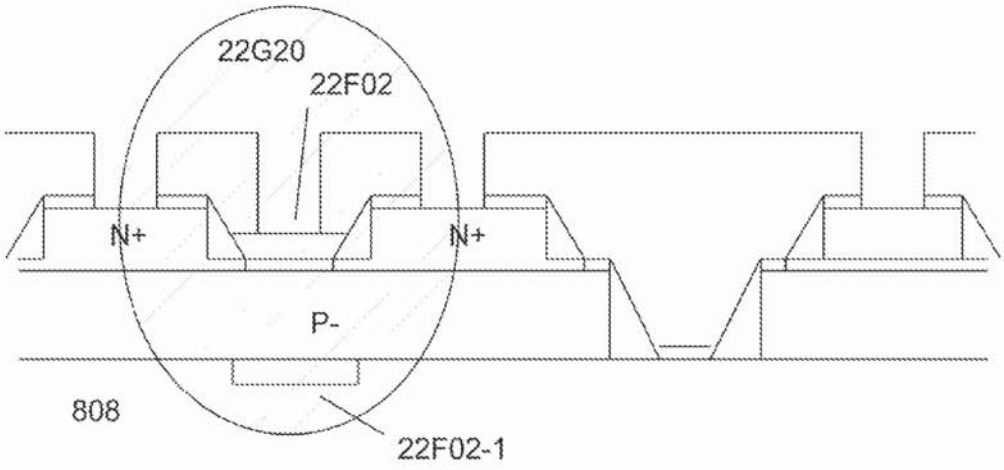


Fig 22H

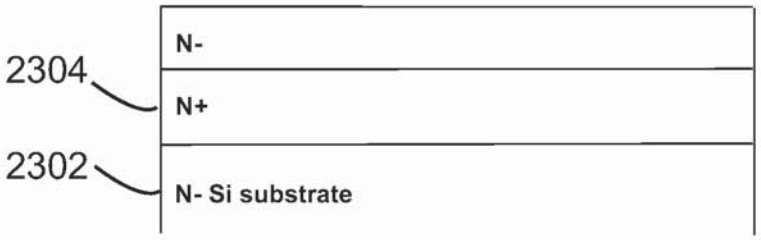


Fig 23A

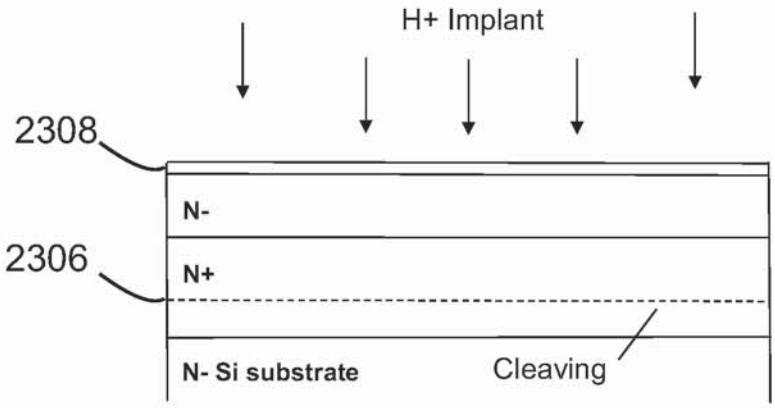


Fig 23B

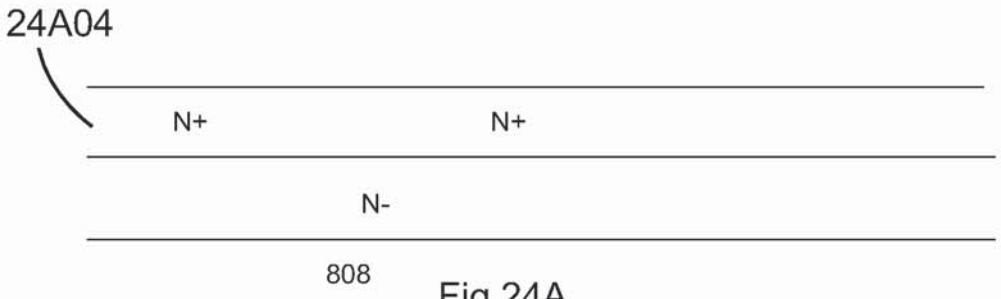


Fig 24A

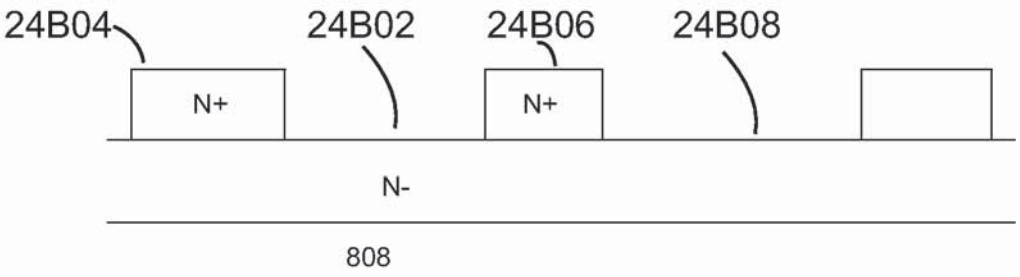


Fig 24B

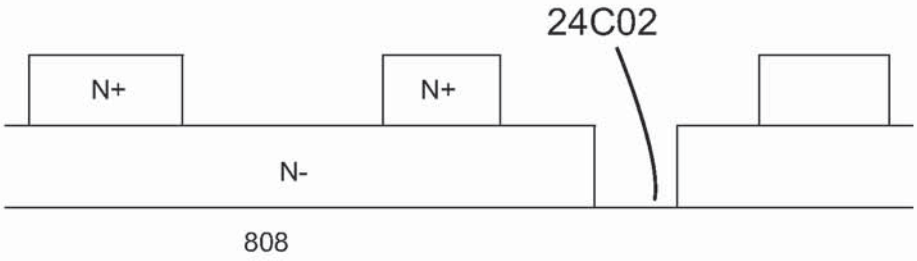


Fig 24C

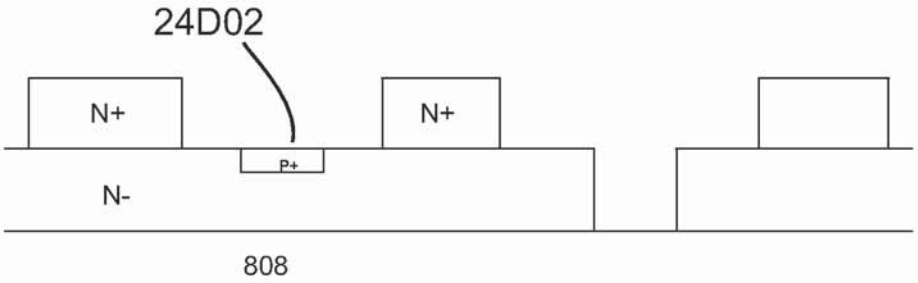


Fig 24D

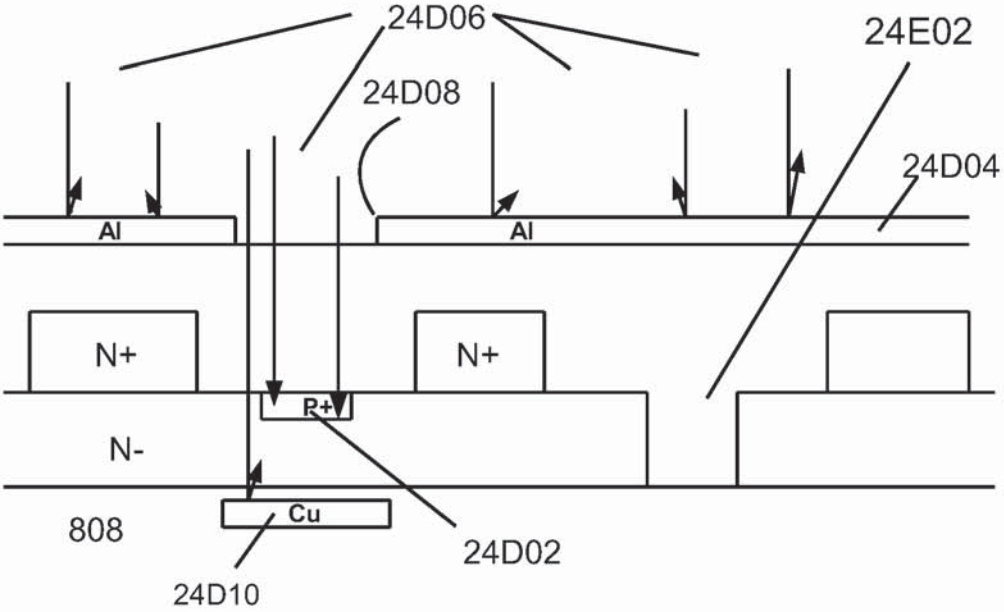


Fig. 24E

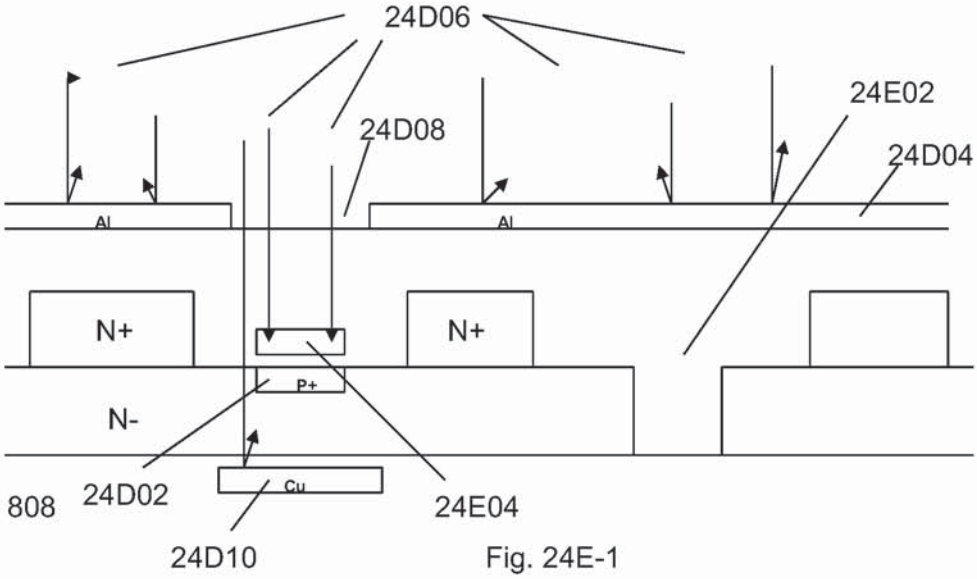


Fig. 24E-1

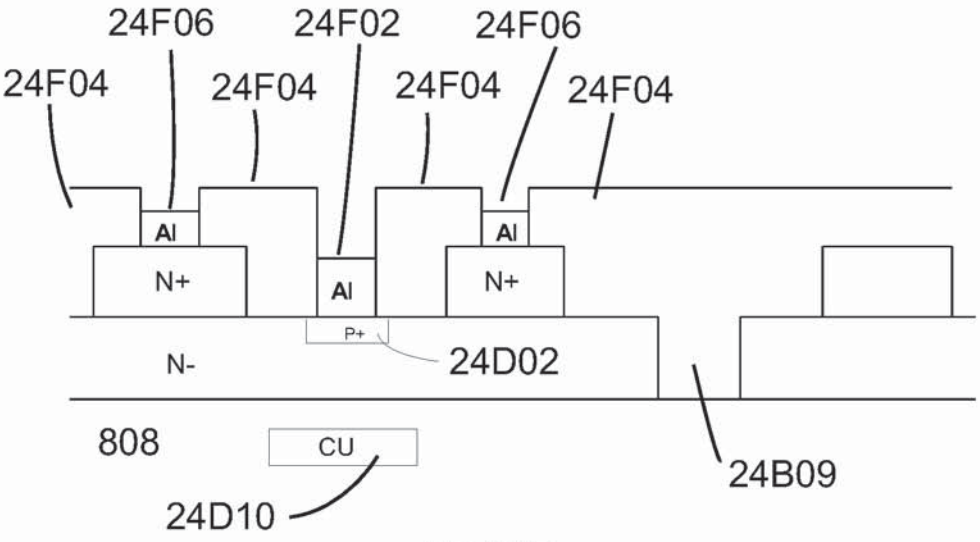


Fig 24F

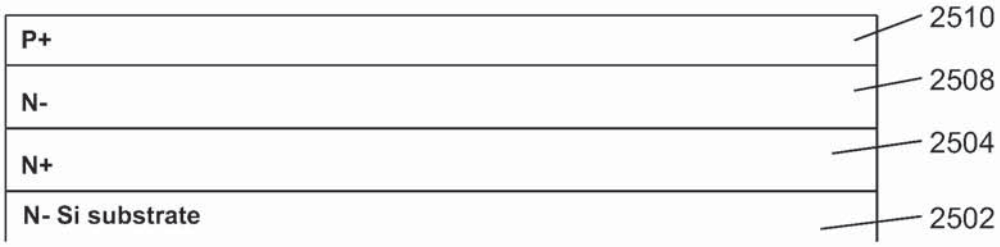


Fig 25A

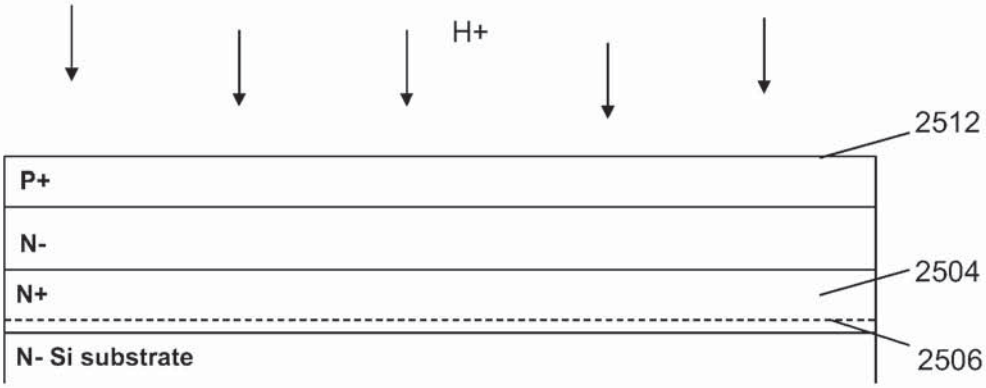


Fig 25B

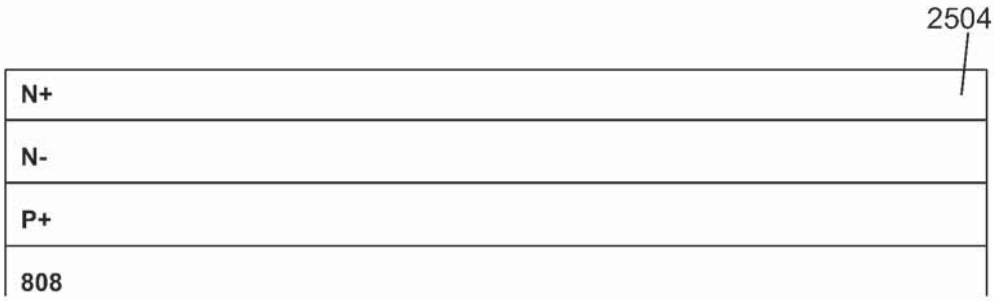


Fig 26A

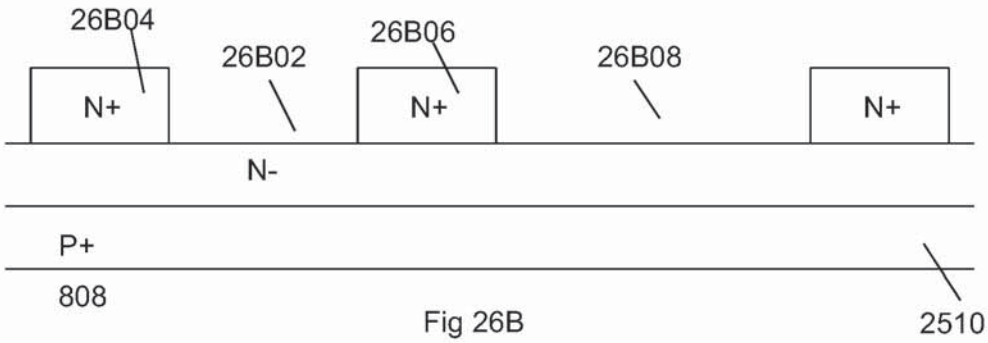


Fig 26B

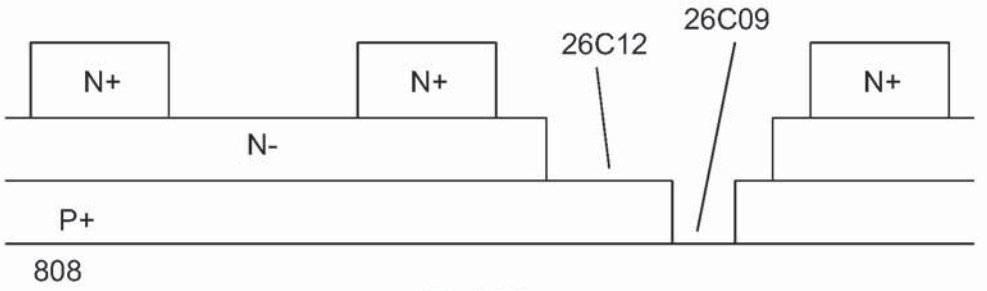


Fig 26C

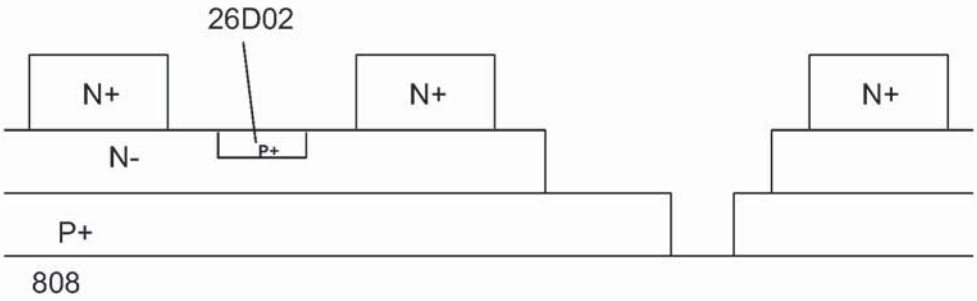


Fig 26D

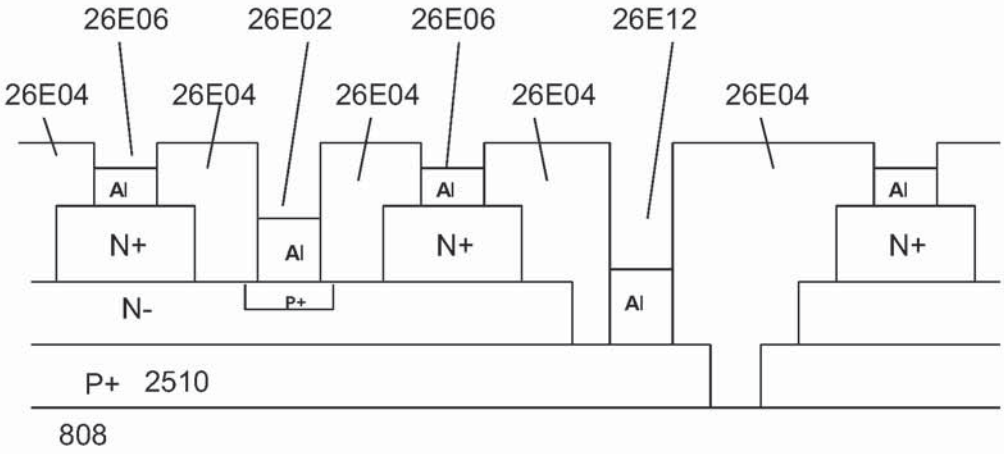


Fig 26E

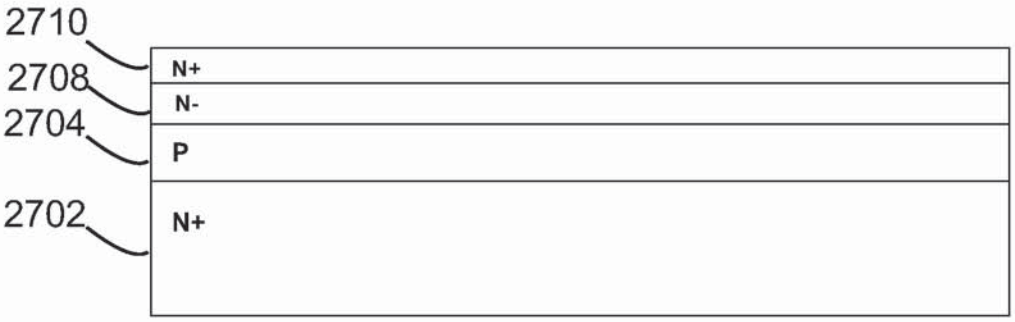


Fig 27A

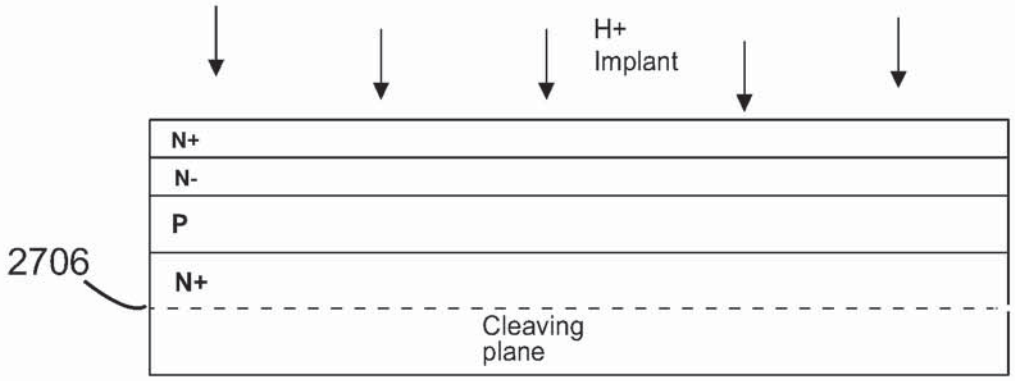


Fig 27B

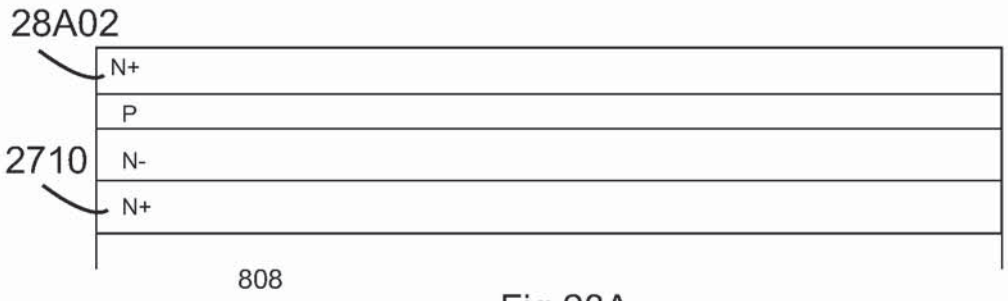


Fig 28A

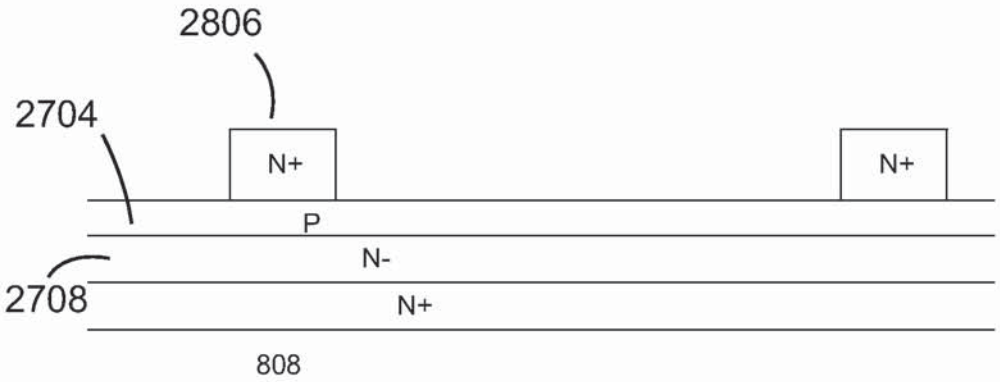


Fig 28B

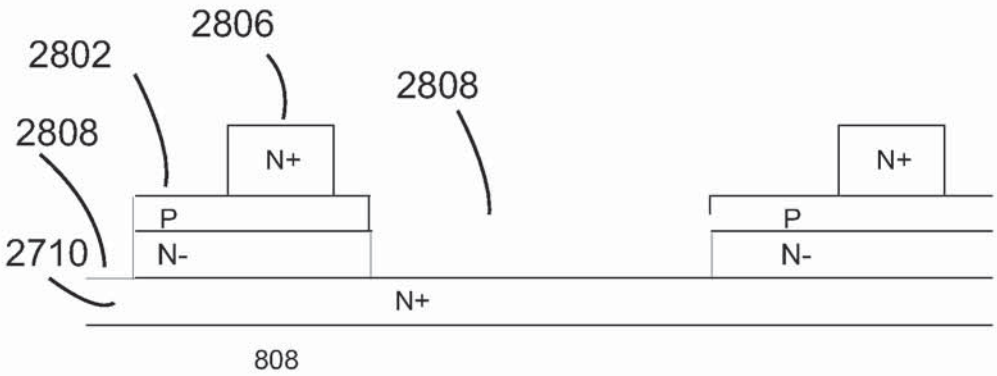


Fig 28C

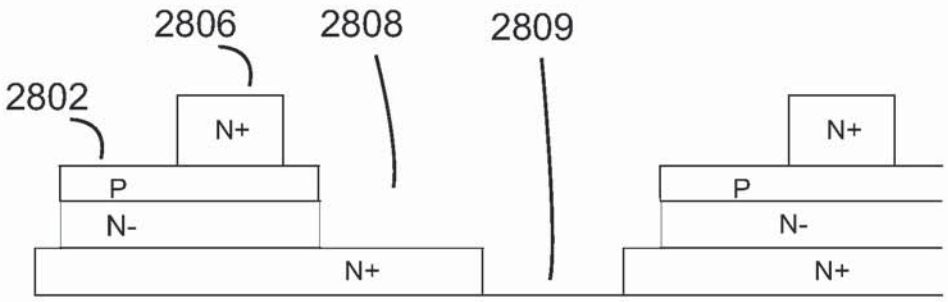


Fig 28D

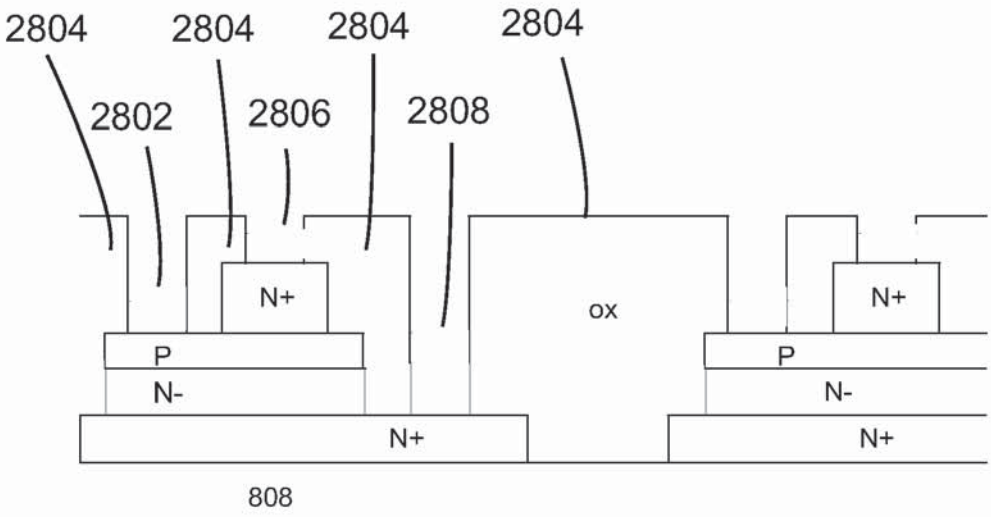


Fig 28E

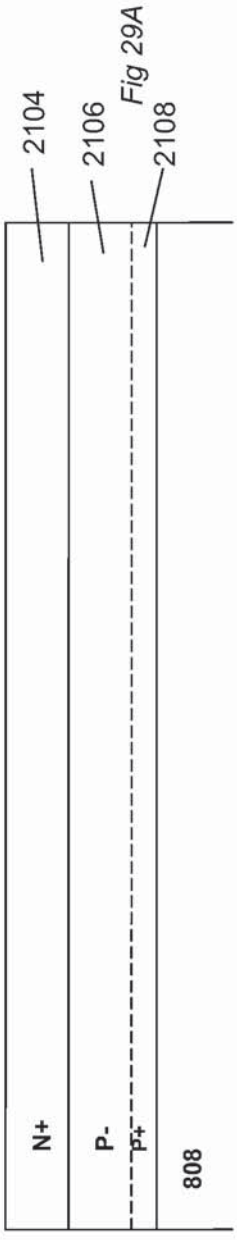


Fig 29A

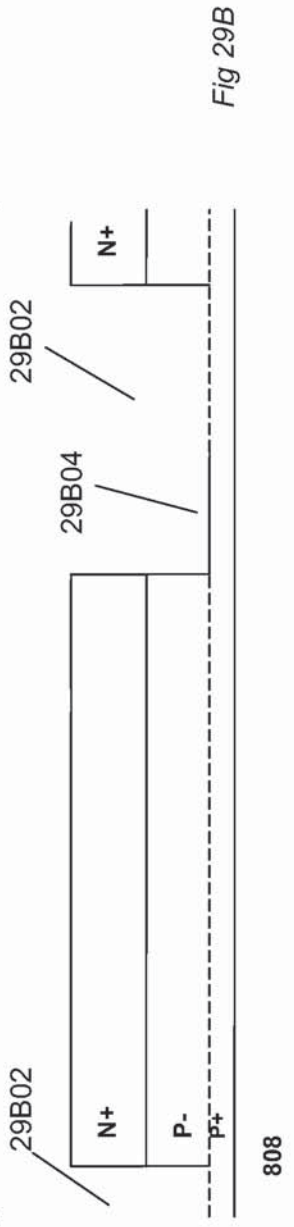


Fig 29B

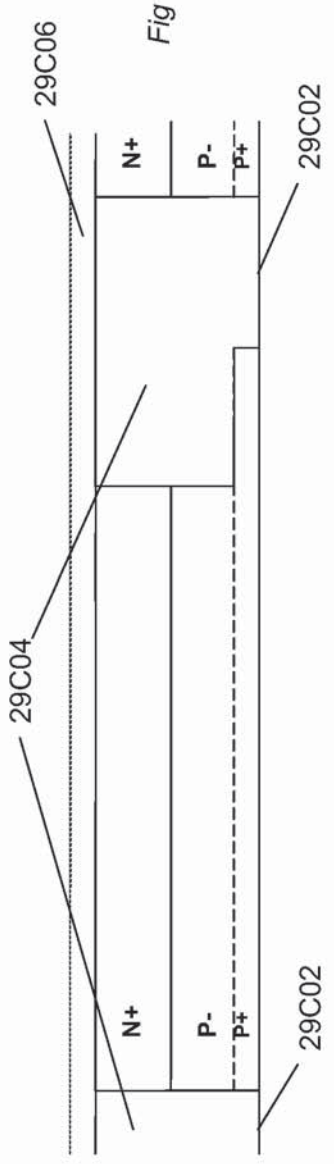


Fig 29C

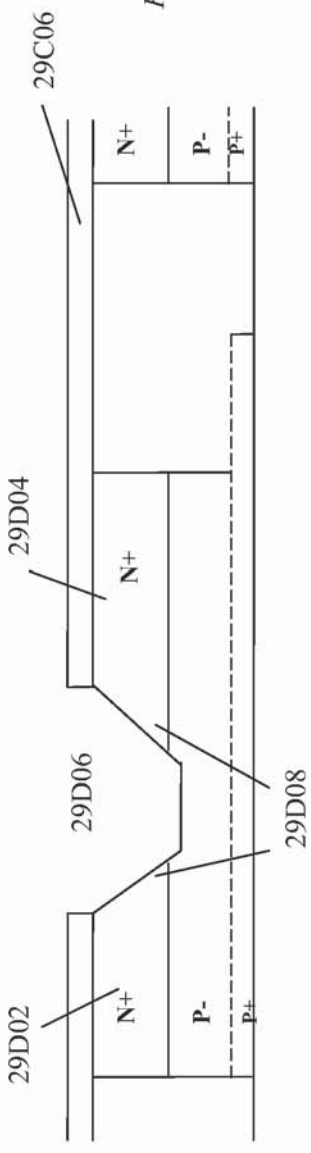


Fig 29D

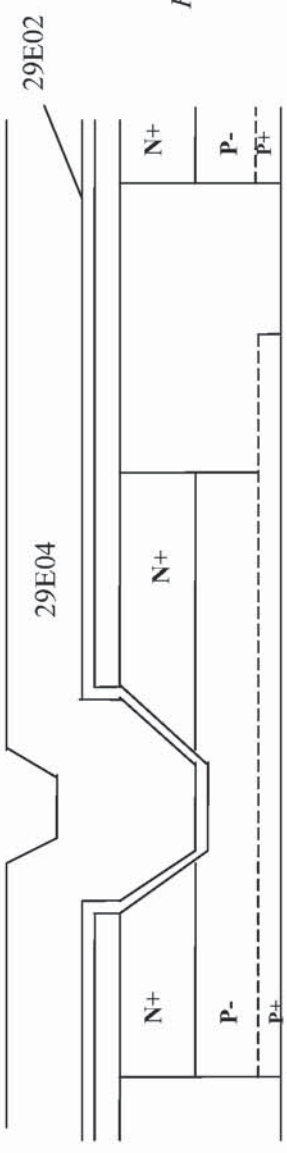


Fig 29E

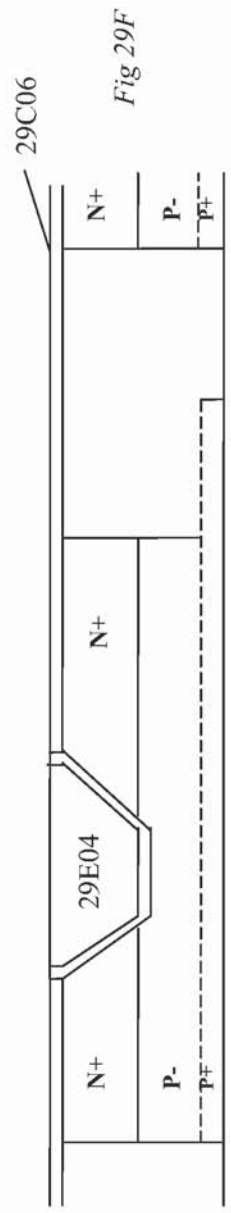


Fig 29F

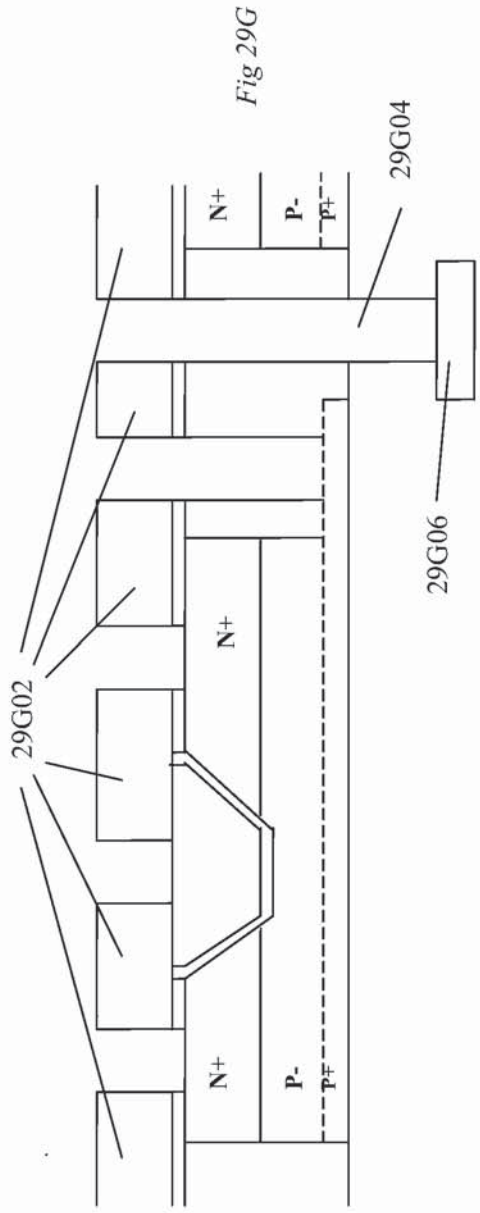


Fig 29G

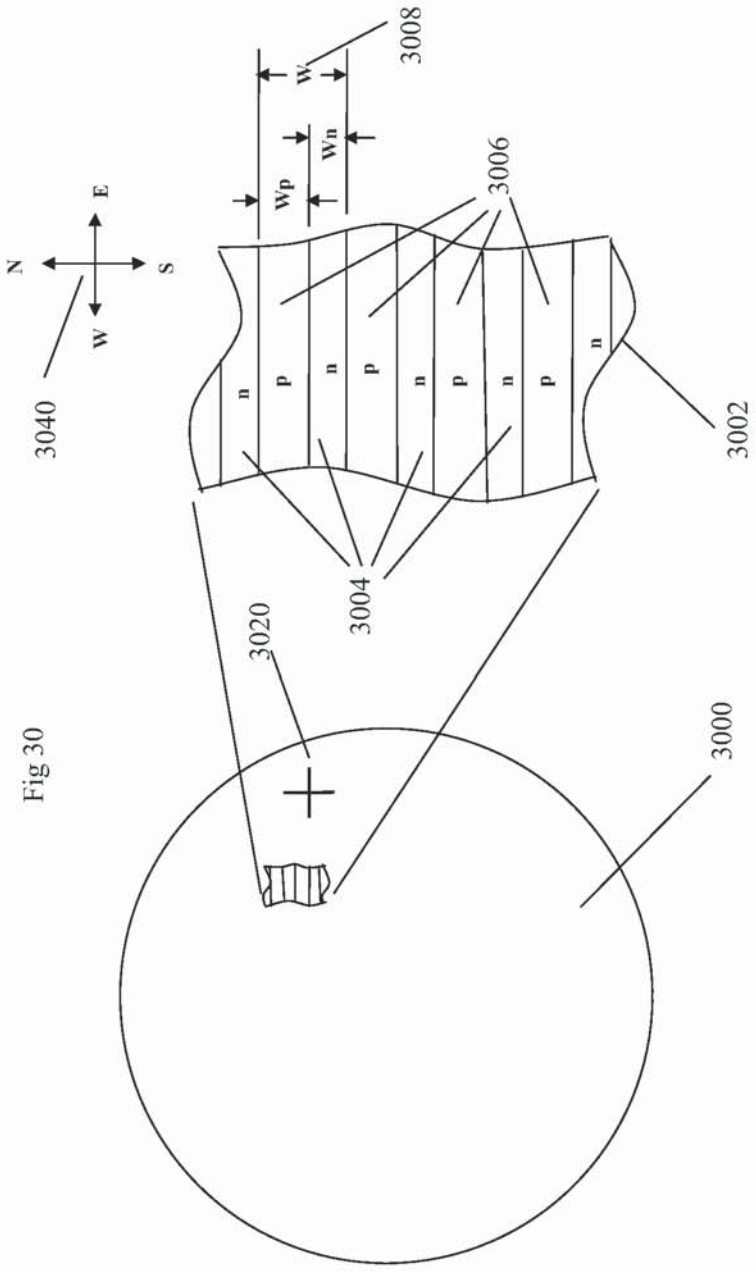


Fig 30

Fig 31

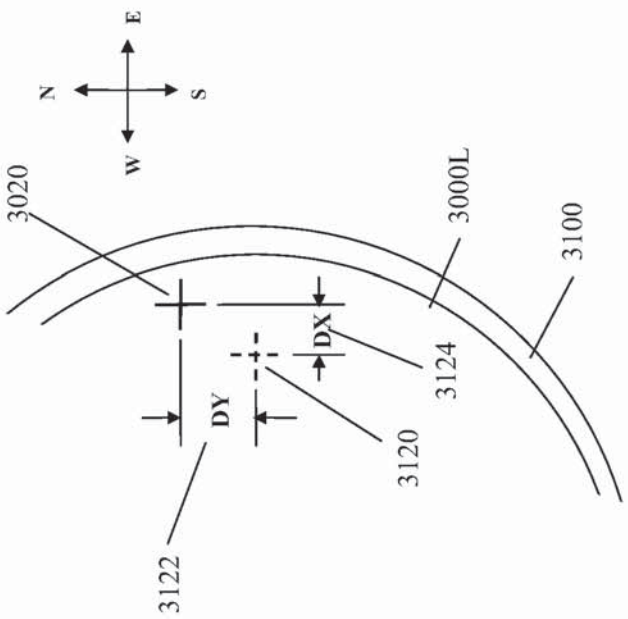
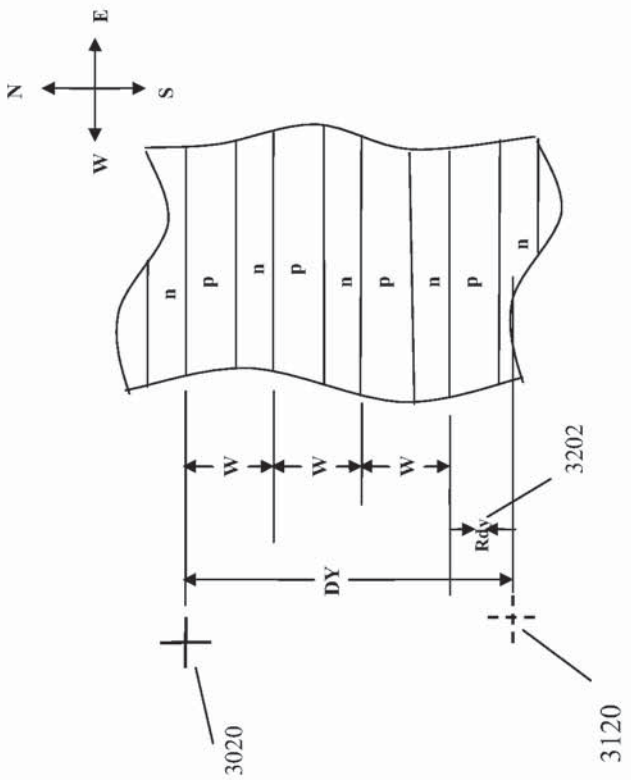


Fig 32



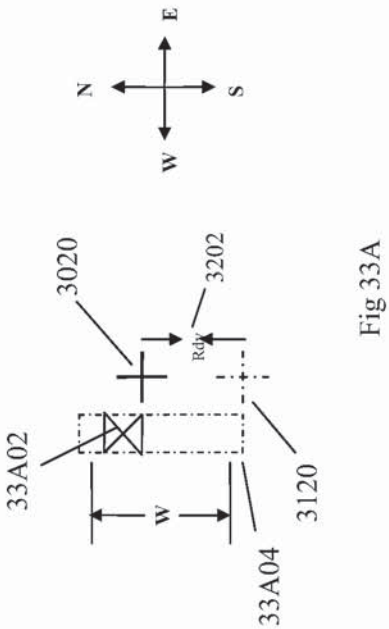


Fig 33A

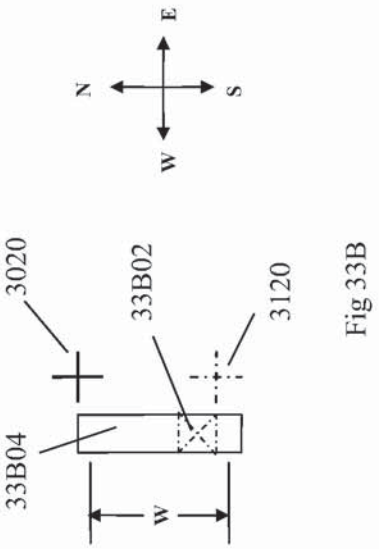


Fig 33B

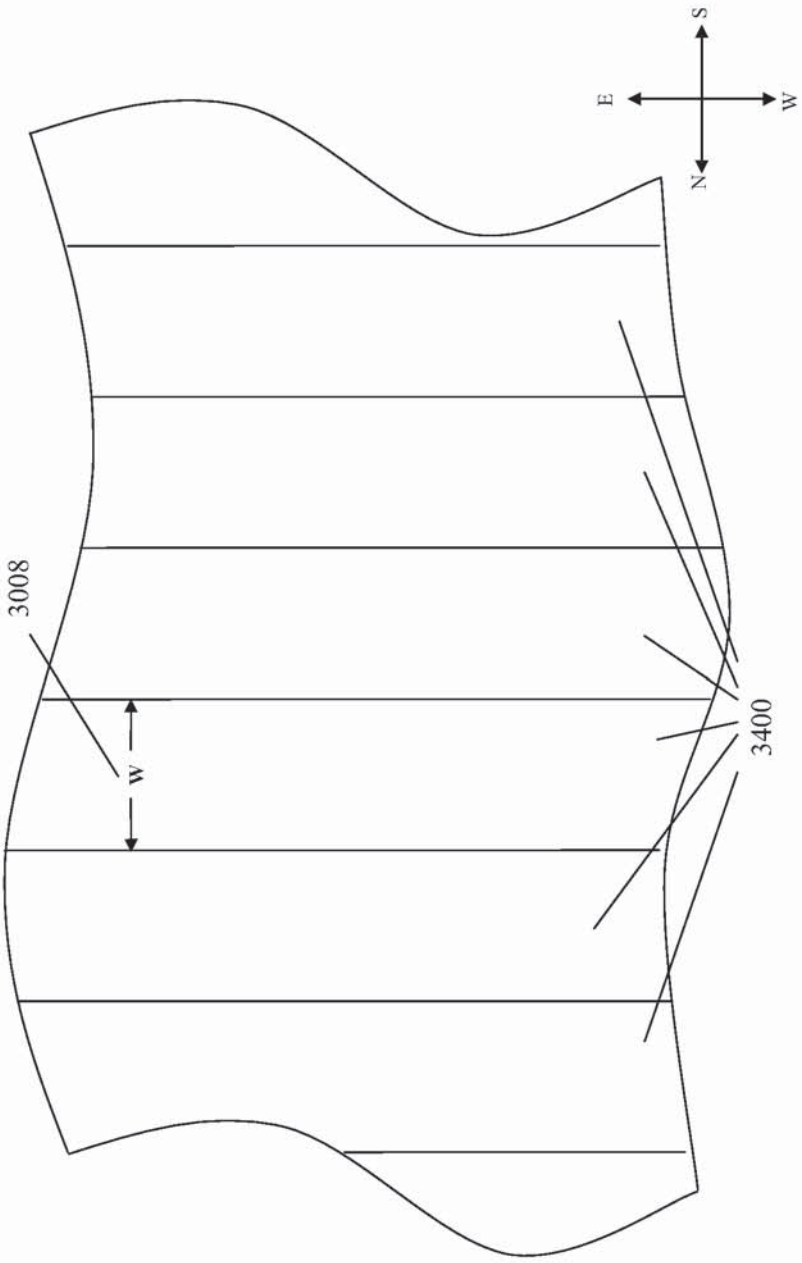
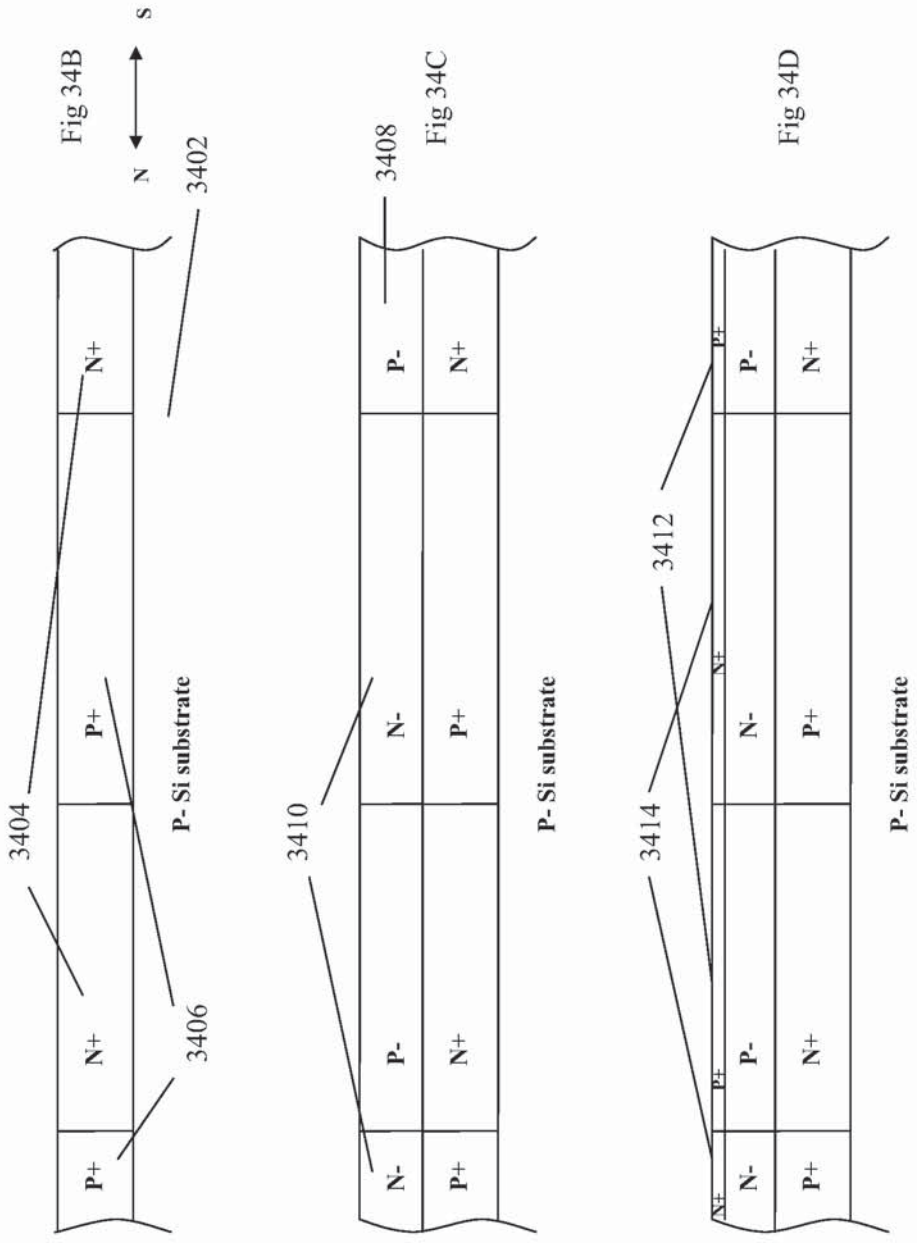


Fig 34A


Fig 34B
S
N
3402
3404
3406
N+
P+
N+
P+
P- Si substrate
Fig 34C
3408
3410
P-
N-
N+
P+
P- Si substrate
Fig 34D
3412
3414
P+
N+
P-
N-
N+
P+
P- Si substrate

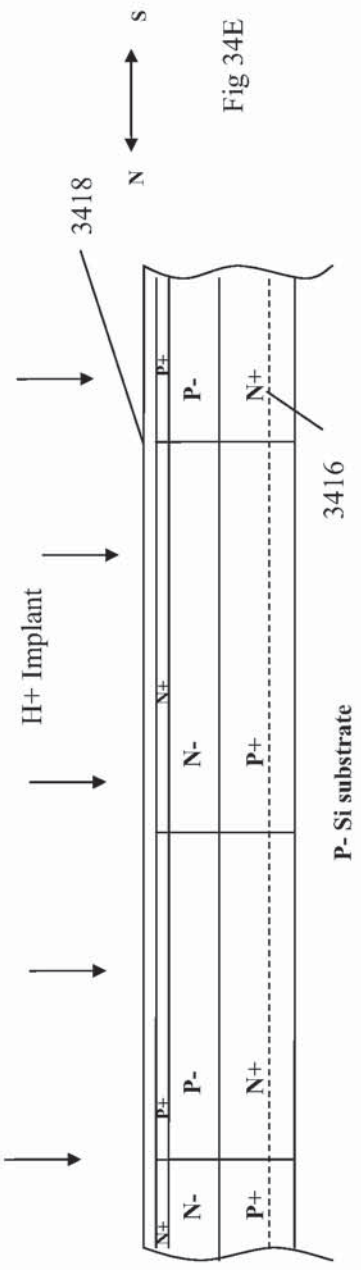
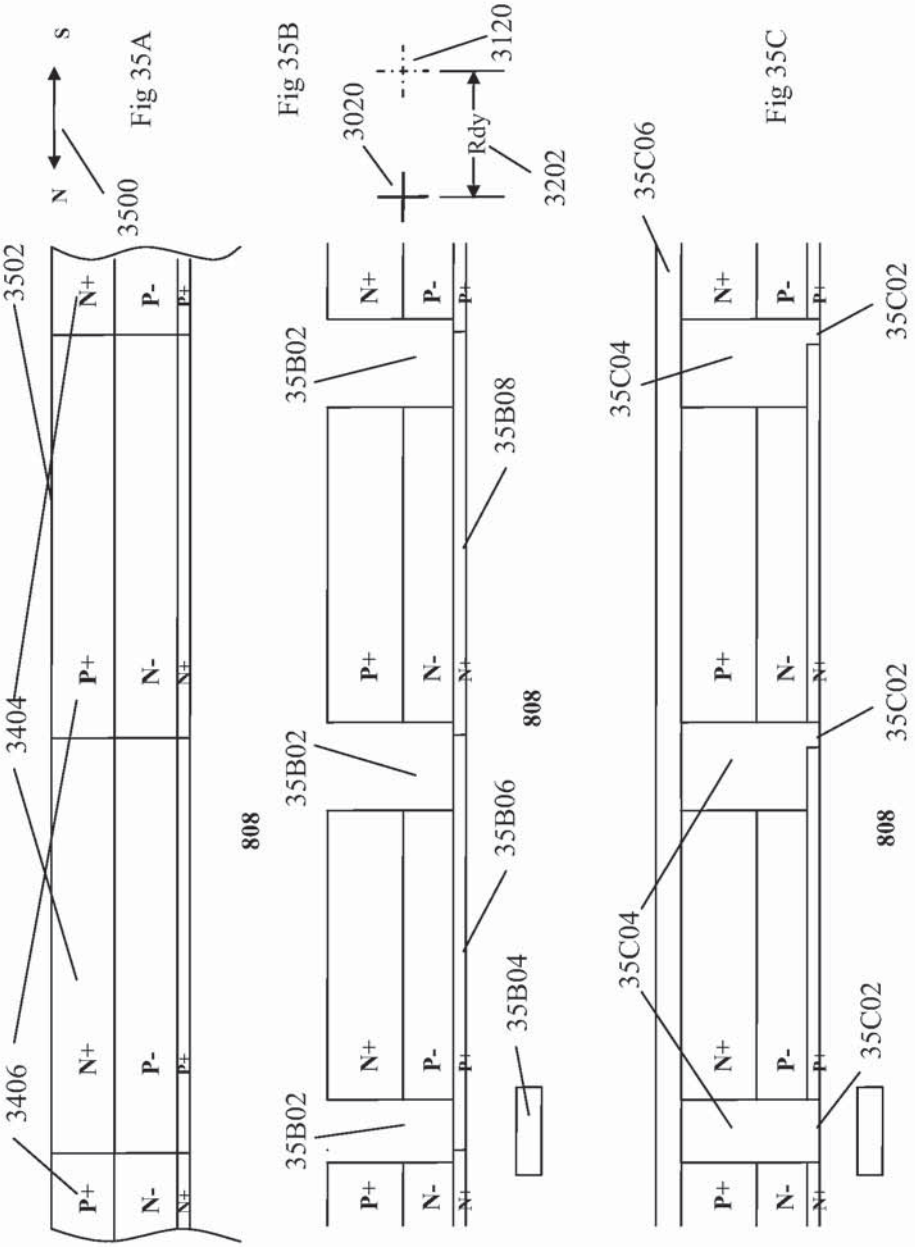


Fig 34E


S
N
3500
Fig 35A
3502
3404
3406
N+
P-
P+
N-
808
Fig 35B
3020
3120
Rdy
3202
35B02
35B08
35B06
35B04
Fig 35C
35C06
35C04
35C02

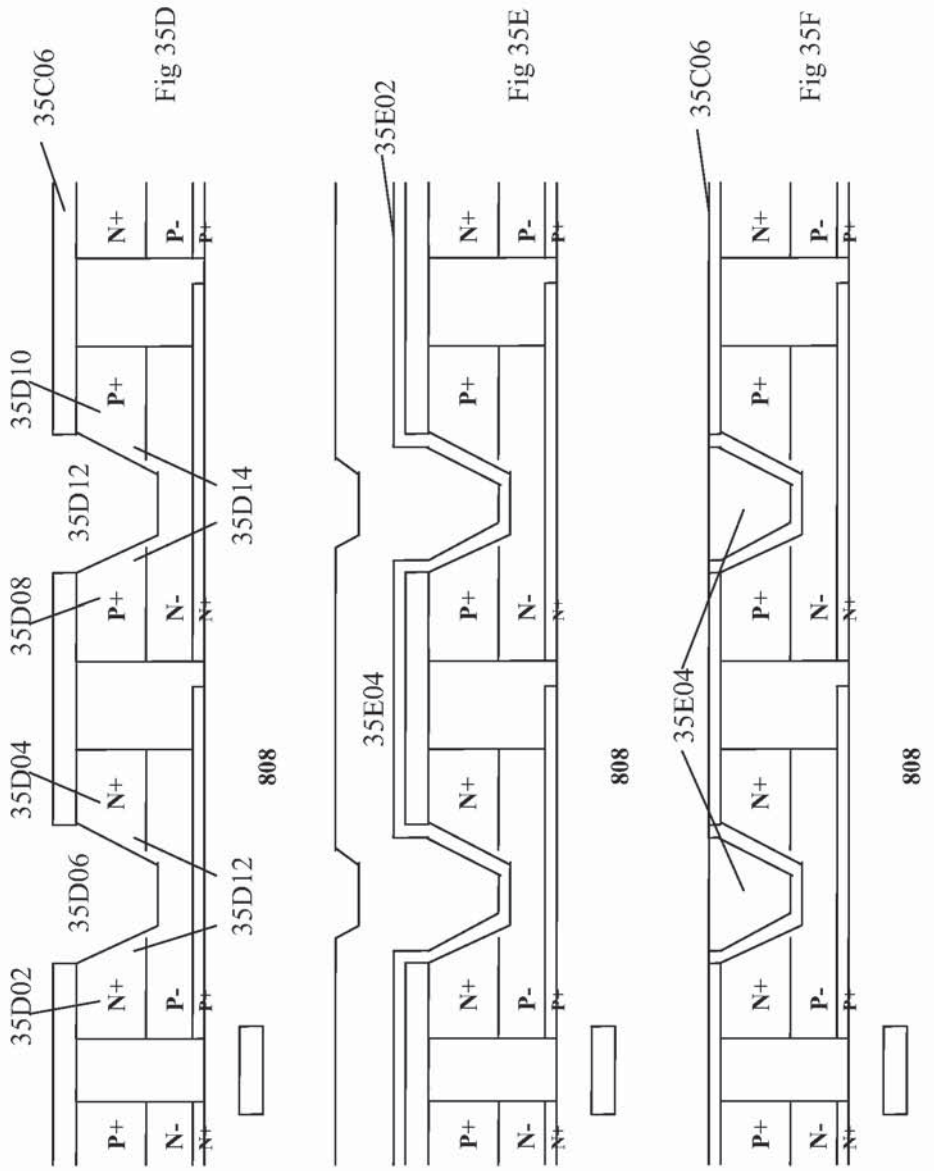
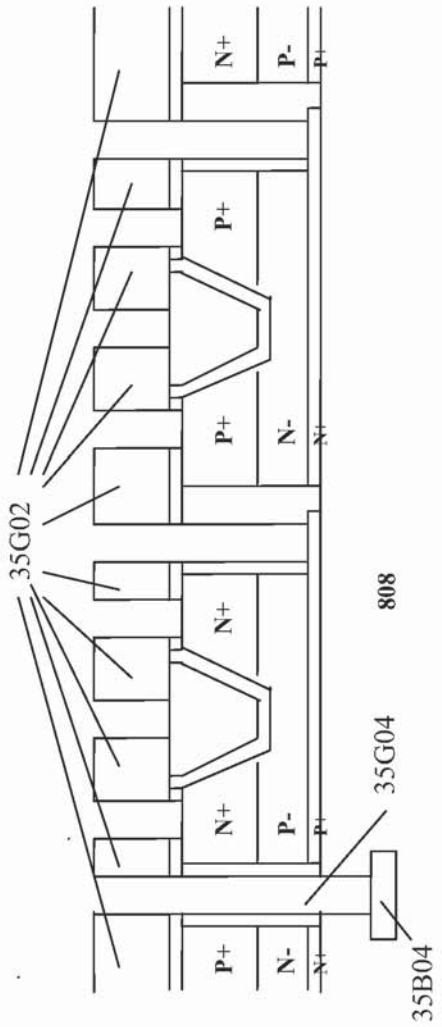

35C06
35D10
35D12
35D14
35D08
35D04
35D06
35D12
35D02
P+
N-
N+
P-
808
Fig 35D
35E02
35E04
Fig 35E
35C06
35E04
Fig 35F

Fig 35G



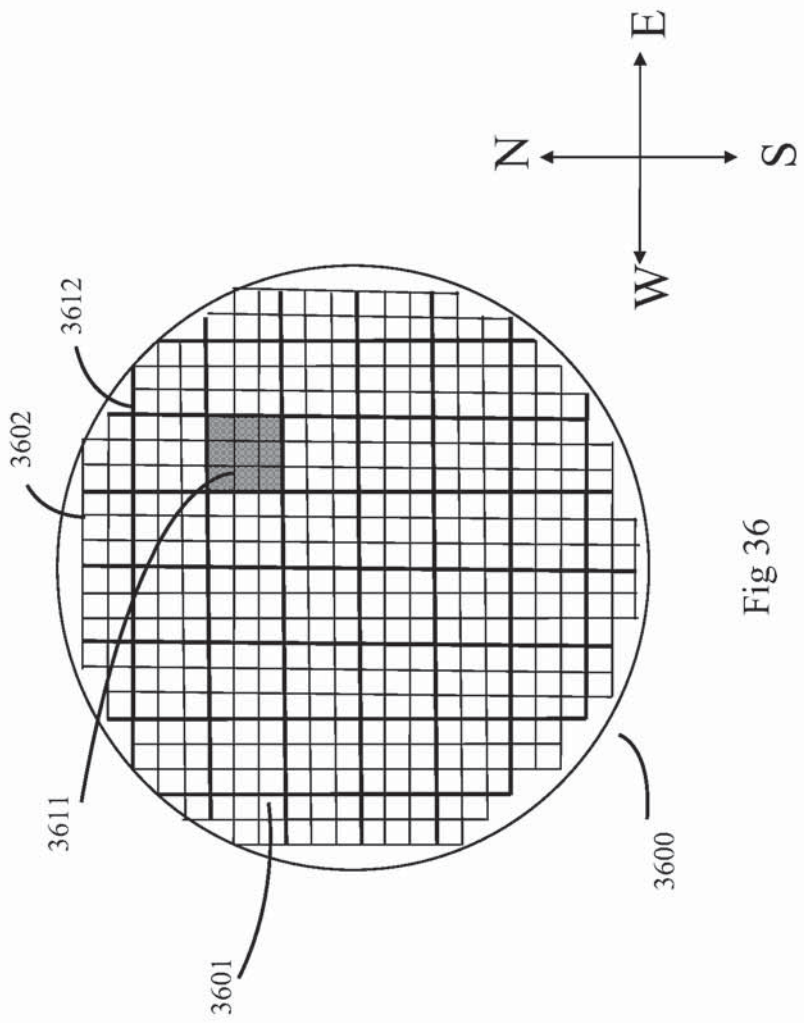


Fig 36

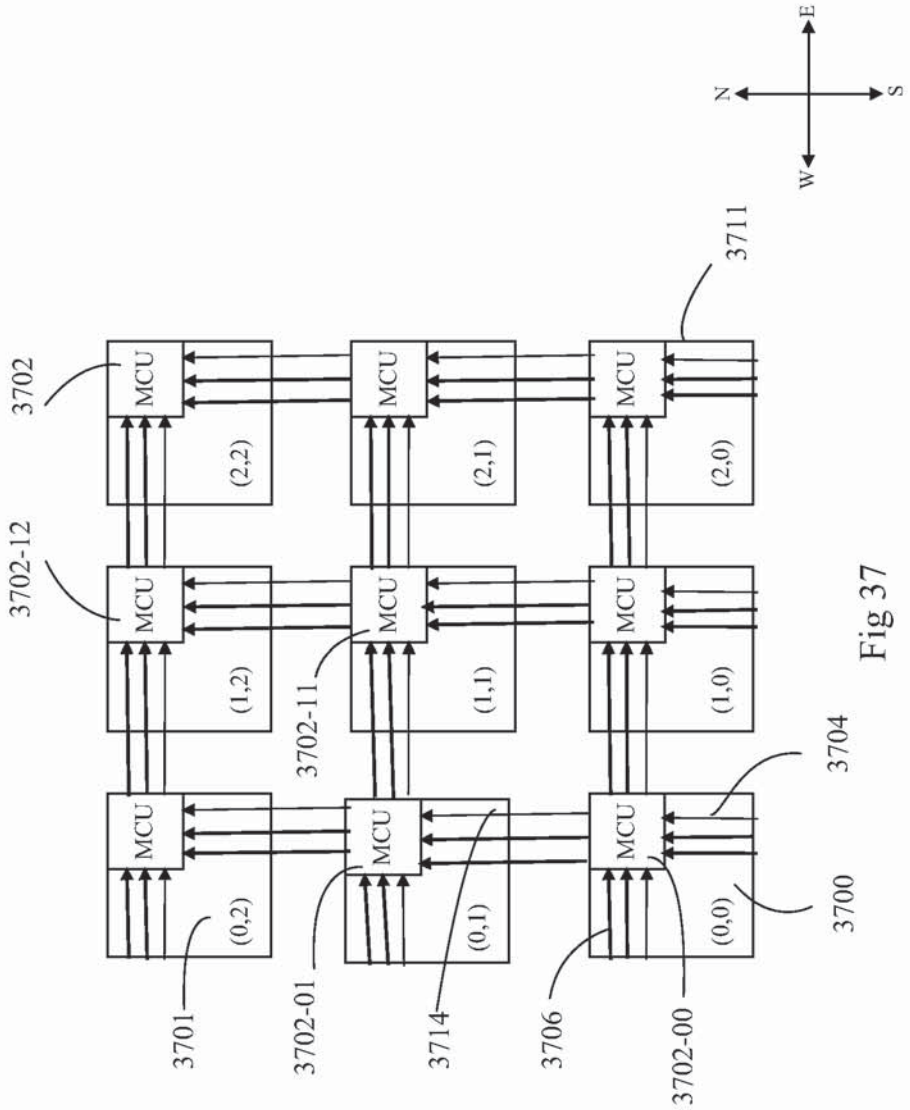
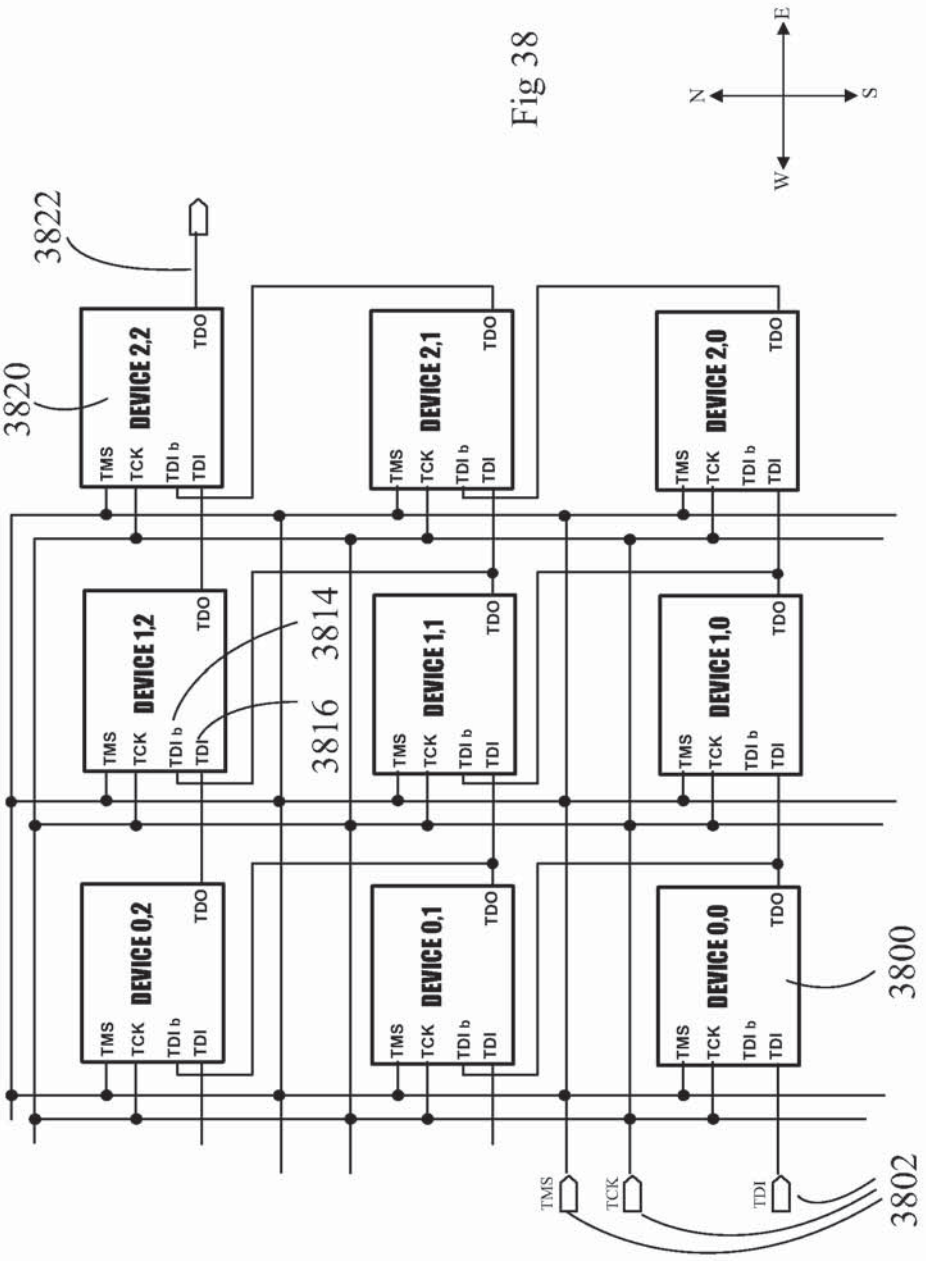

E
N
S
W
3711
3702
3702-12
3702-11
3704
3700
3701
3702-01
3714
3706
3702-00
MCU
(2,2)
(2,1)
(2,0)
(1,2)
(1,1)
(1,0)
(0,2)
(0,1)
(0,0)

Fig 37

Fig 38


N
E
S
W
3822
3820
3816
3814
3800
3802
DEVICE 2,2
DEVICE 2,1
DEVICE 2,0
DEVICE 1,2
DEVICE 1,1
DEVICE 1,0
DEVICE 0,2
DEVICE 0,1
DEVICE 0,0
TMS
TCK
TDI b
TDI
TDO

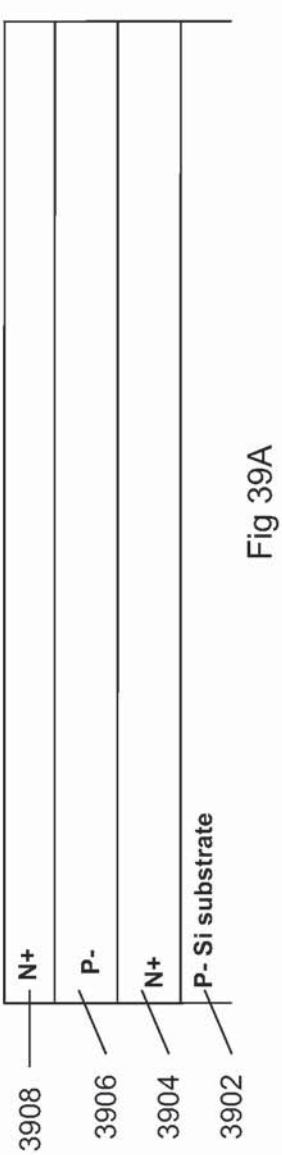


Fig 39A

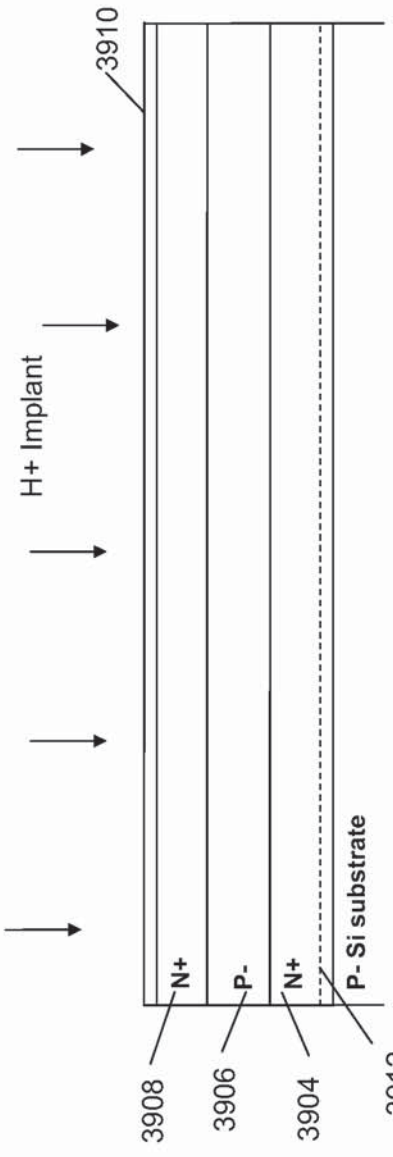


Fig 39B

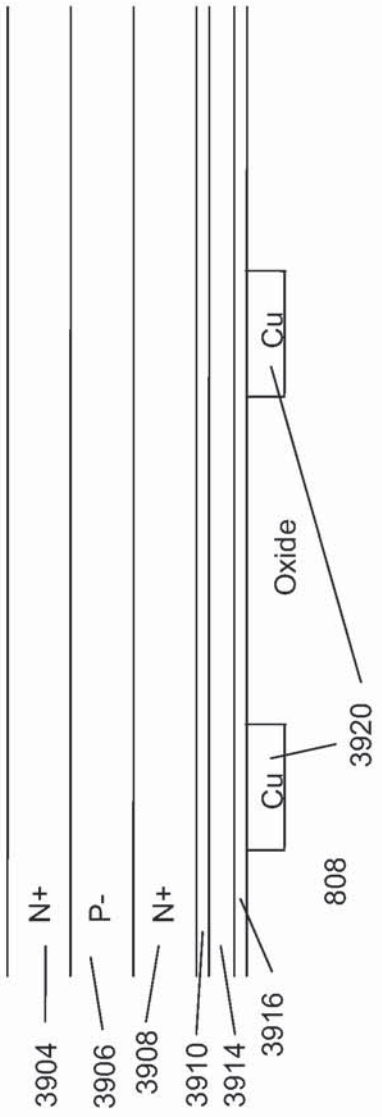


Fig 39C



Fig 40A

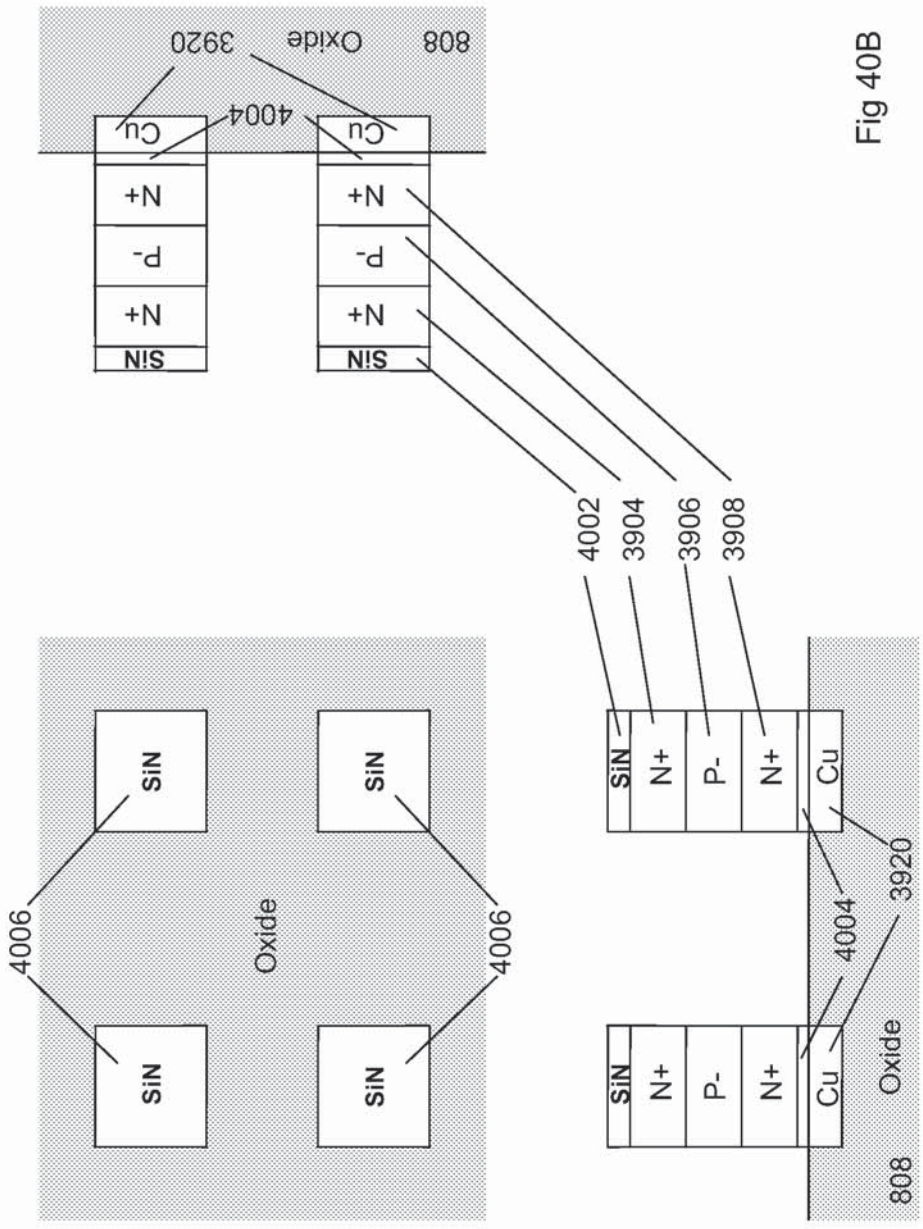

808
Oxide
3920
4004
Cu
Cu
N+
P-
N+
SiN
SiN
N+
P-
N+
Cu
4002
3904
3906
3908
SiN
SiN
SiN
SiN
4006
4006
Oxide
SiN
N+
P-
N+
Cu
Oxide
808
4004
3920

Fig 40B

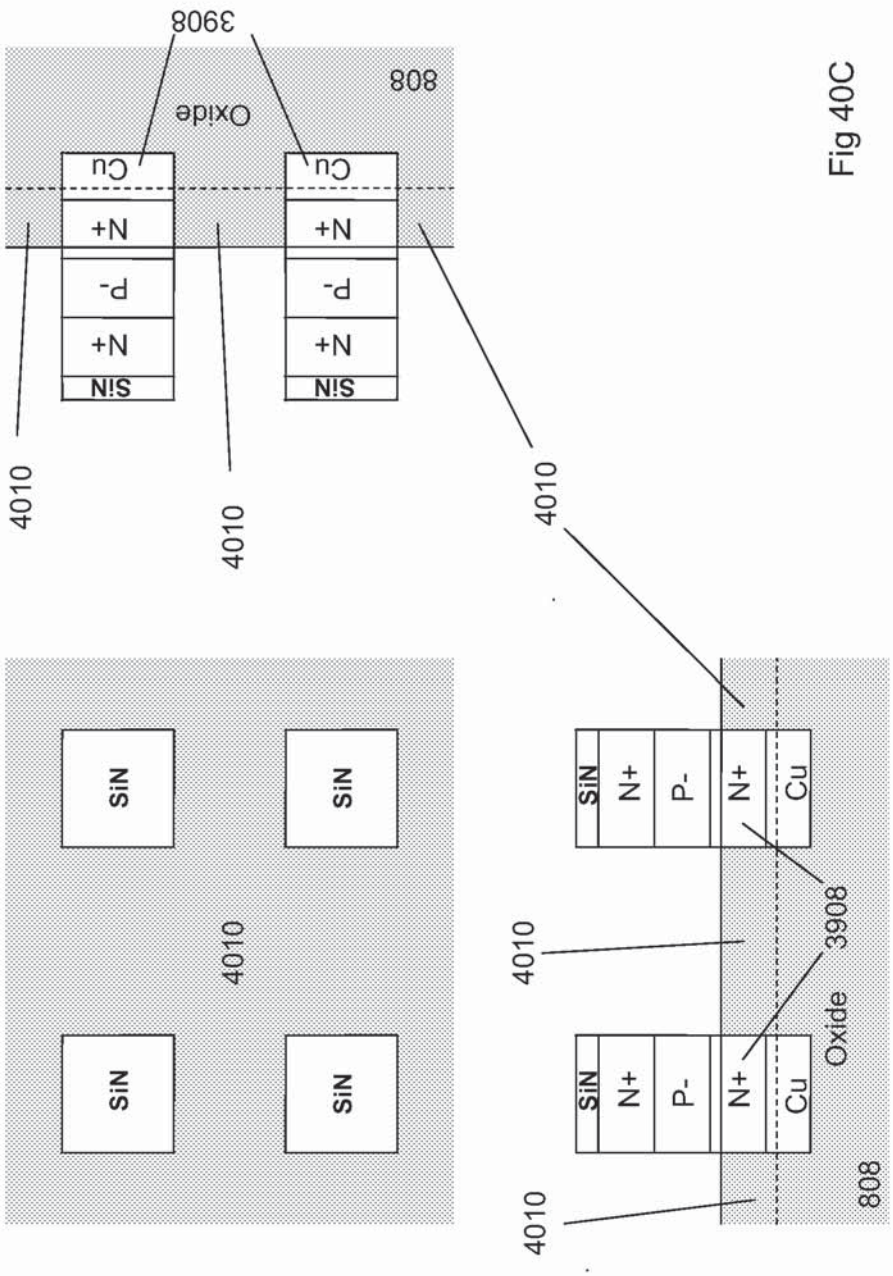


Fig 40C

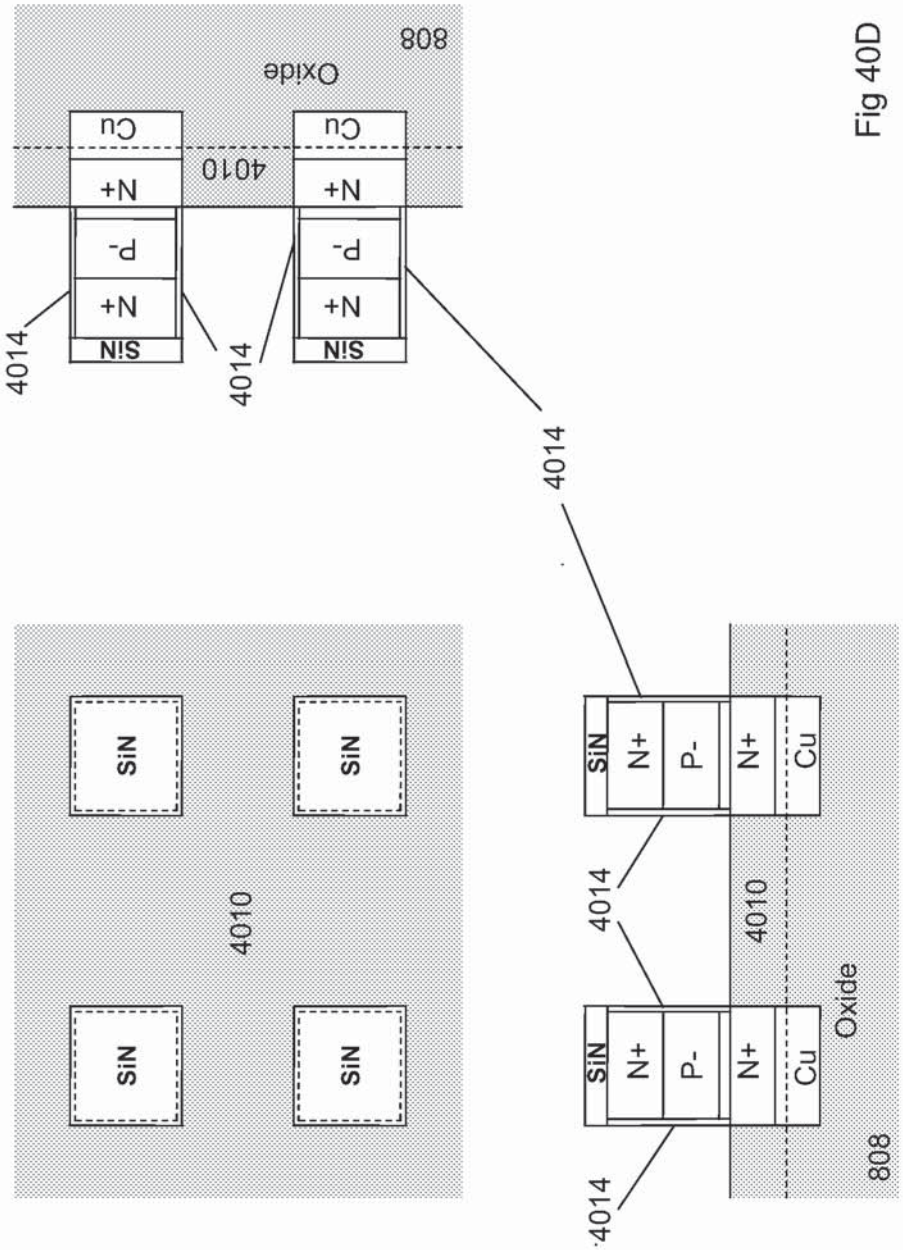


Fig 40D

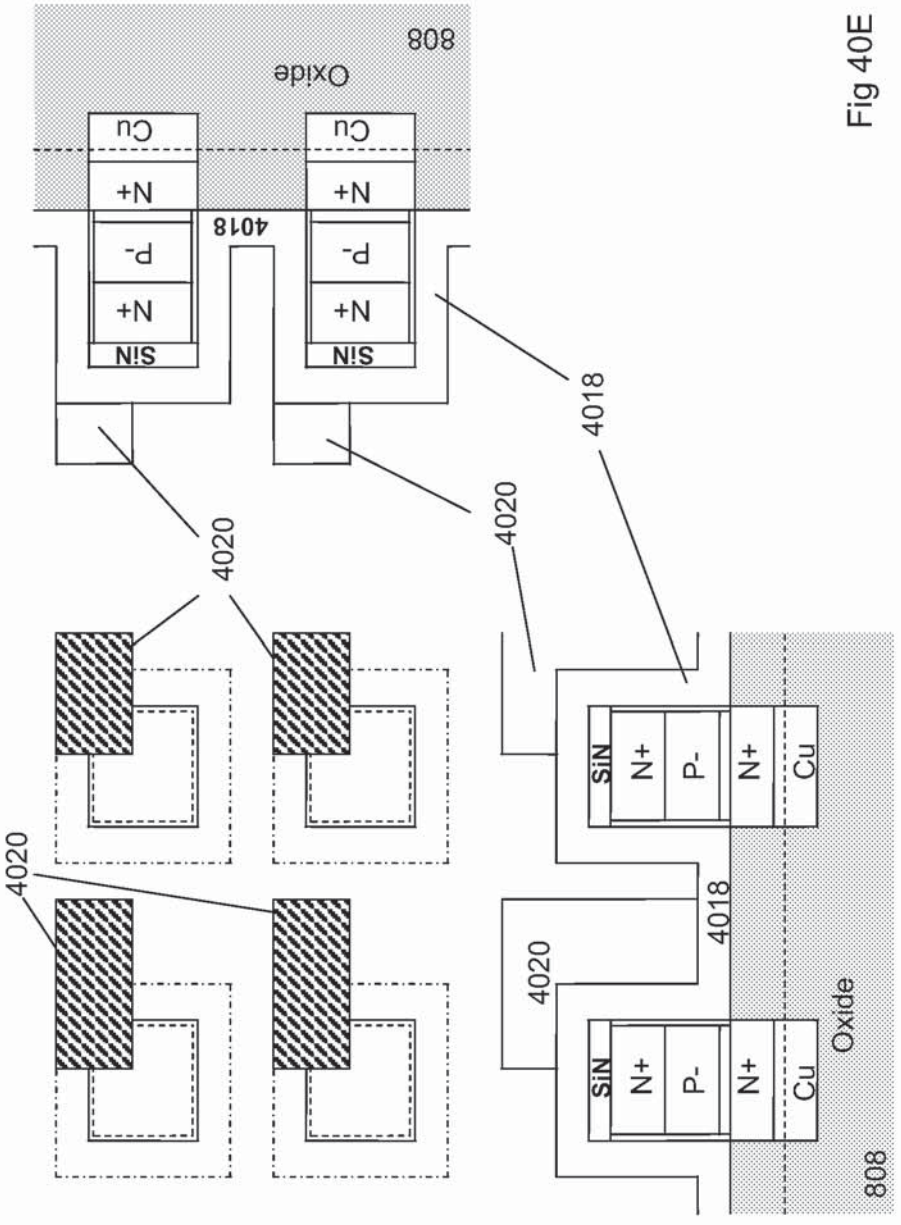


Fig 40E

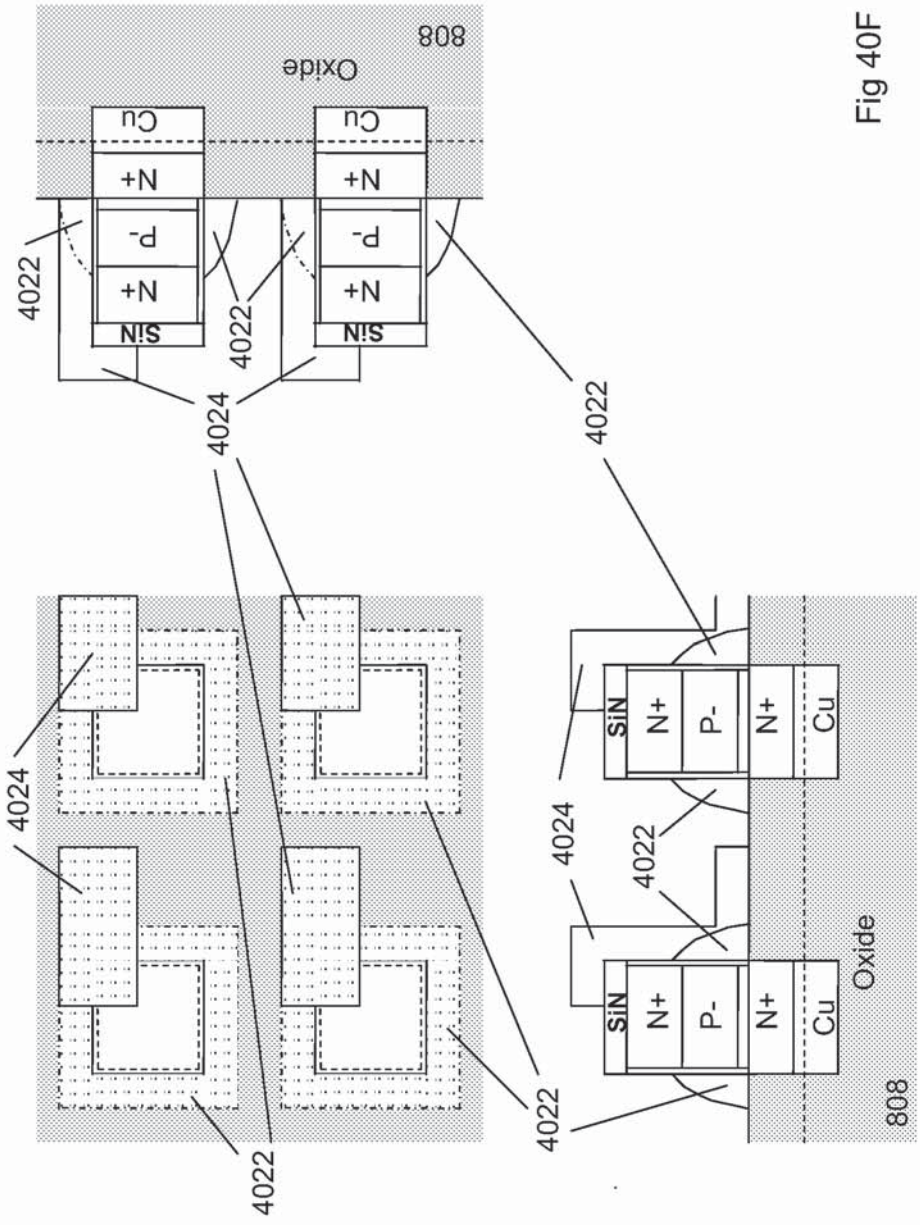

808
Oxide
Cu
N+
P-
N+
SiN
4022
4024
4022
4024
4022
4024
4022
SiN
N+
P-
N+
Cu
Oxide
808

Fig 40F

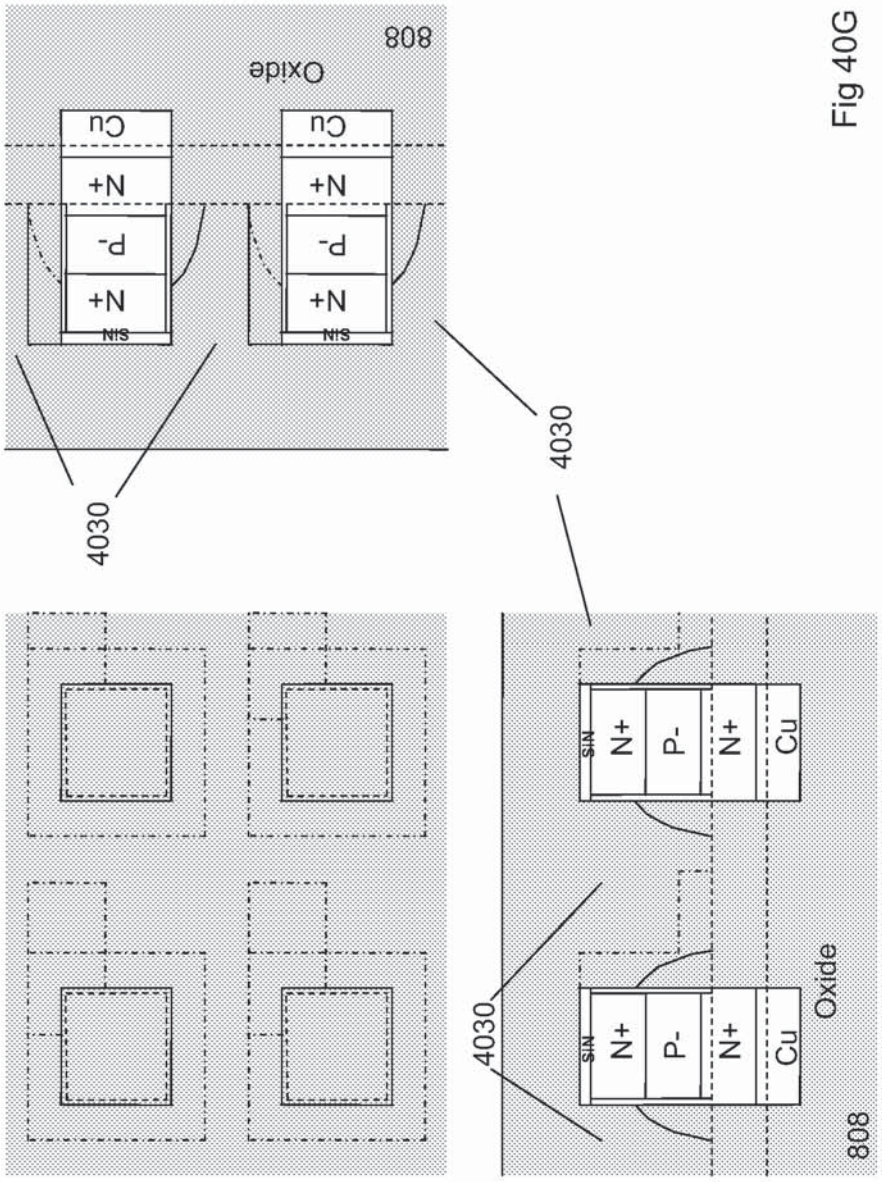


Fig 40G

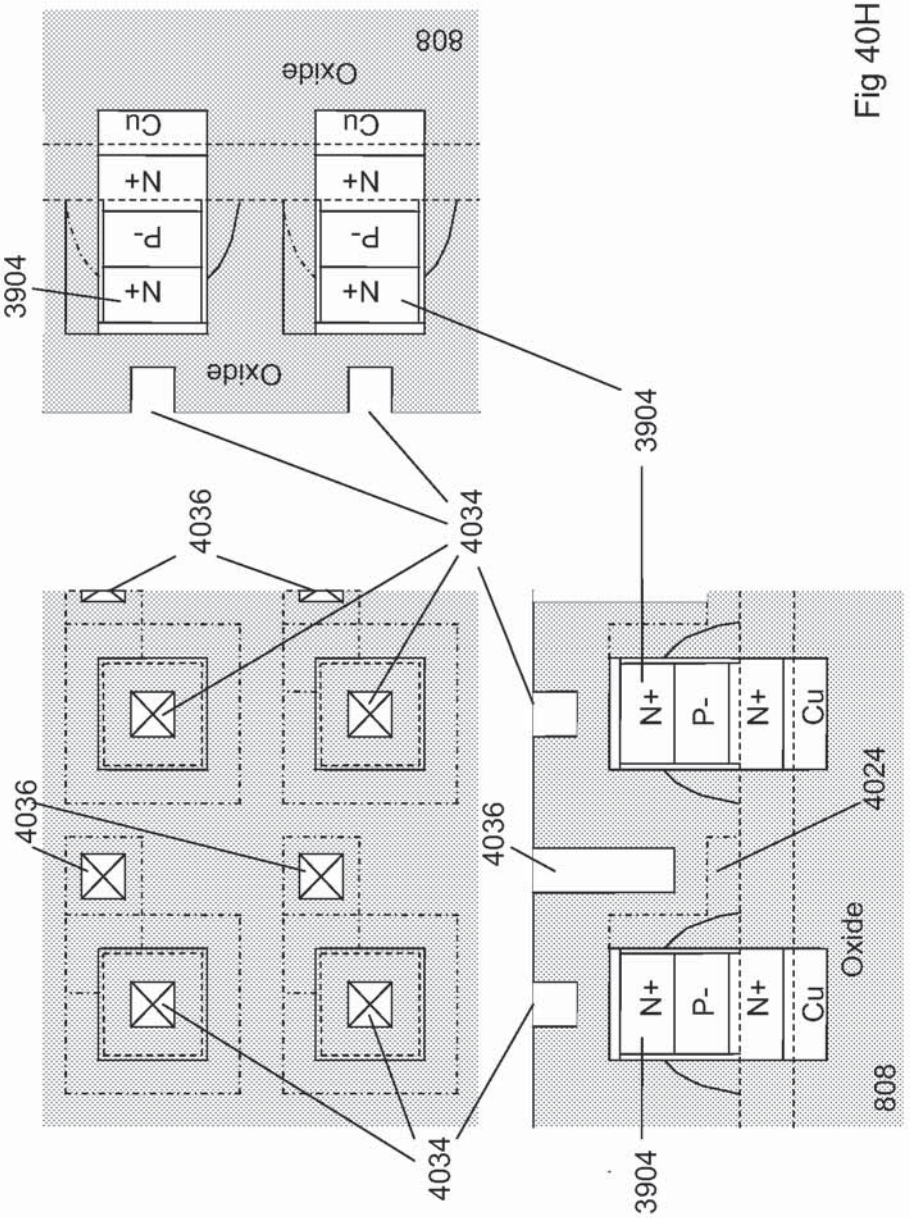

808
Oxide
Cu
N+
P-
N+
3904
Oxide
4034
4036
3904
N+
P-
N+
Cu
4024
4036
Oxide
808
4034
3904

Fig 40H

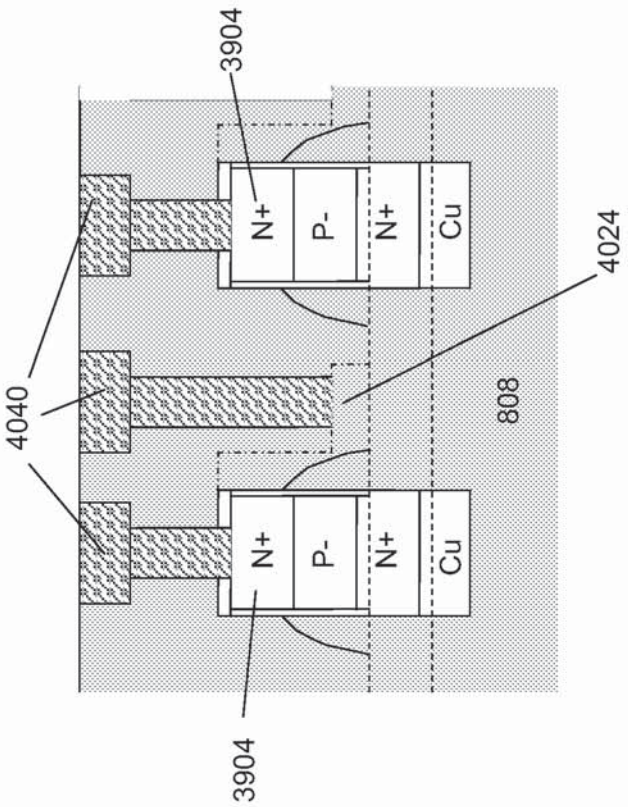


Fig 40I

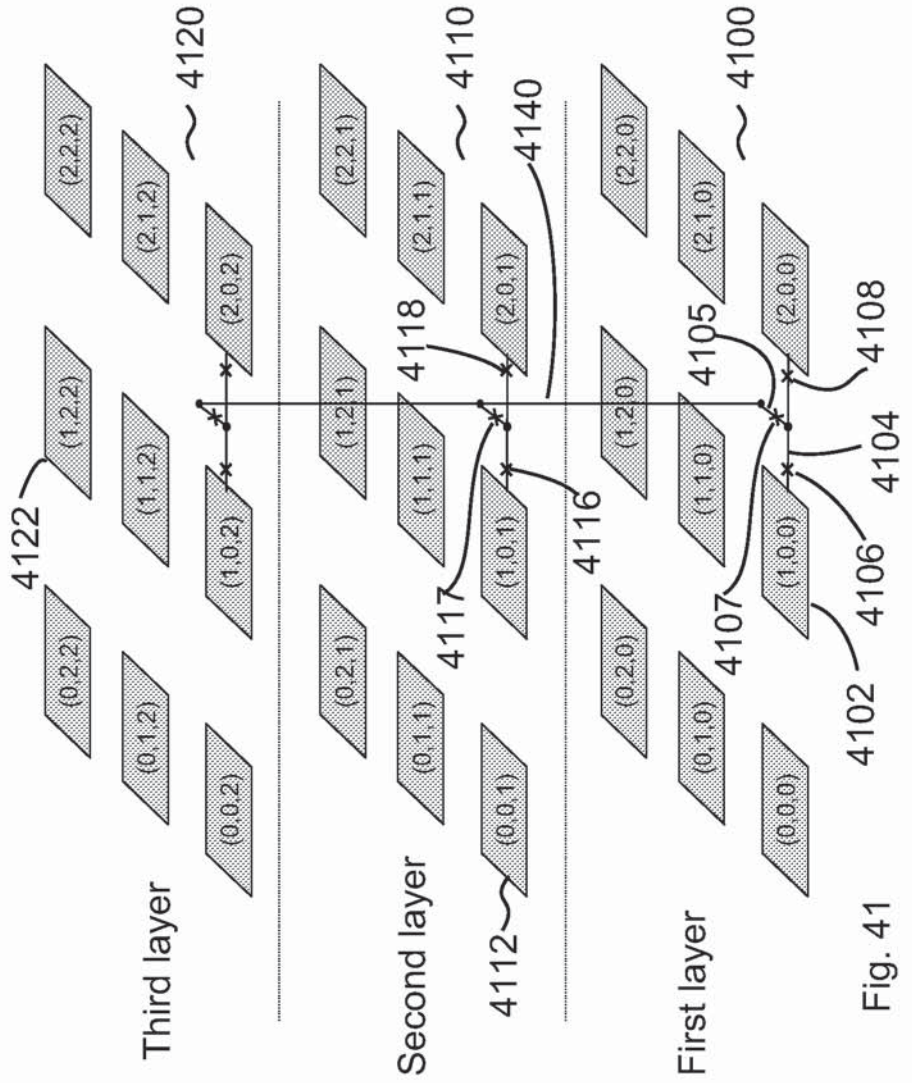

Third layer
Second layer
First layer
(0,0,2)
(0,1,2)
(0,2,2)
(1,0,2)
(1,1,2)
(1,2,2)
(2,0,2)
(2,1,2)
(2,2,2)
(0,0,1)
(0,1,1)
(0,2,1)
(1,0,1)
(1,1,1)
(1,2,1)
(2,0,1)
(2,1,1)
(2,2,1)
(0,0,0)
(0,1,0)
(0,2,0)
(1,0,0)
(1,1,0)
(1,2,0)
(2,0,0)
(2,1,0)
(2,2,0)
4100
4102
4104
4105
4106
4107
4108
4110
4112
4116
4117
4118
4120
4122
4140

Fig. 41

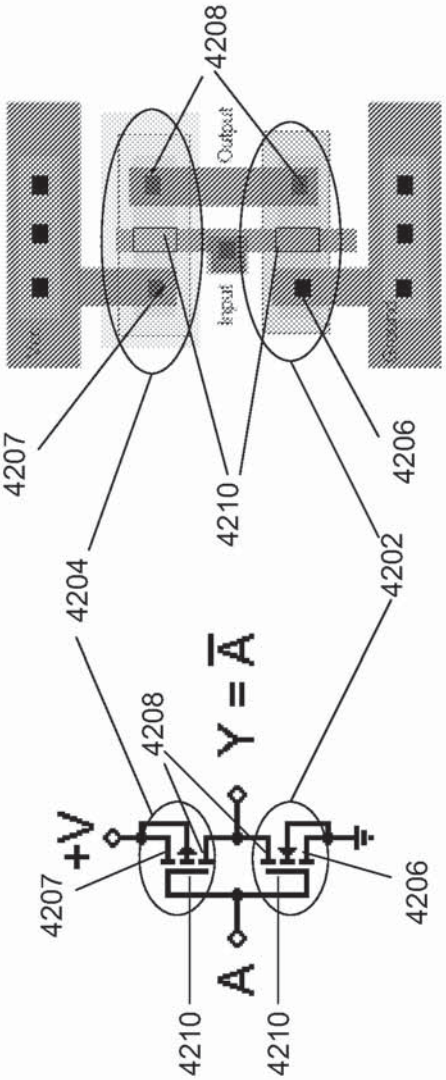

4208
Output
Input
4207
4210
4206
4204
4202
Y = $\overline{A}$
4208
+V
4207
4206
A
4210
4210

Fig 42

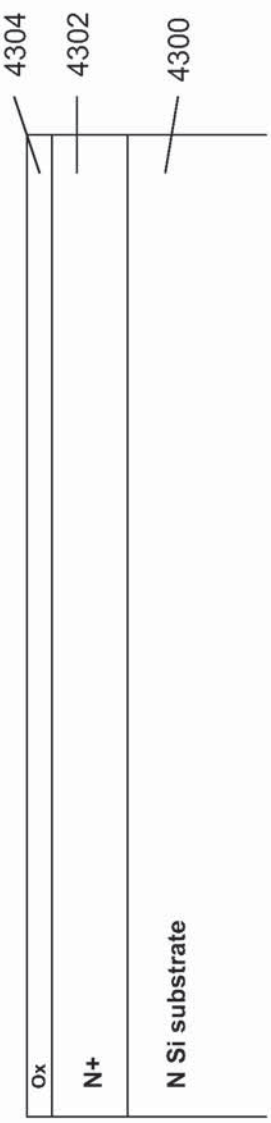


Fig 43A

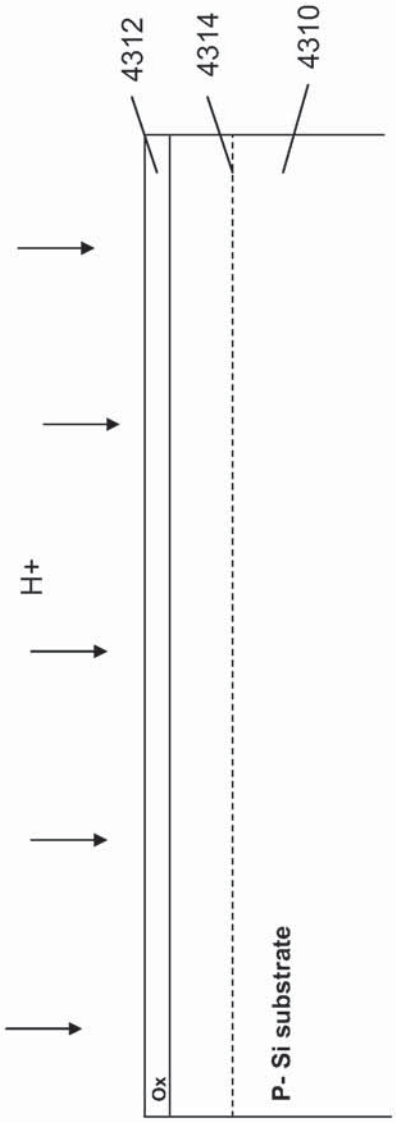


Fig 43B

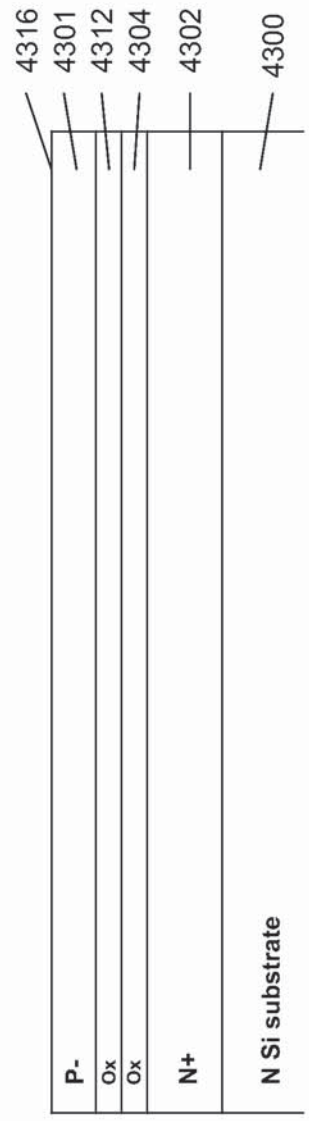


Fig 43C

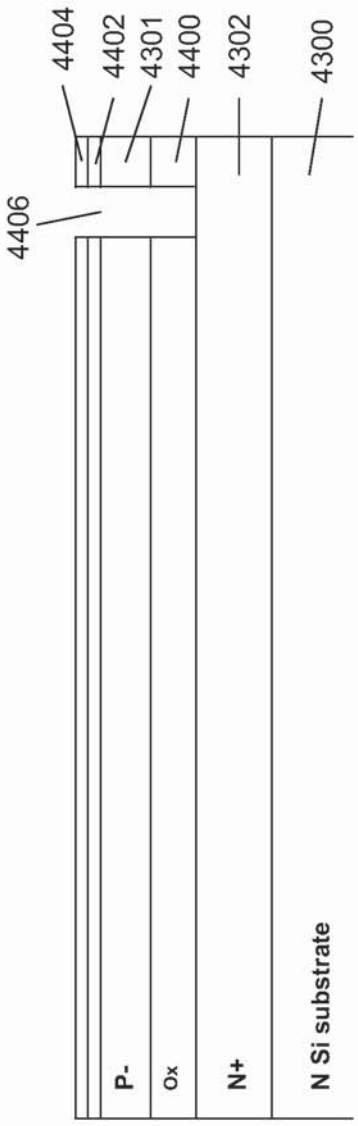


Fig 44A

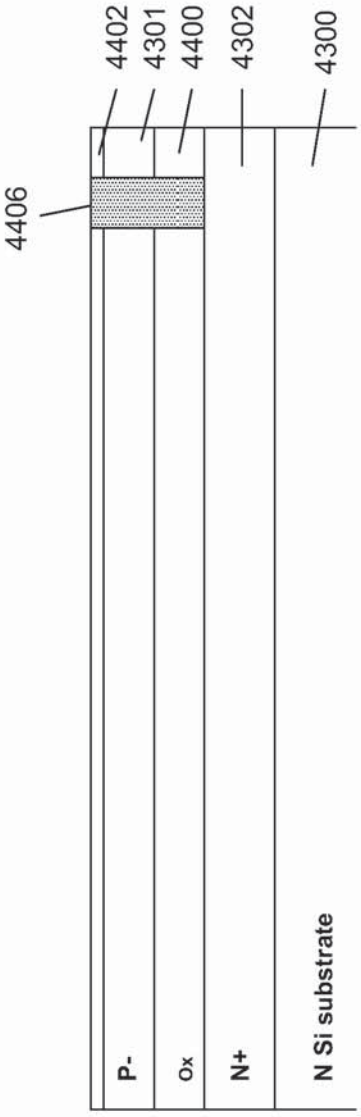


Fig 44B

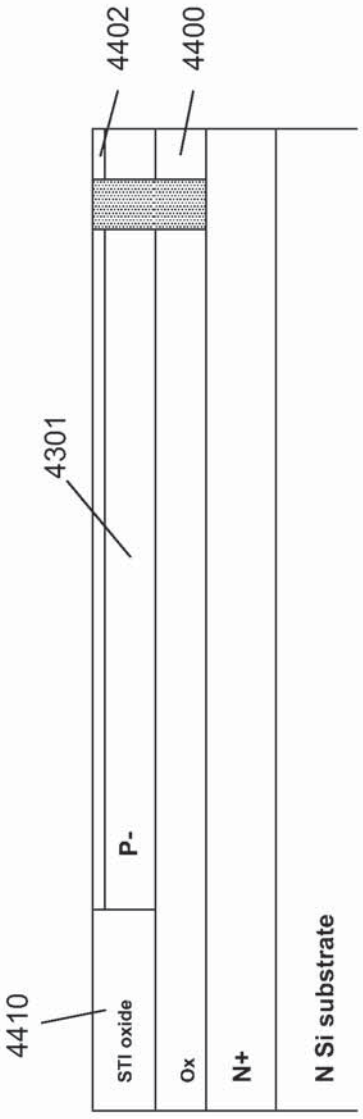


Fig 44C

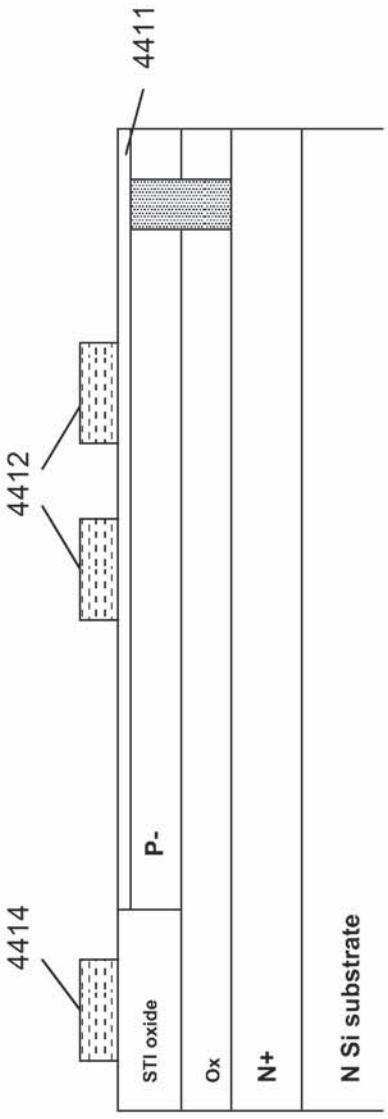


Fig 44D

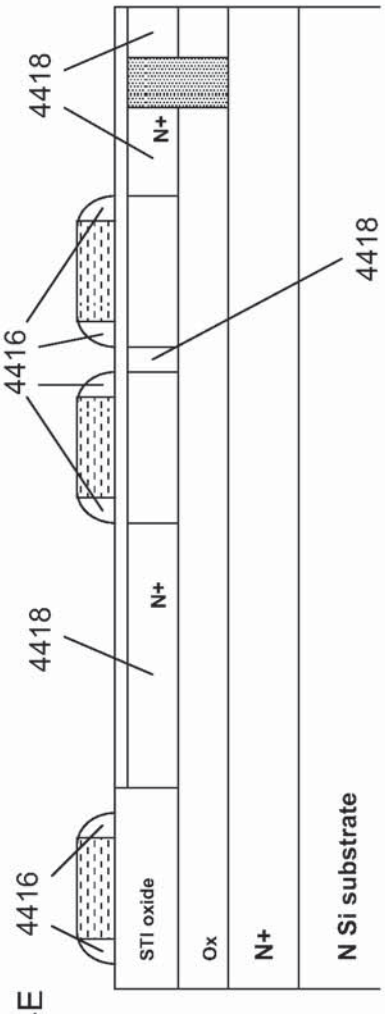


Fig 44E

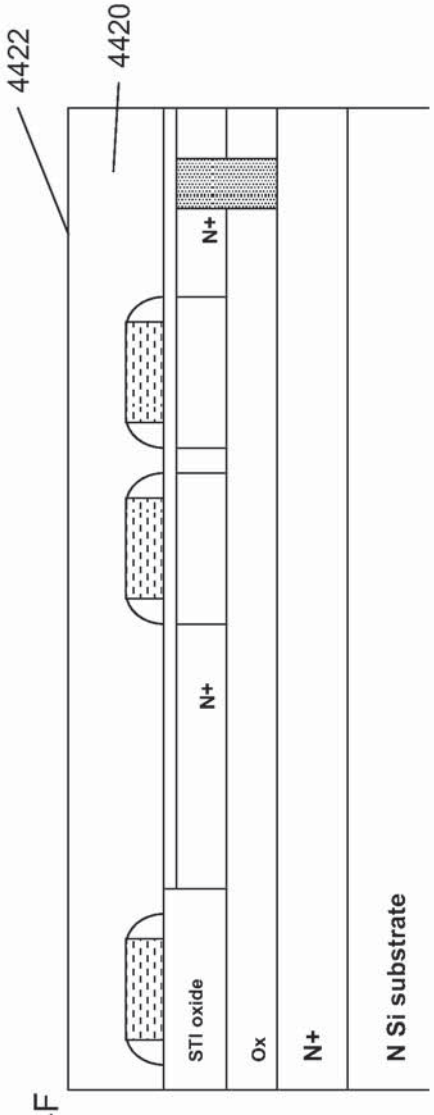


Fig 44F

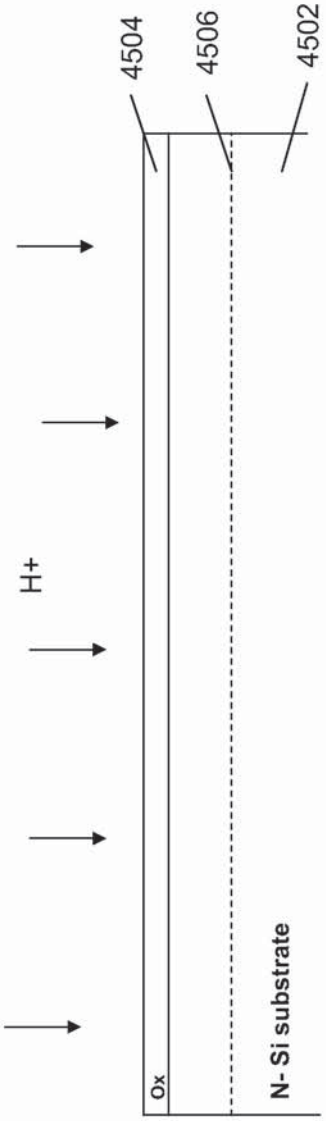


Fig 45A

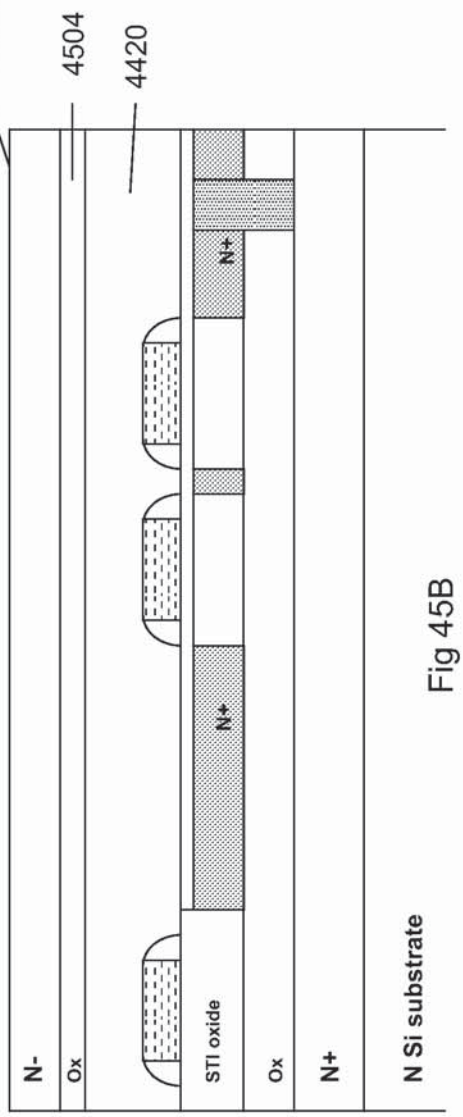


Fig 45B

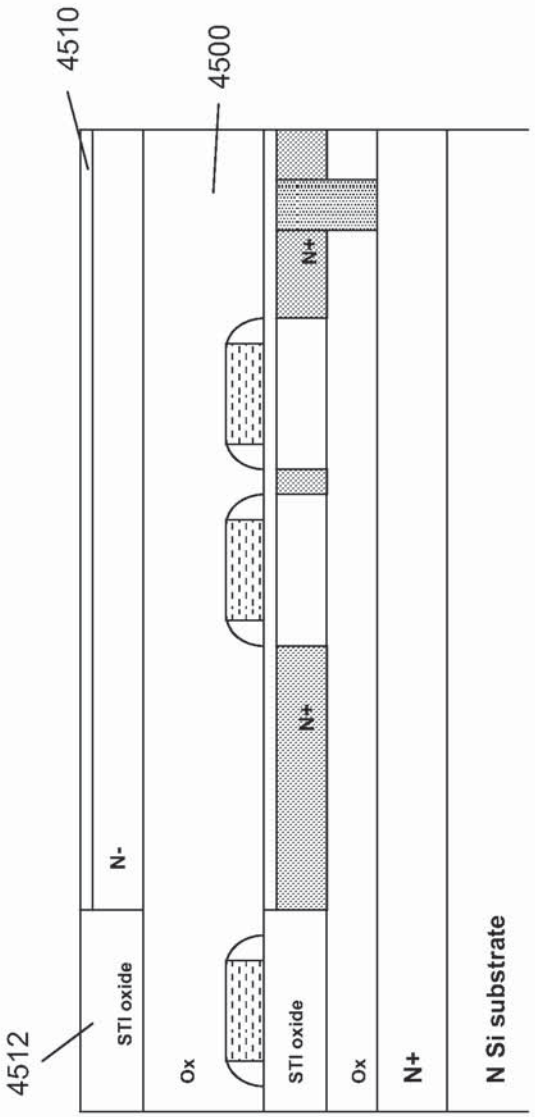


Fig 45C

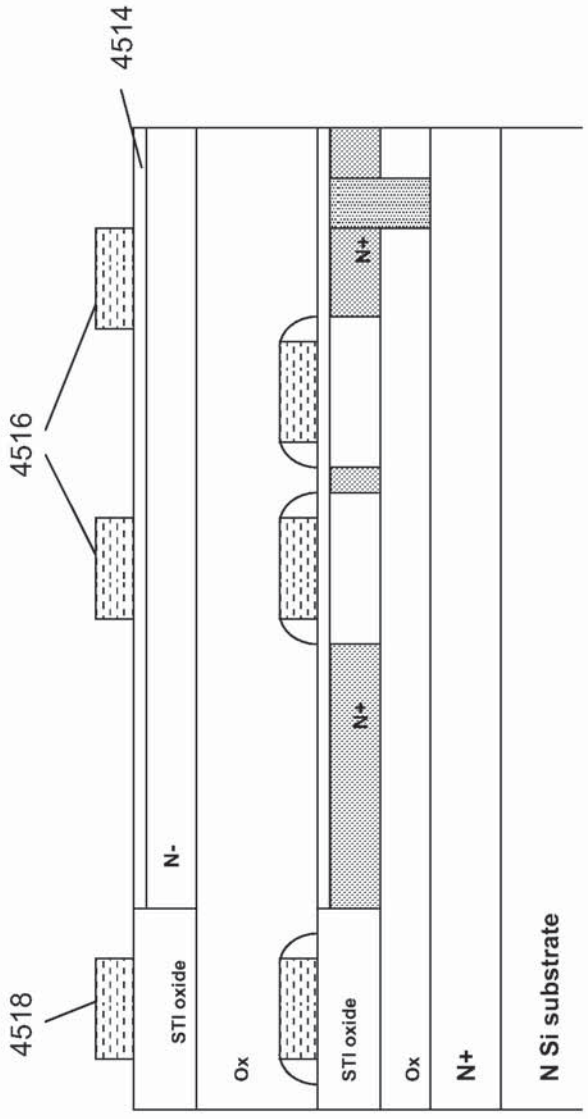


Fig 45D

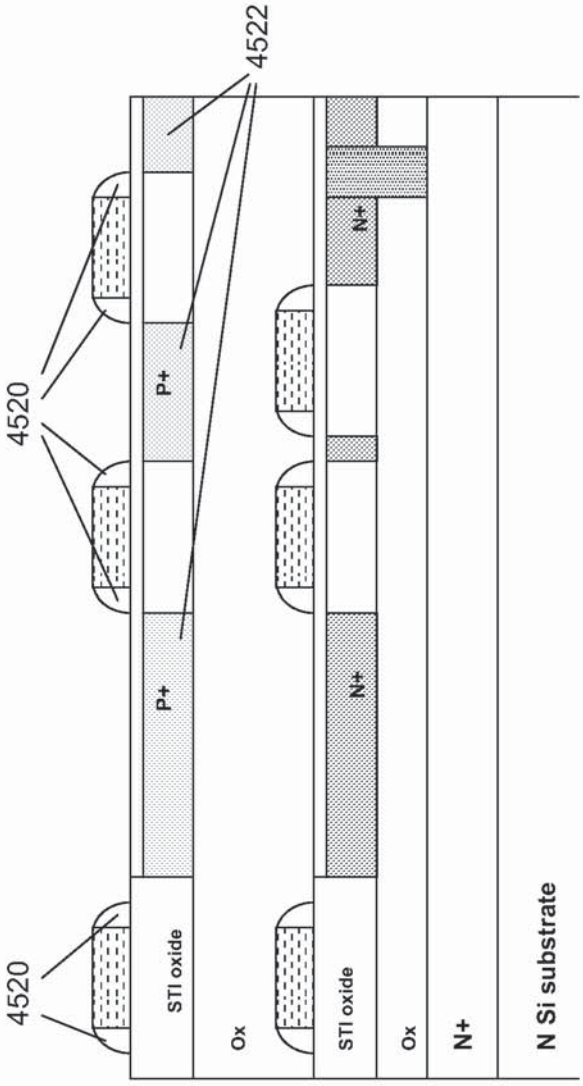


Fig 45E

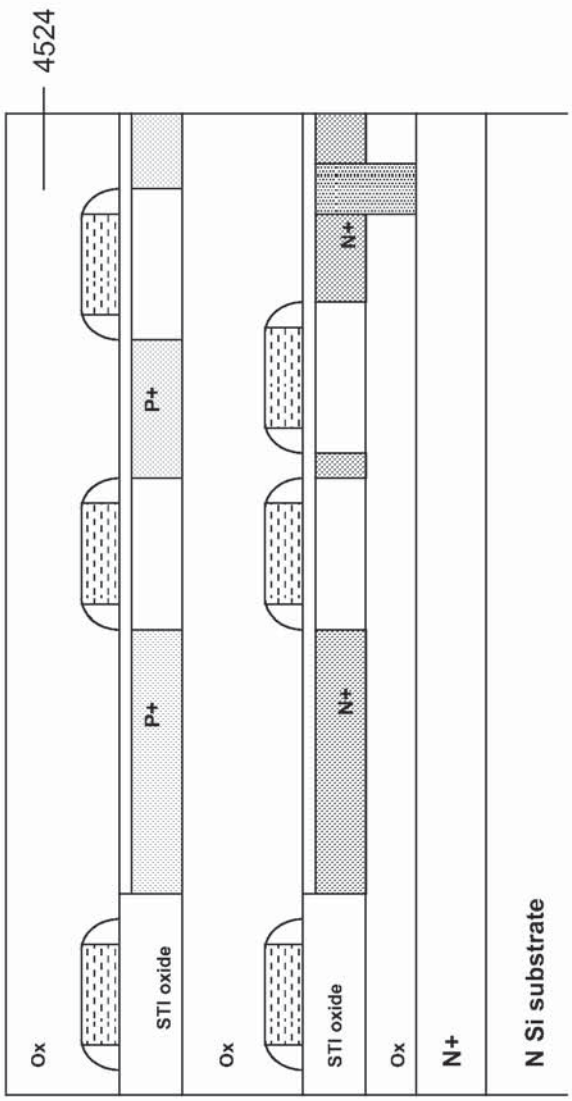


Fig 45F

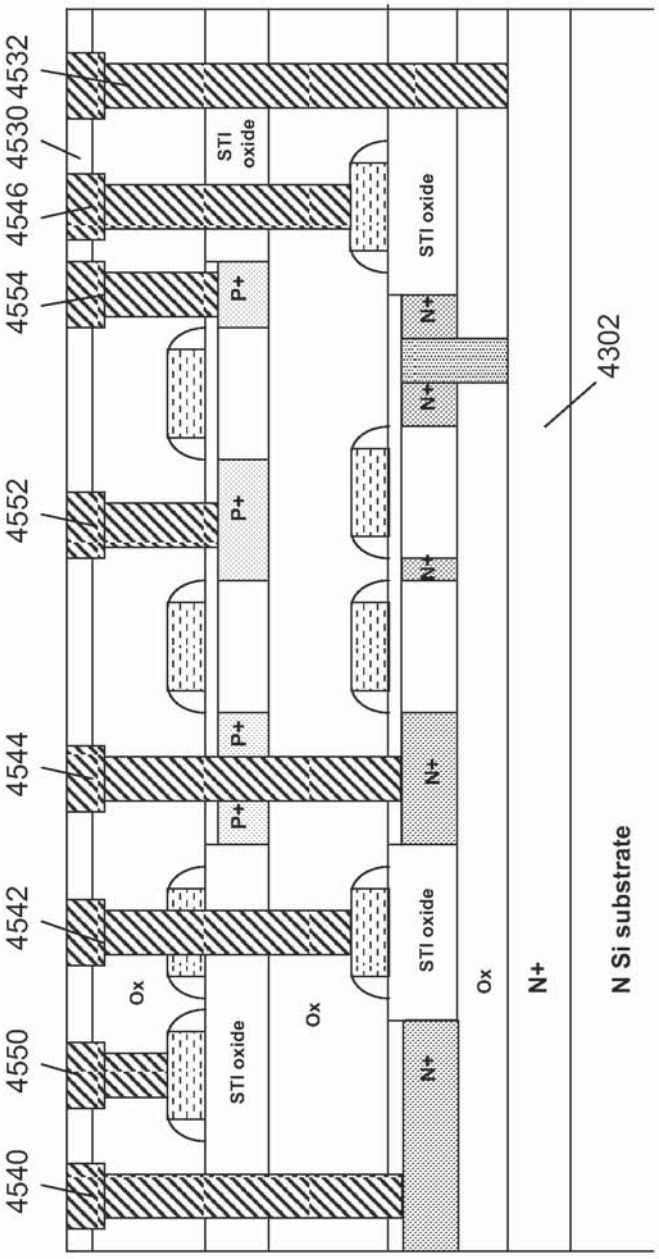

4532
4530
4546
4554
4552
4544
4542
4550
4540
STI oxide
STI oxide
P+
P+
P+
P+
N+
N+
N+
N+
Ox
Ox
STI oxide
STI oxide
Ox
N+
N Si substrate
4302

Fig 45G

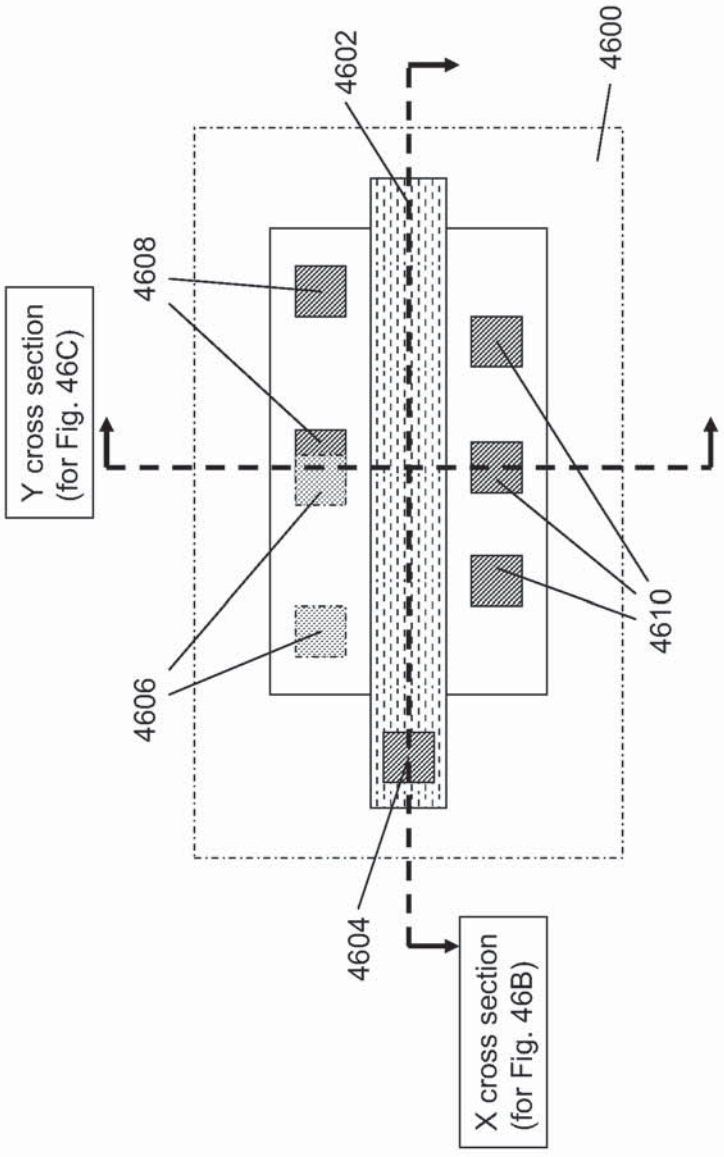

4600
4602
4608
4606
4610
4604
Y cross section
(for Fig. 46C)
X cross section
(for Fig. 46B)

Fig 46A

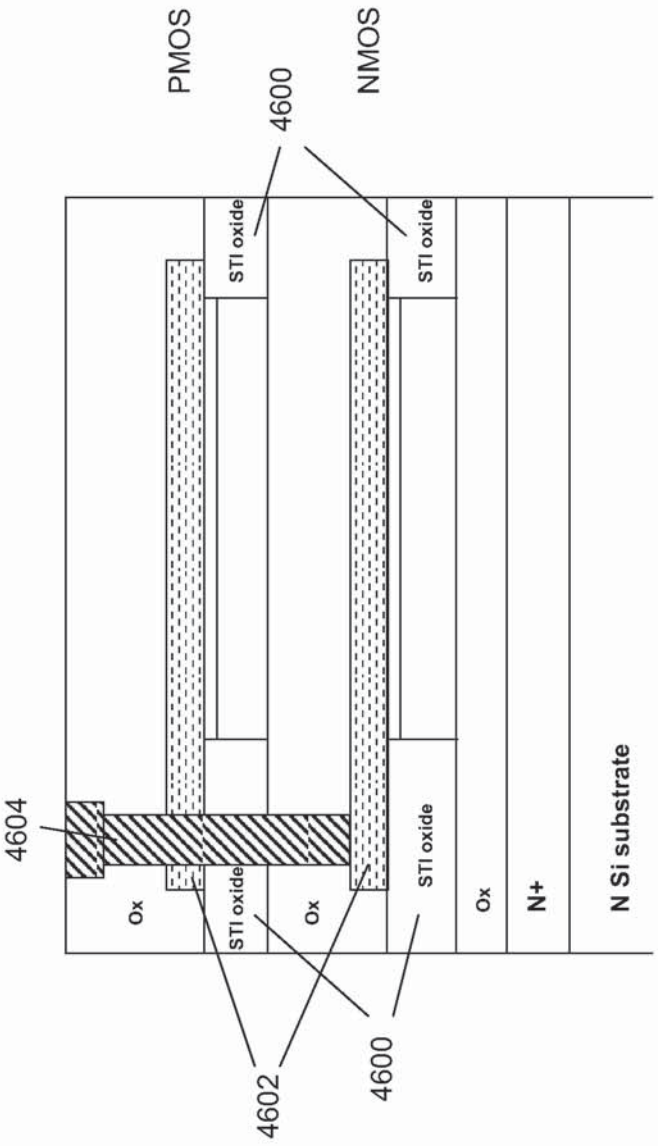

PMOS
NMOS
4600
STI oxide
STI oxide
4604
Ox
STI oxide
Ox
STI oxide
Ox
N+
N Si substrate
4602
4600

Fig 46B

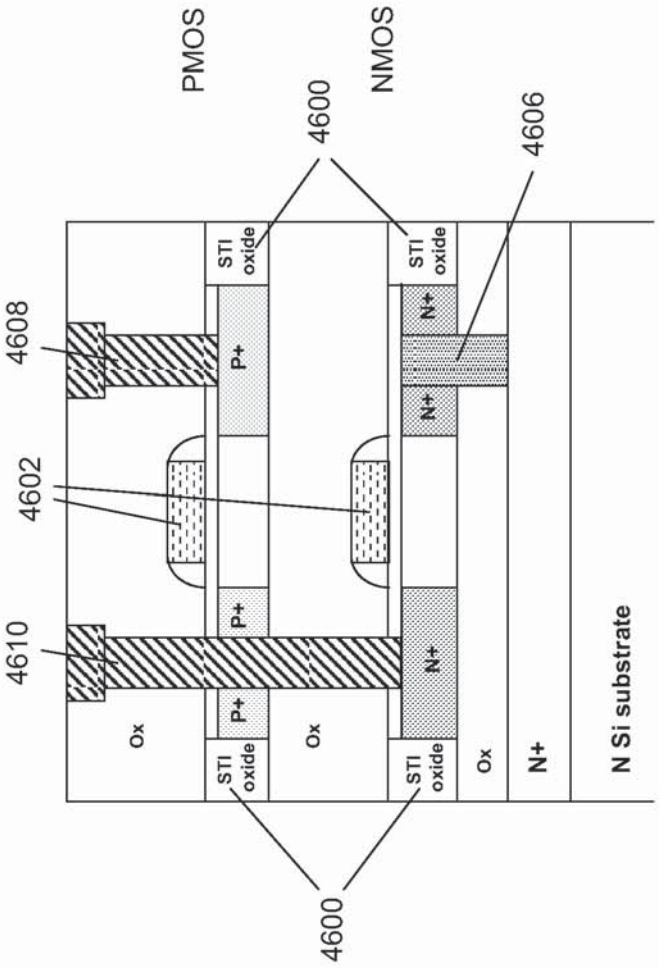

PMOS
NMOS
4600
4606
4608
4602
4610
4600
STI oxide
STI oxide
P+
N+
N+
P+
P+
N+
Ox
Ox
Ox
STI oxide
STI oxide
N+
N Si substrate

Fig 46C

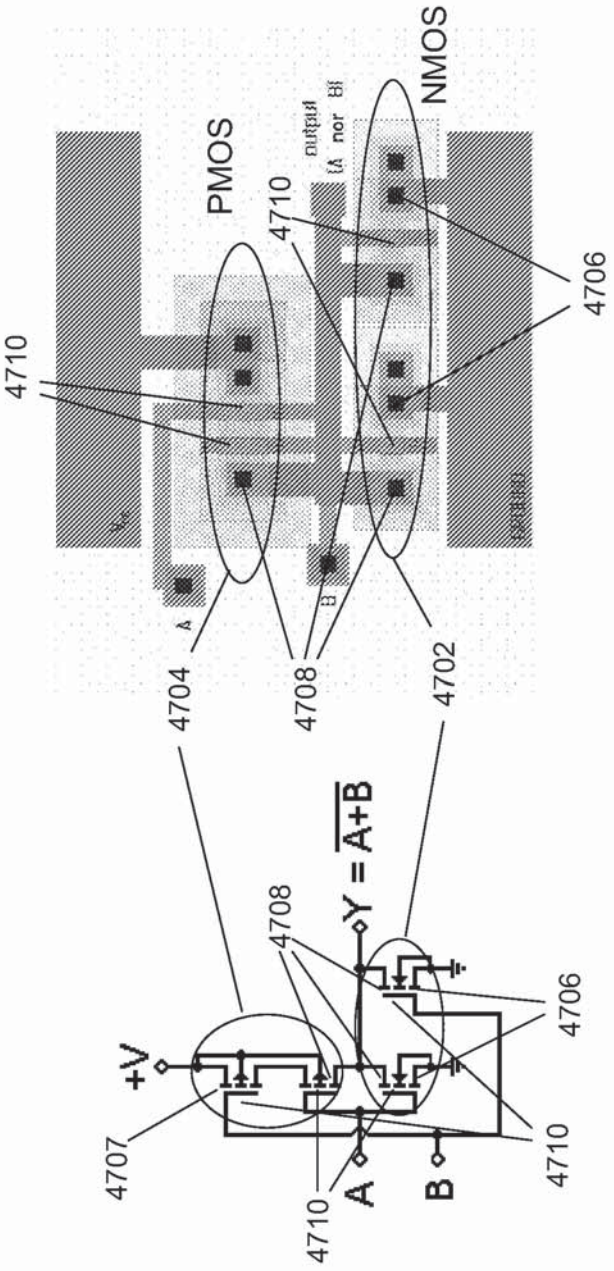


Fig 47

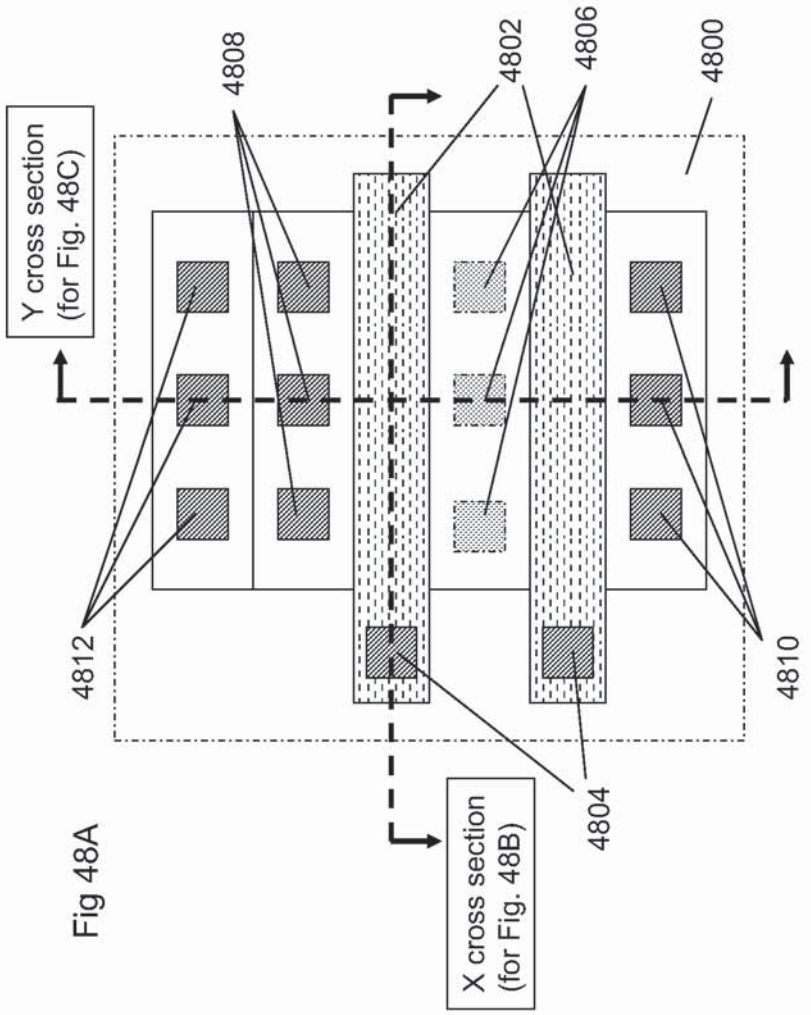

Y cross section
(for Fig. 48C)
4808
4802
4806
4800
4812
4810
4804
X cross section
(for Fig. 48B)

Fig 48A

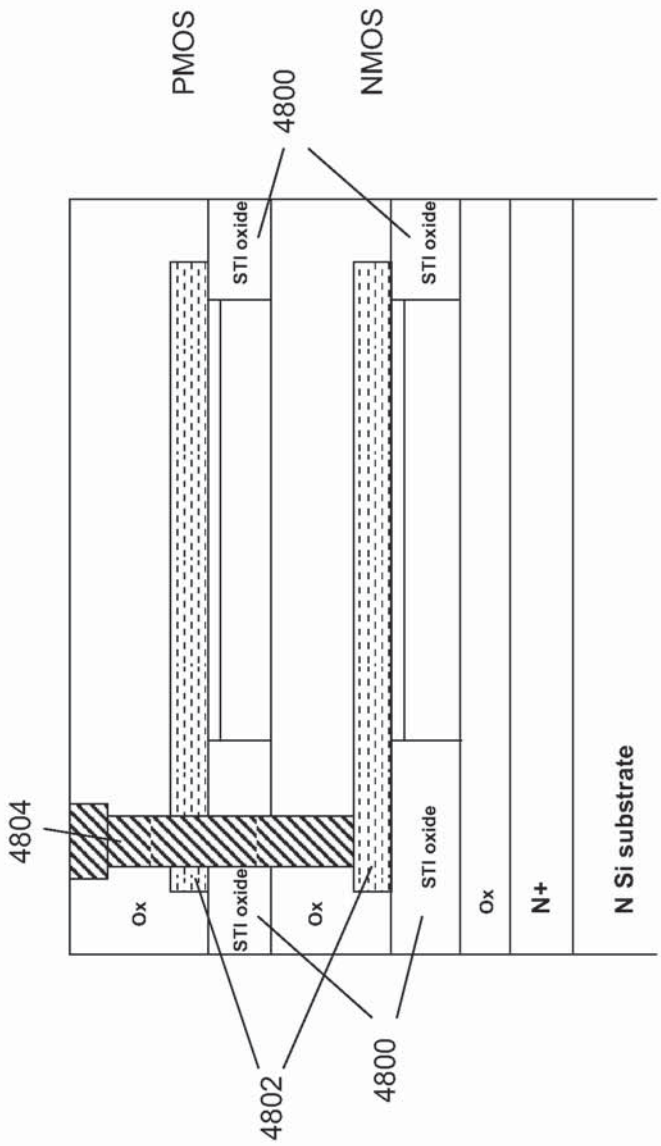

PMOS
NMOS
4800
STI oxide
STI oxide
4804
Ox
STI oxide
Ox
STI oxide
Ox
N+
N Si substrate
4802
4800

Fig 48B

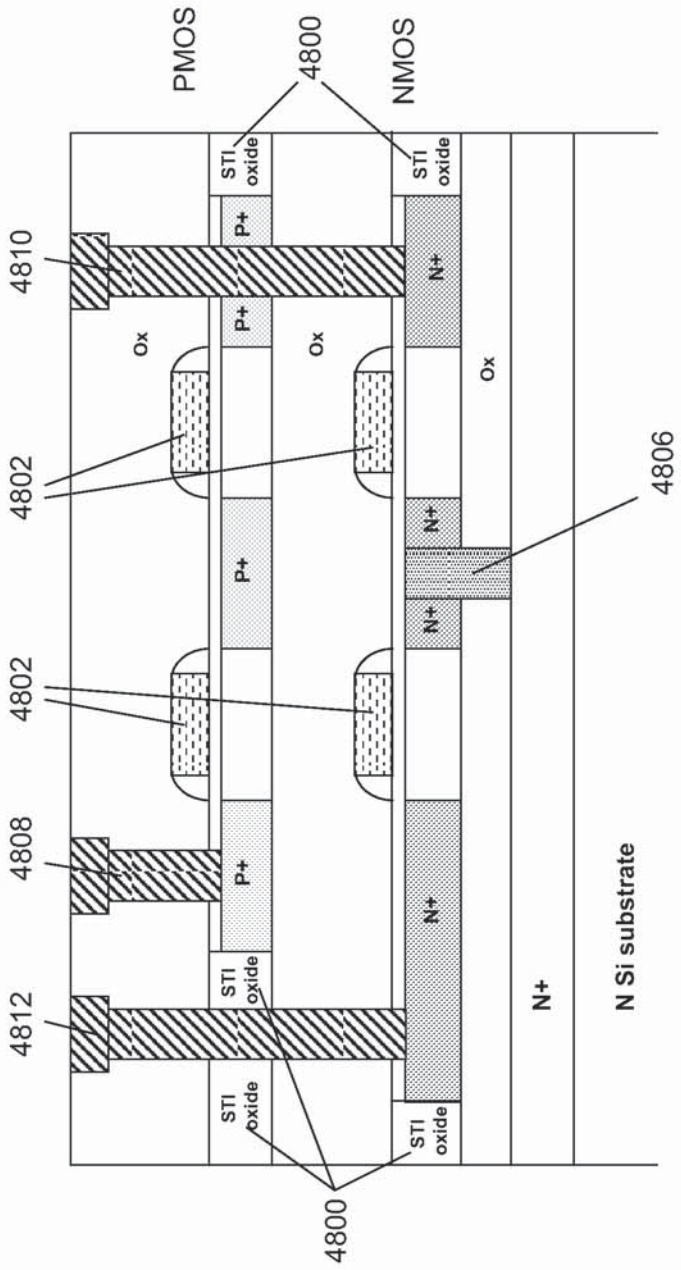

PMOS
4800
NMOS
STI oxide
P+
N+
4810
Ox
4802
4806
4808
4812
N Si substrate

Fig 48C

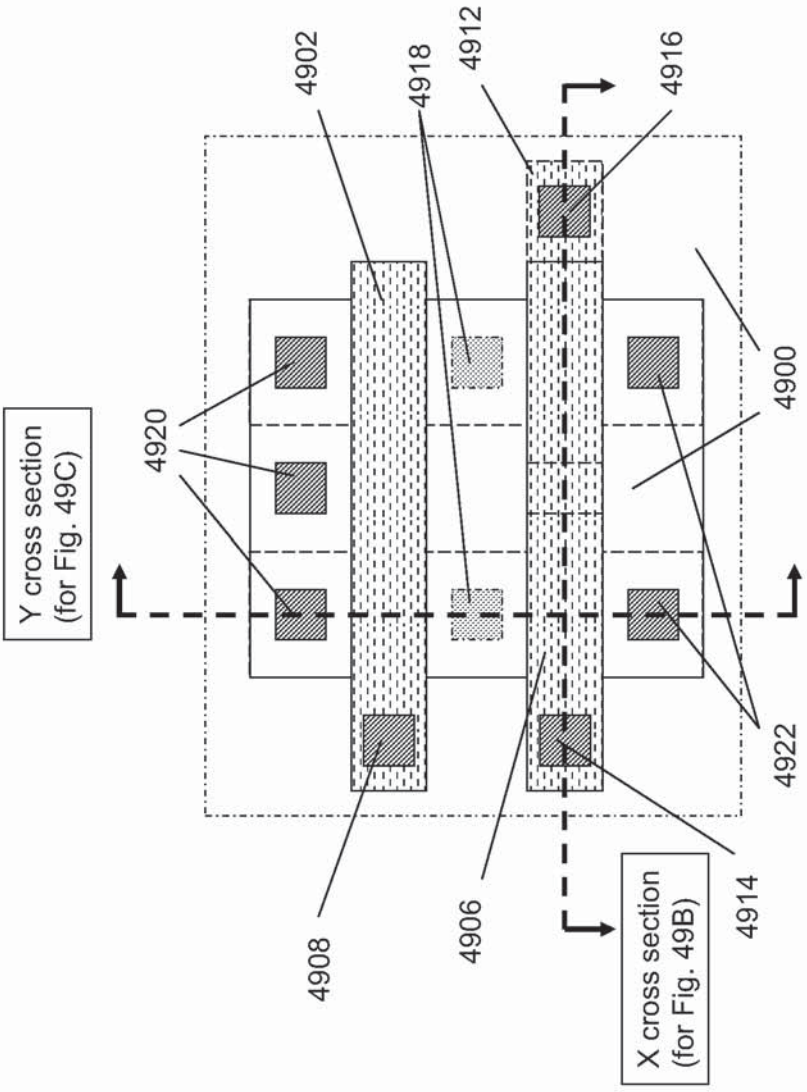

4902
4918
4912
4916
4900
4920
4922
4908
4906
4914
Y cross section
(for Fig. 49C)
X cross section
(for Fig. 49B)

Fig 49A

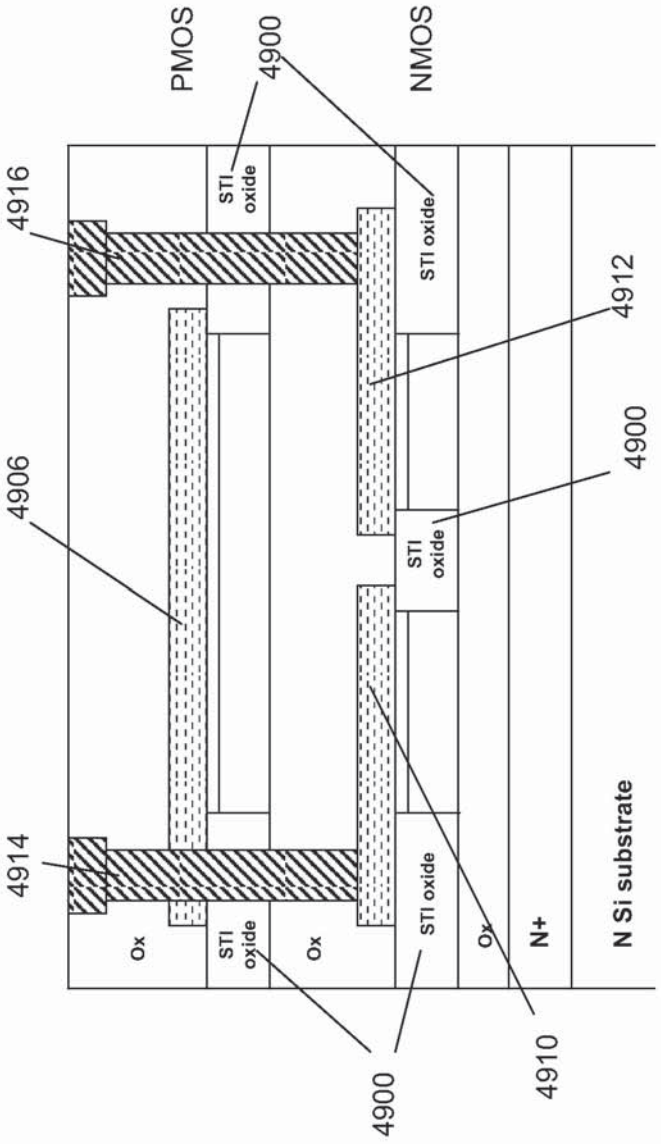

PMOS
4900
NMOS
4916
STI oxide
STI oxide
4912
4906
4900
STI oxide
4914
Ox
STI oxide
Ox
STI oxide
Ox
N+
N Si substrate
4900
4910

Fig 49B

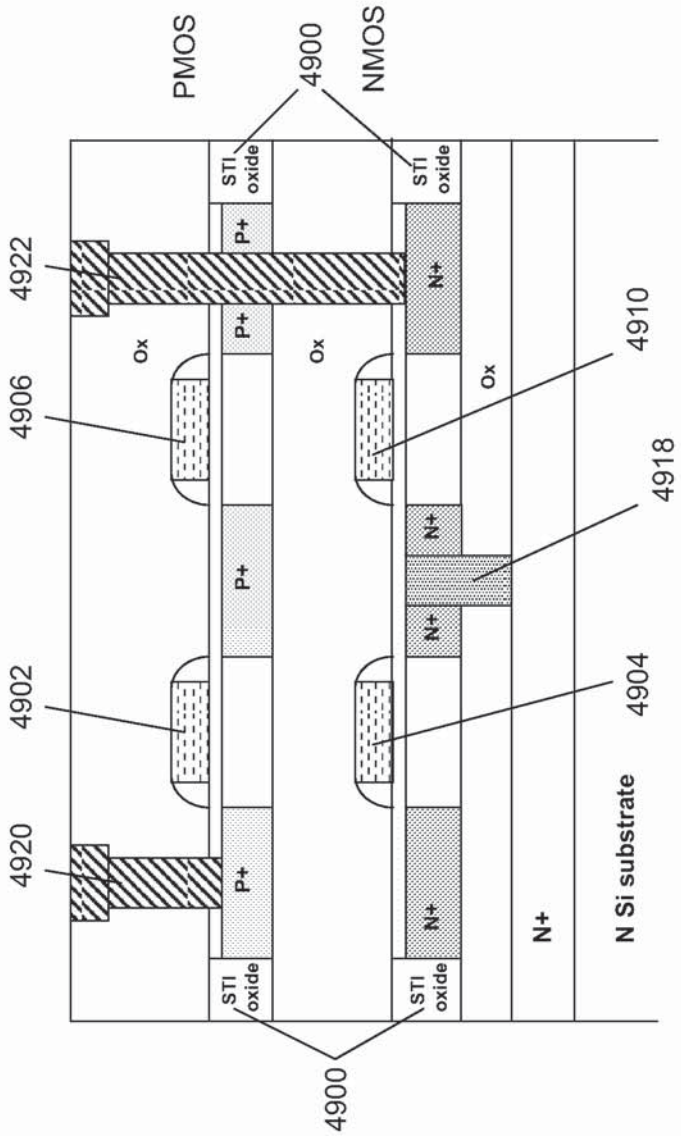

PMOS
4900
NMOS
STI oxide
P+
N+
Ox
4922
4906
4910
4918
4902
4904
4920
N Si substrate
4900

Fig 49C

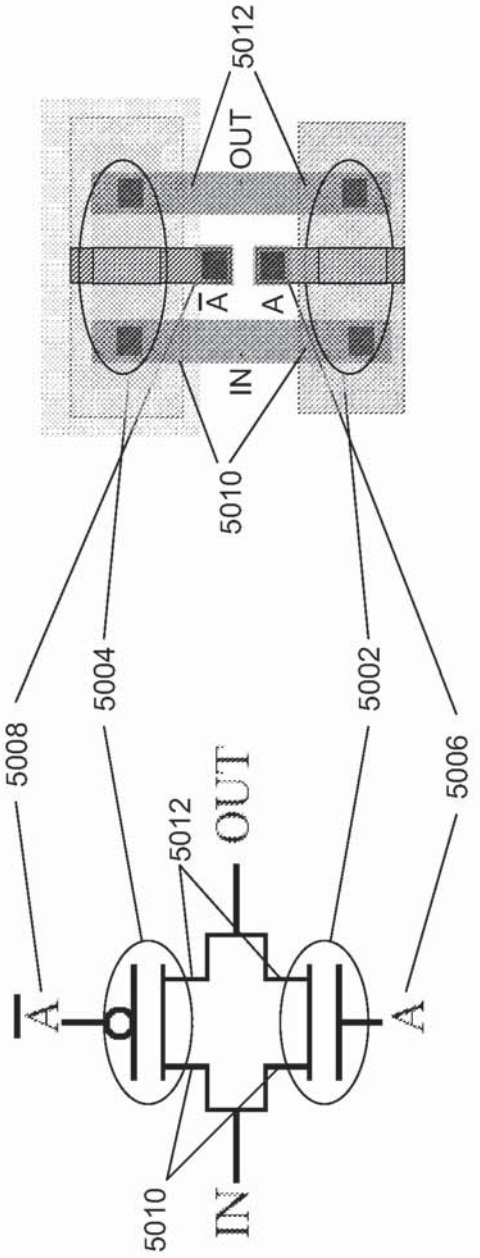


Fig 50A

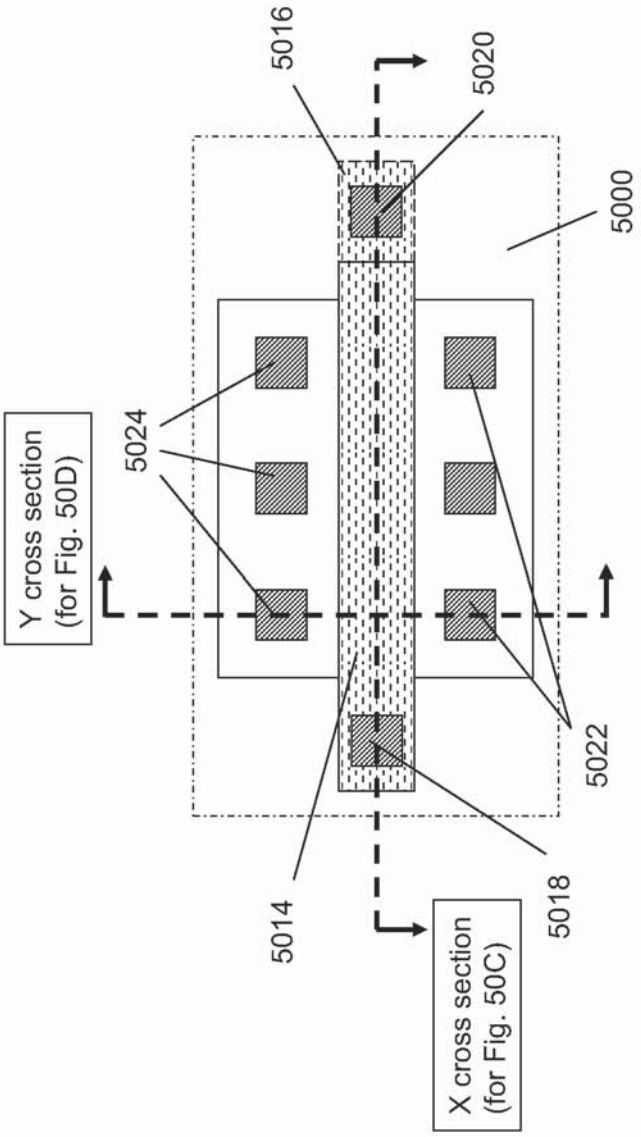

5016
5020
5000
5024
Y cross section
(for Fig. 50D)
5022
5014
5018
X cross section
(for Fig. 50C)

Fig 50B

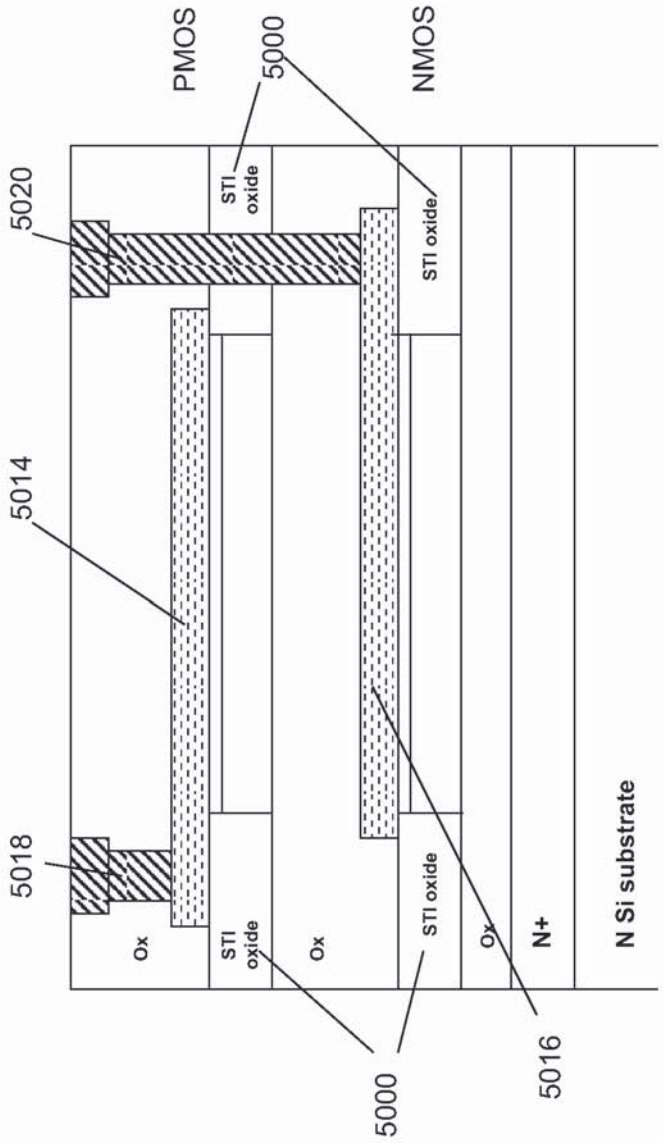

PMOS
5000
NMOS
5020
STI oxide
STI oxide
5014
5018
Ox
STI oxide
Ox
STI oxide
Ox
N+
N Si substrate
5000
5016

Fig 50C

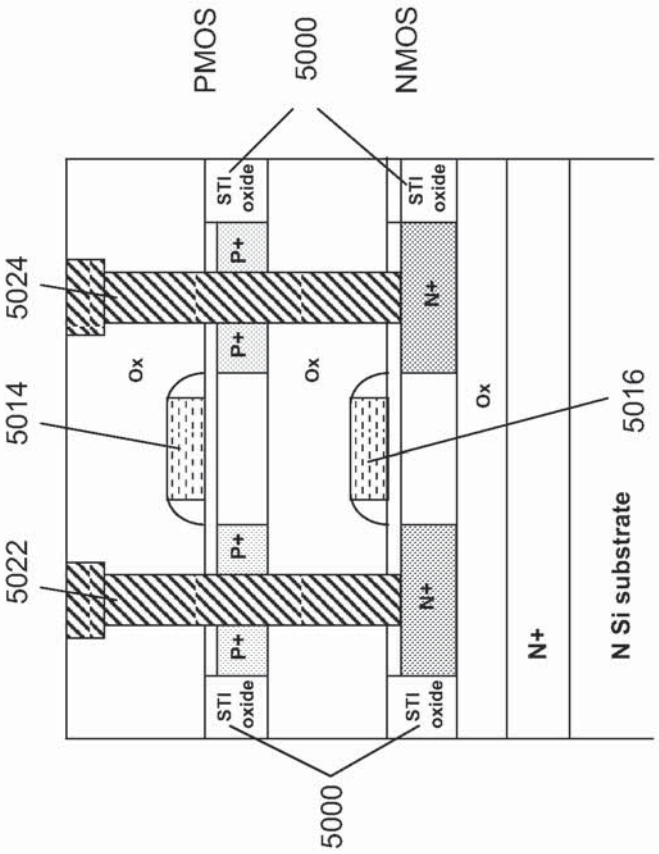

PMOS
5000
NMOS
STI oxide
P+
N+
5024
5014
5022
5016
Ox
N+
N Si substrate
5000

Fig 50D

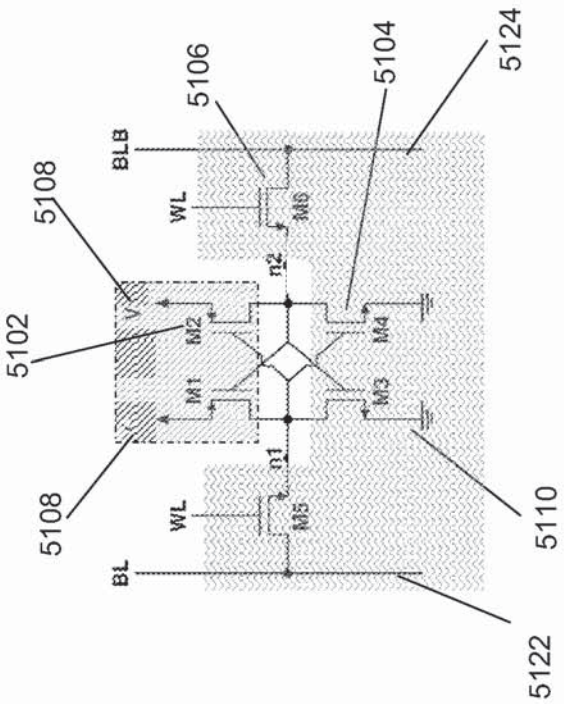

5102
5104
5106
5108
5108
5110
5122
5124
BLB
WL
M6
n2
M2
M4
M1
M3
n1
WL
M5
BL

Fig 51A

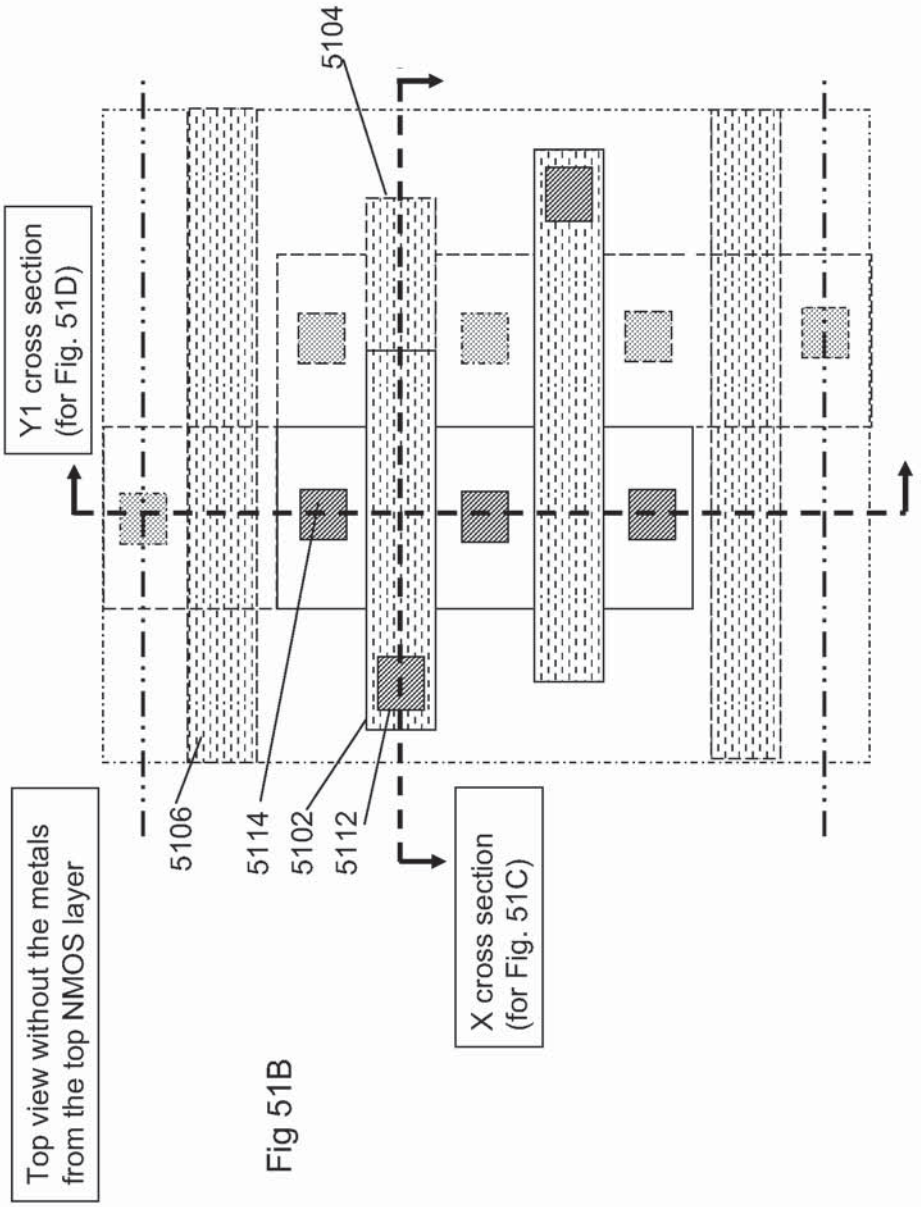

Y1 cross section
(for Fig. 51D)
5104
5106
5114
5102
5112
X cross section
(for Fig. 51C)
Top view without the metals
from the top NMOS layer

Fig 51B

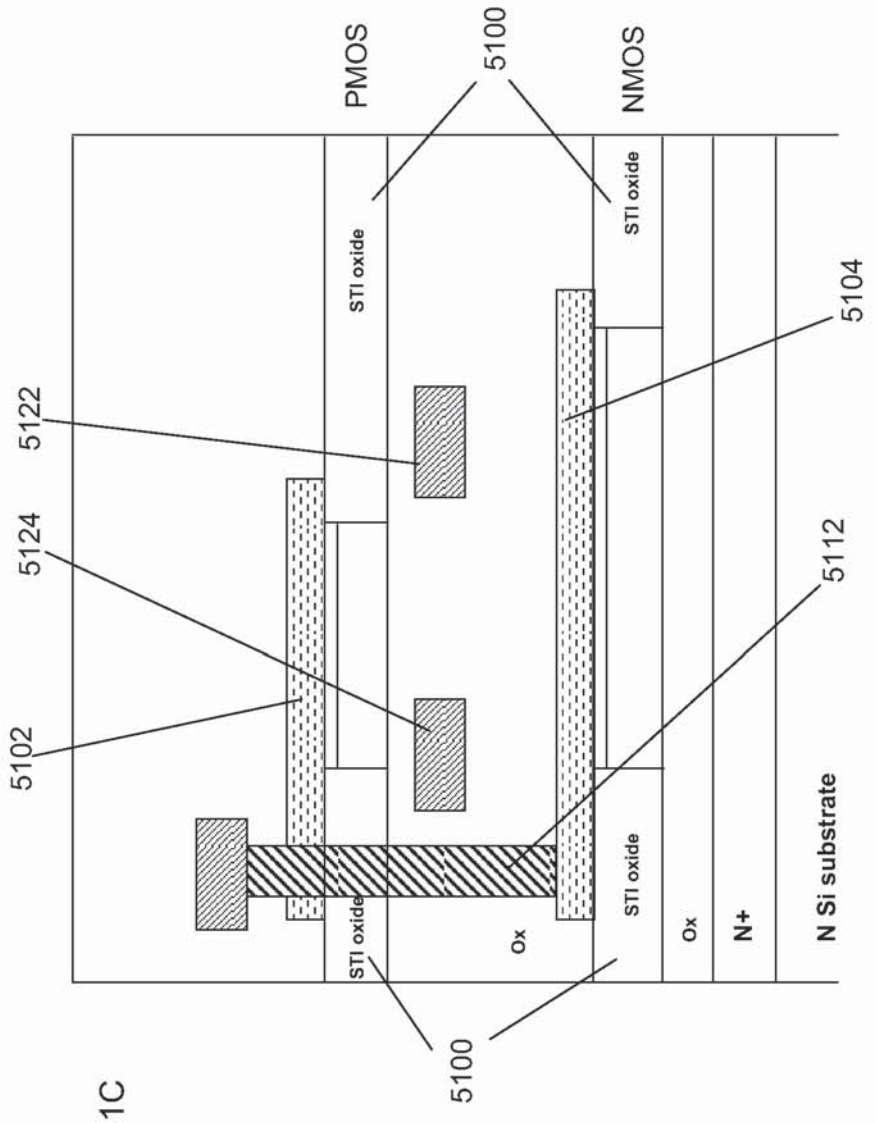

PMOS
5100
NMOS
STI oxide
STI oxide
5104
5122
5124
5112
5102
STI oxide
Ox
STI oxide
Ox
N+
N Si substrate
5100

Fig 51C

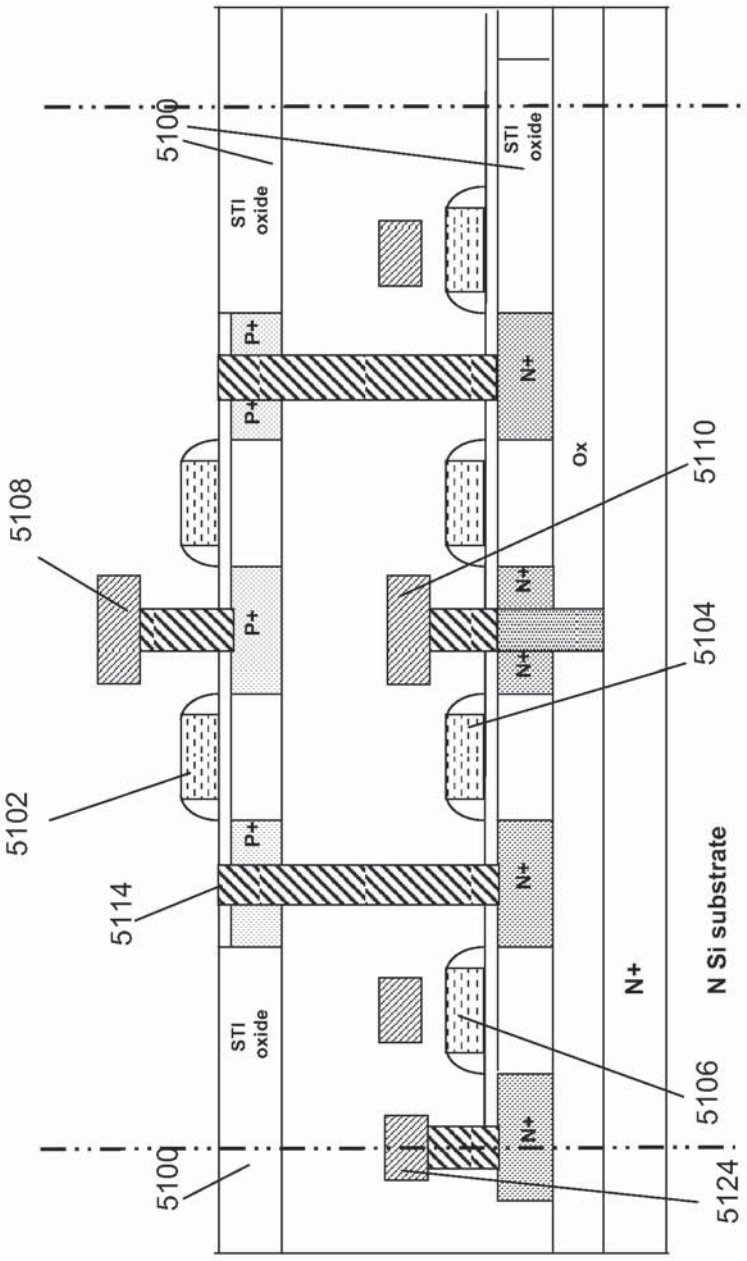

5100
STI oxide
STI oxide
P+
P+
N+
Ox
5110
5108
P+
N+
5104
N+
5102
P+
N+
5114
STI oxide
N+
N Si substrate
5106
5100
N+
5124

Fig 51D

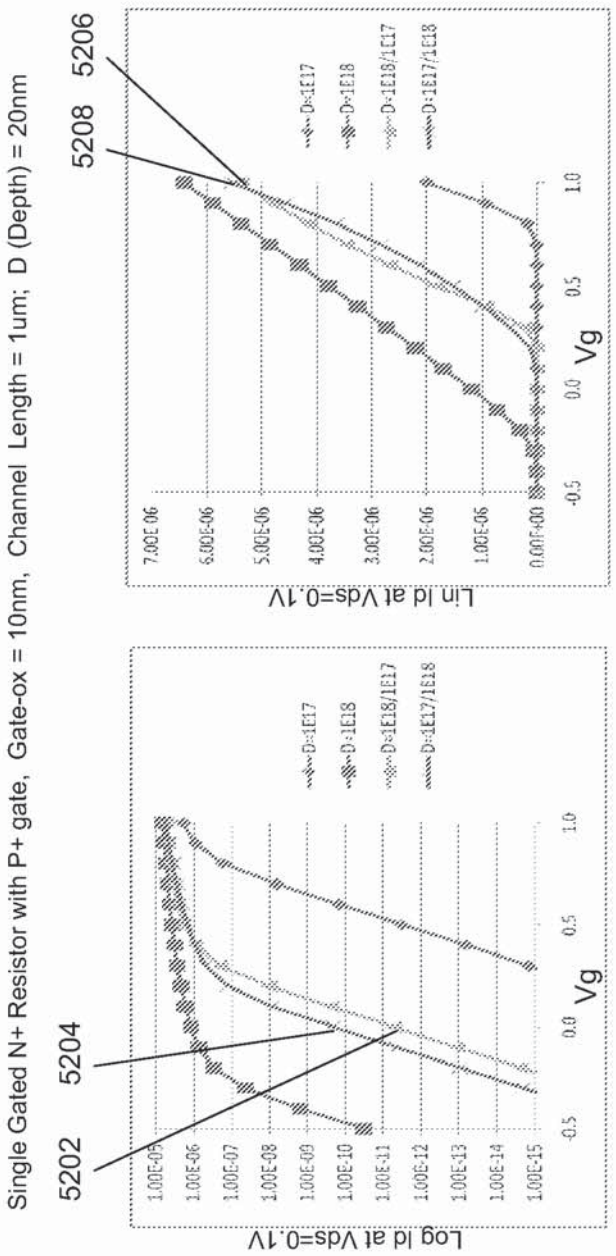


Fig 52A

Fig 52B

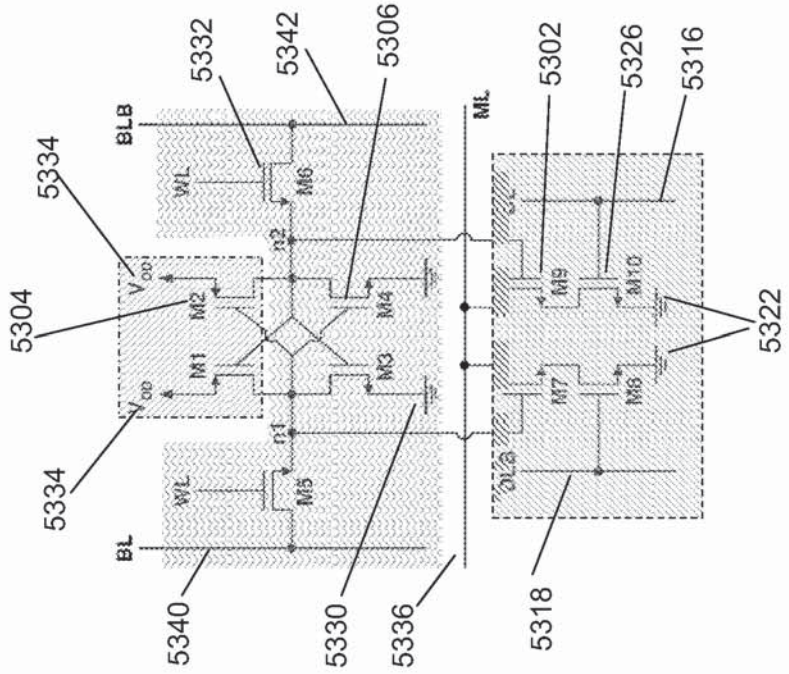

5332
5342
5306
5302
5326
5316
BLB
ML
5334
WL
M6
n2
M9
M10
5304
V_{DD}
M2
M4
M1
M3
M7
M8
5322
V_{DD}
5334
n1
WL
M5
DL
BL
5340
5330
5336
5318

Fig 53A

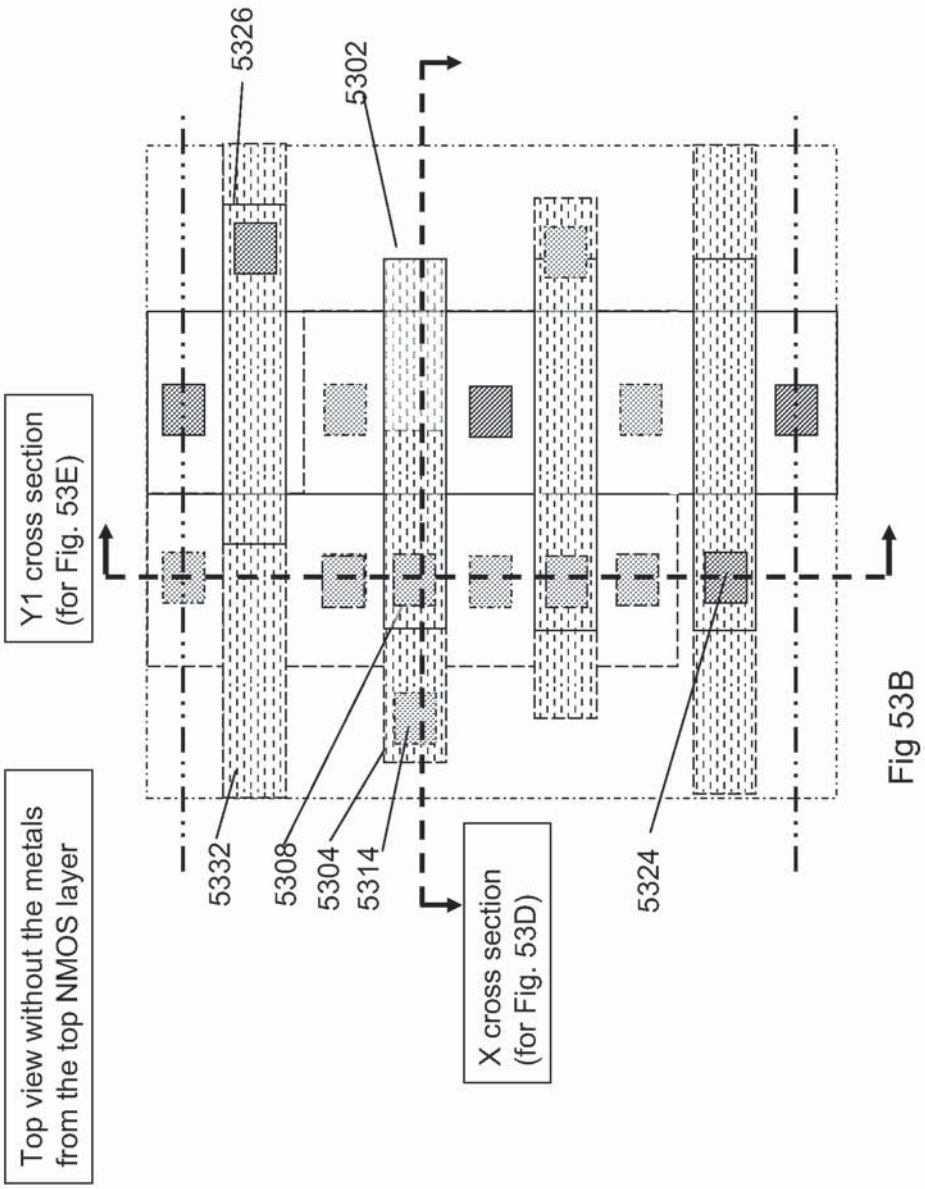

Top view without the metals from the top NMOS layer
Y1 cross section (for Fig. 53E)
X cross section (for Fig. 53D)
5326
5302
5332
5308
5304
5314
5324

Fig 53B

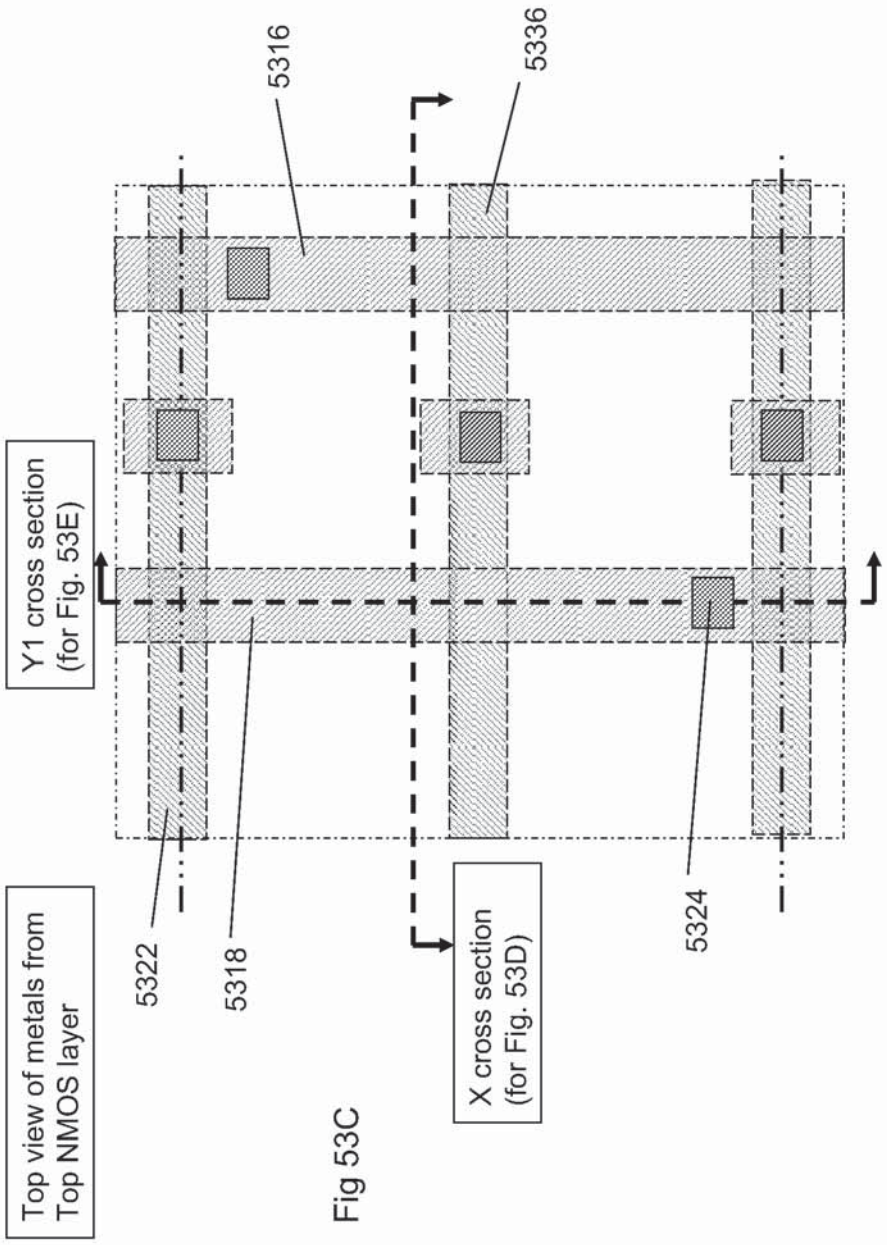

5316
5336
Y1 cross section
(for Fig. 53E)
Top view of metals from
Top NMOS layer
5322
5318
X cross section
(for Fig. 53D)
5324

Fig 53C

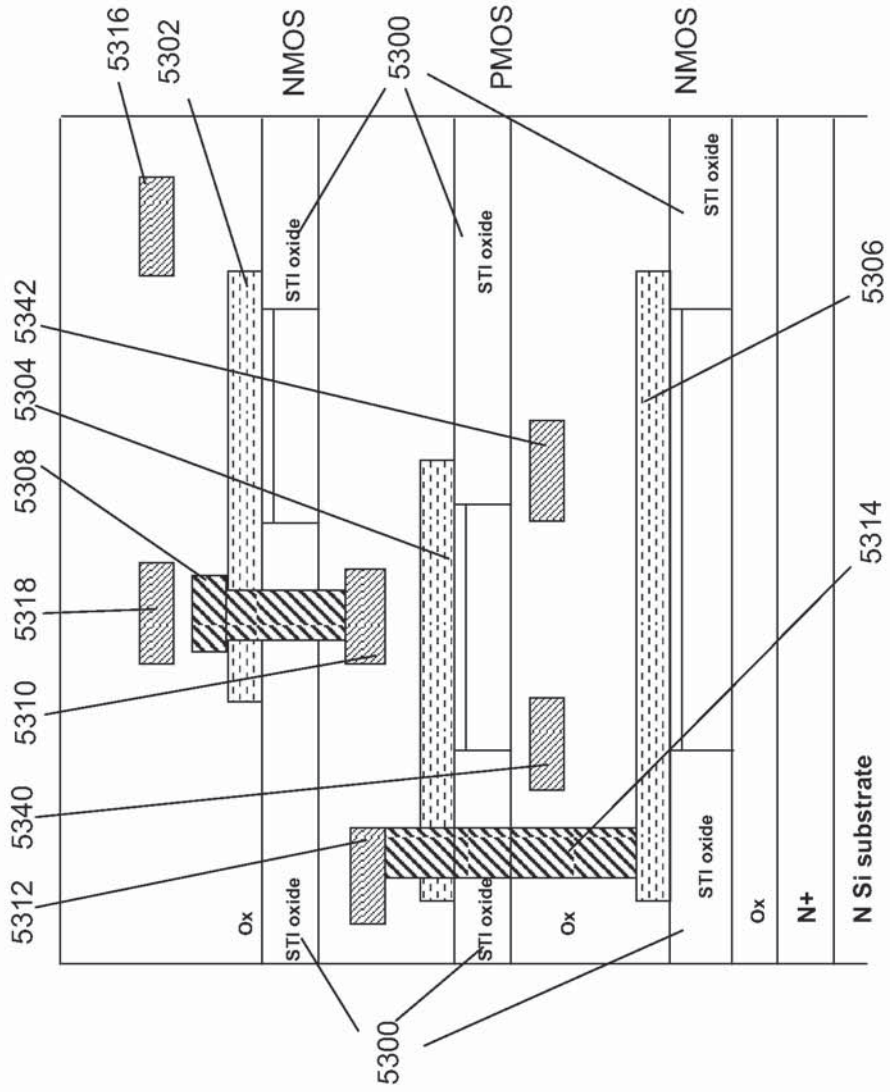

5316
5302
NMOS
5300
PMOS
NMOS
STI oxide
STI oxide
STI oxide
5342
5304
5308
5318
5310
5340
5312
5306
5314
Ox
STI oxide
STI oxide
Ox
STI oxide
Ox
N+
N Si substrate
5300

Fig 53D

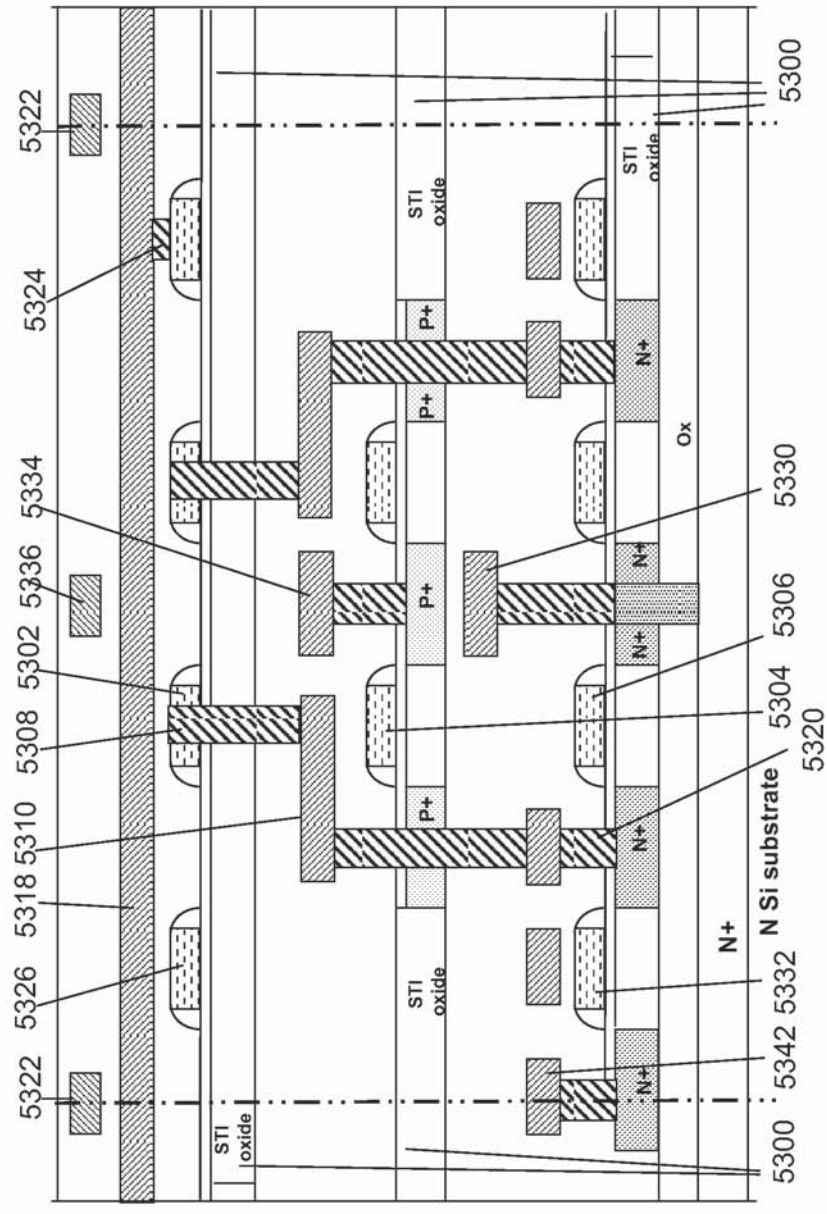

5322
5324
5334
5336
5302
5308
5310
5318
5326
5322
5300
5330
5306
5304
5320
5332
5342
5300
STI oxide
P+
N+
Ox
N Si substrate

Fig 53E

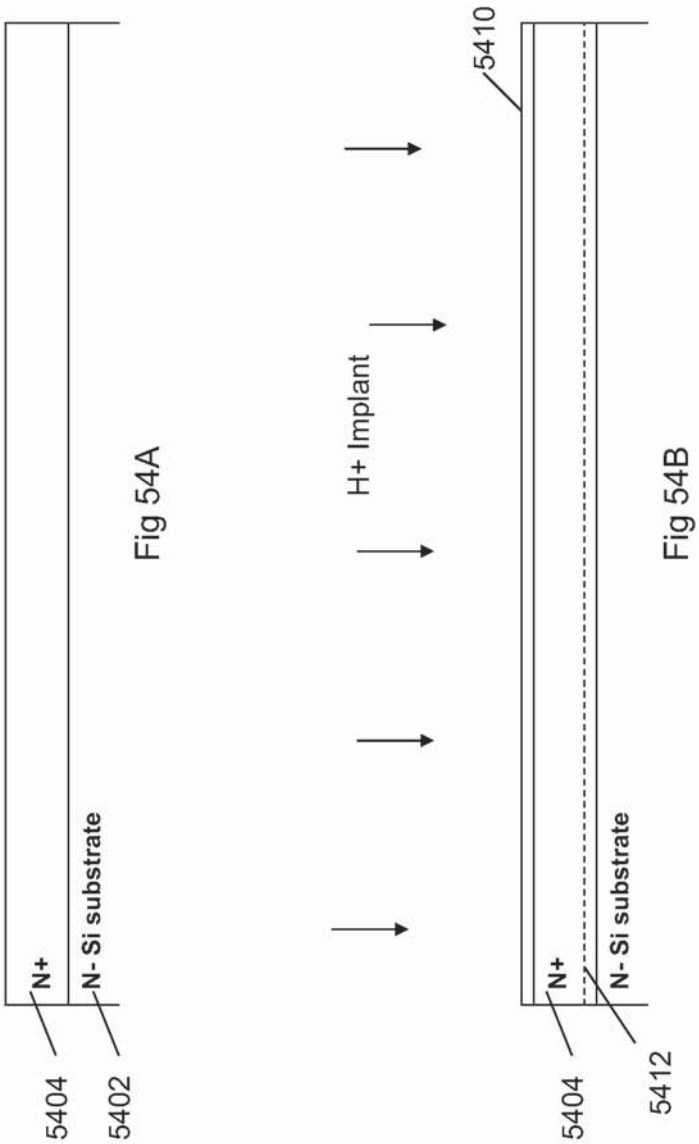


Fig 54A

Fig 54B

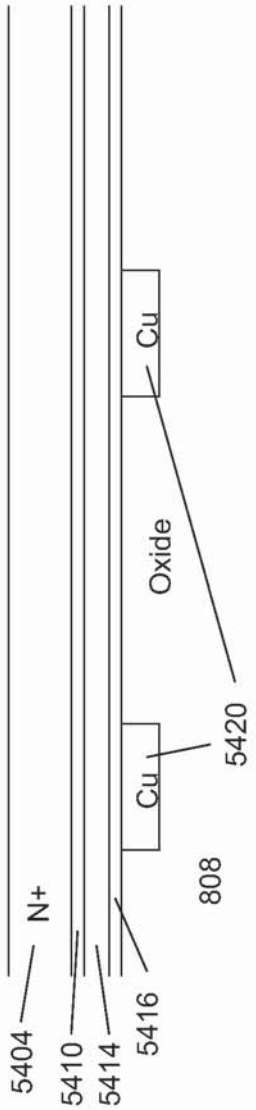


Fig 54C



Fig 55A

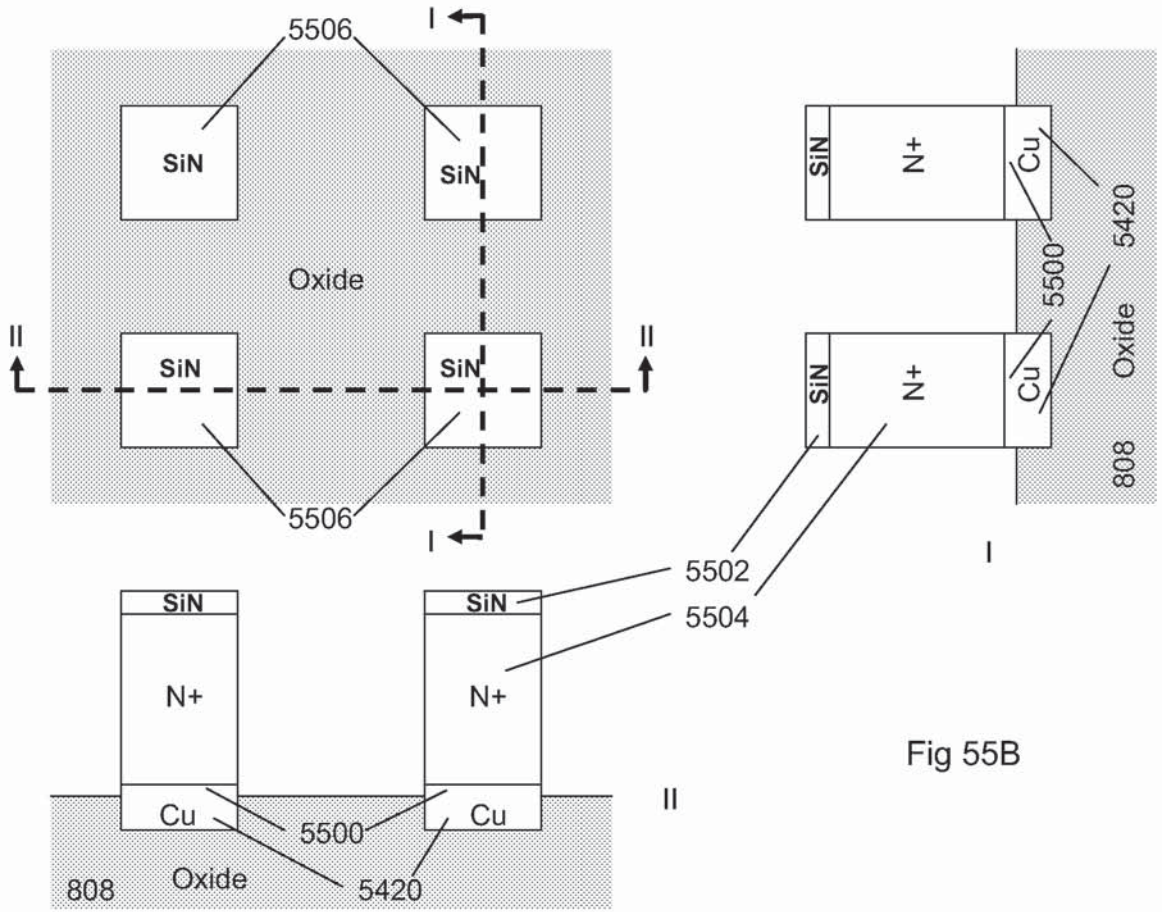
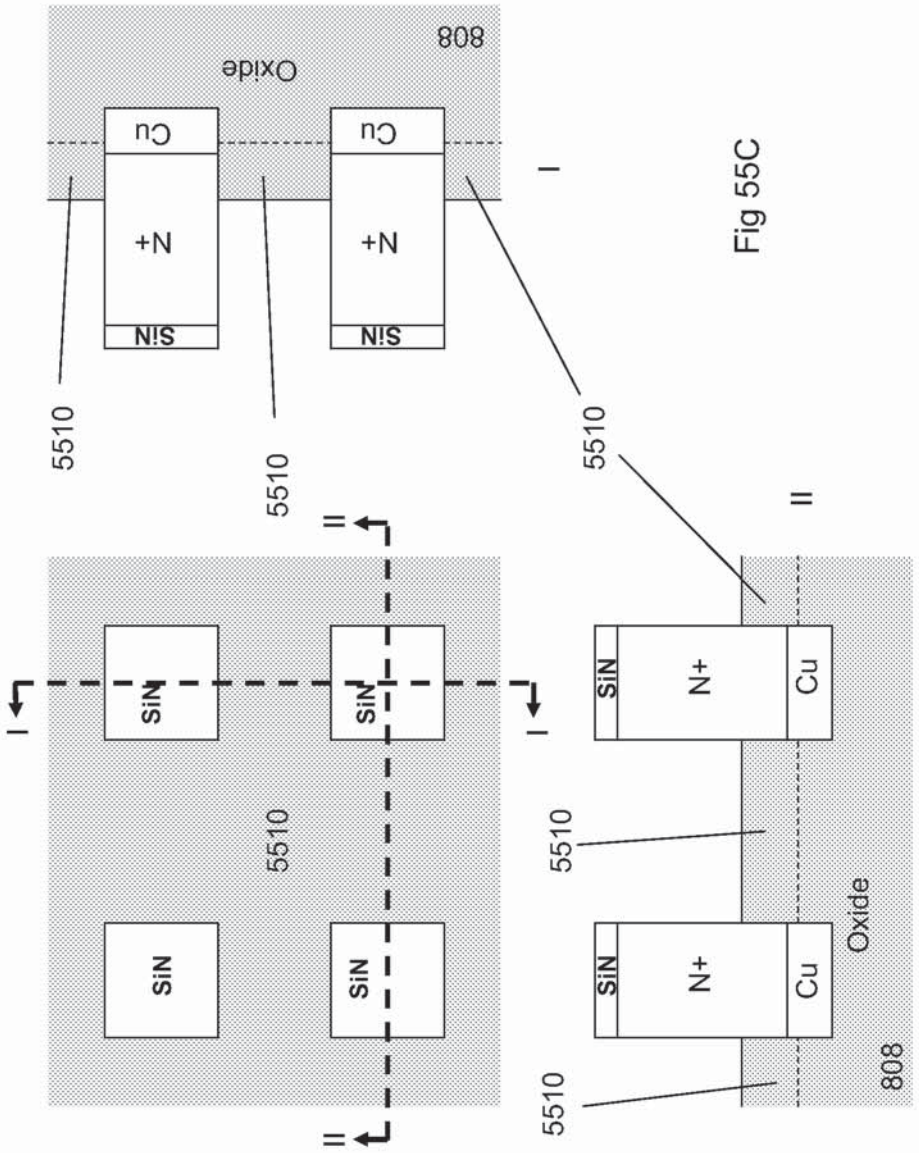

5506
I
SiN
SiN
Oxide
II
SiN
SiN
II
5506
I
SiN
N+
Cu
5420
5500
SiN
N+
Cu
Oxide
808
I
5502
5504
SiN
SiN
N+
N+
Cu
Cu
5500
II
808
Oxide
5420

Fig 55B


808
Oxide
Cu
N+
SiN
5510
I
II
Fig 55C

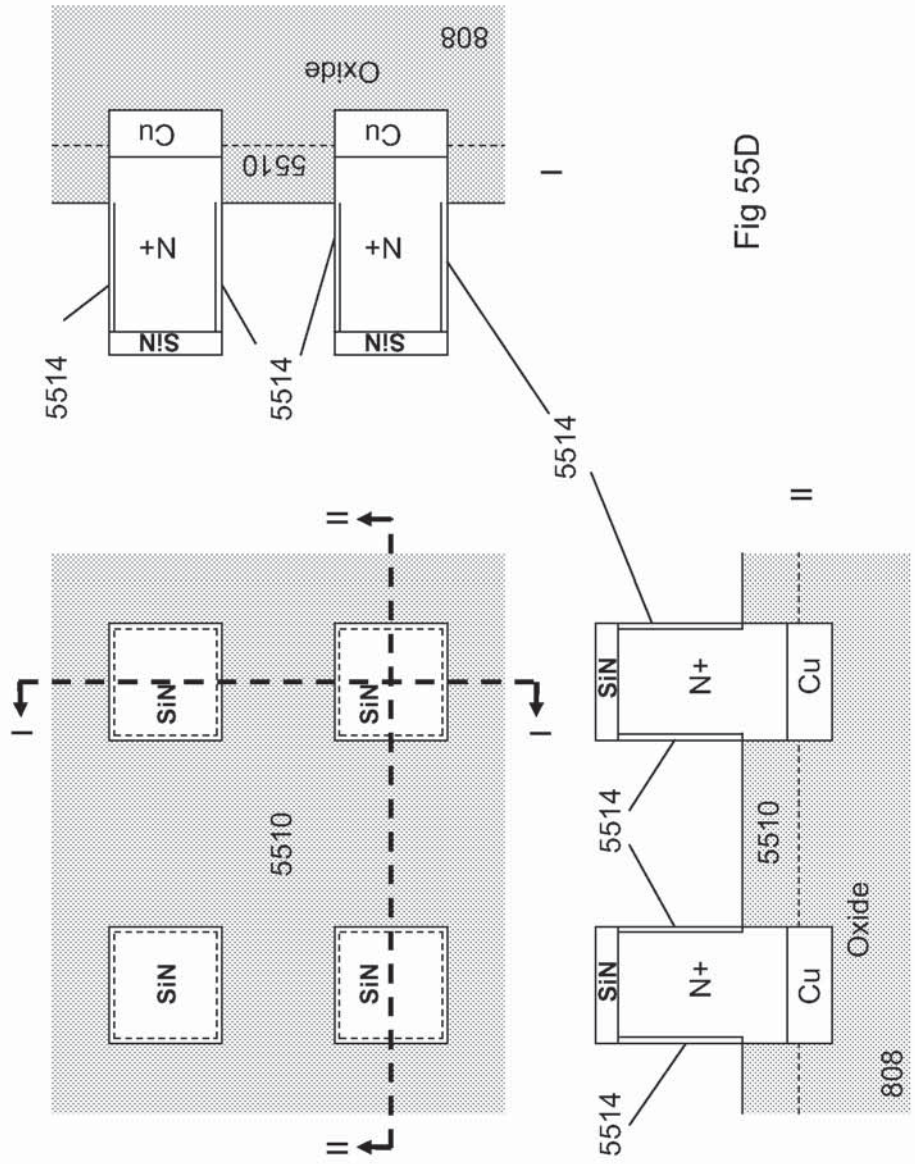


Fig 55D

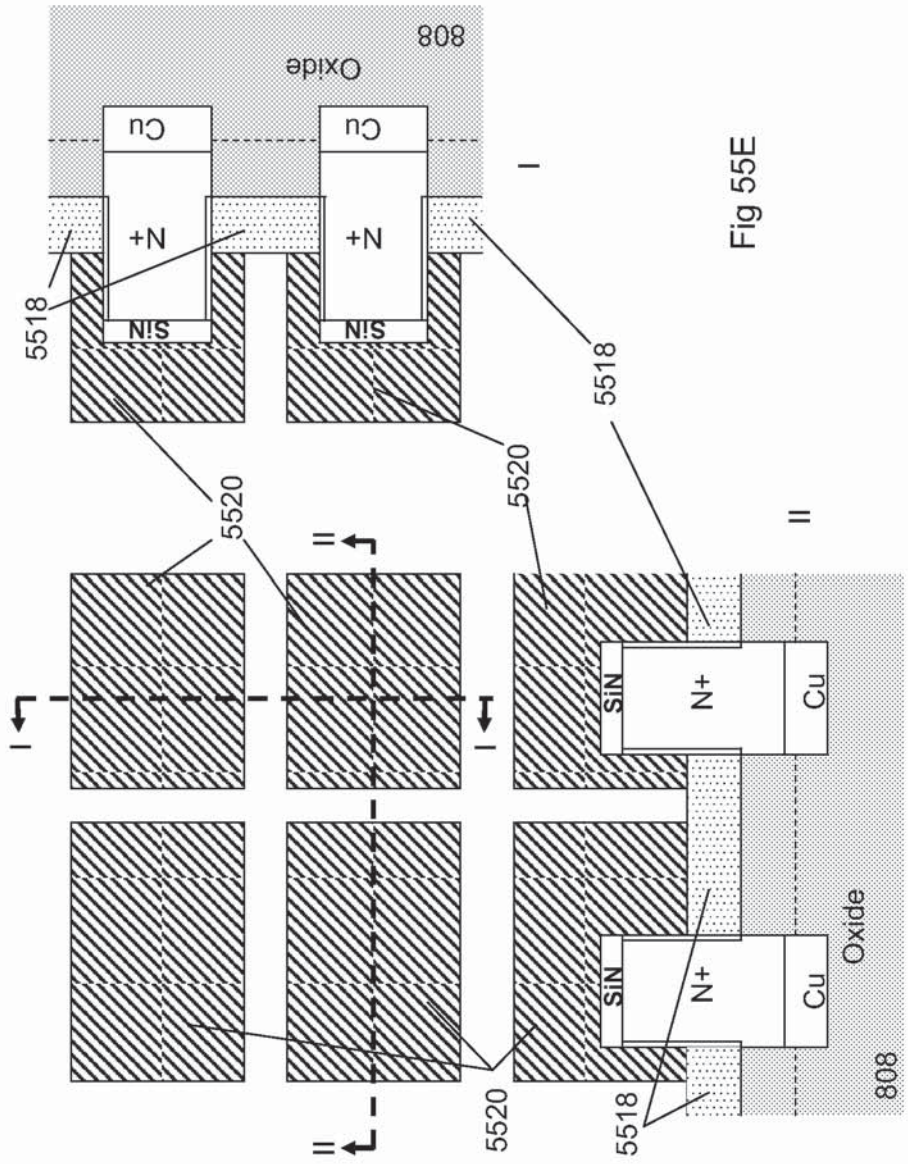


Fig 55E

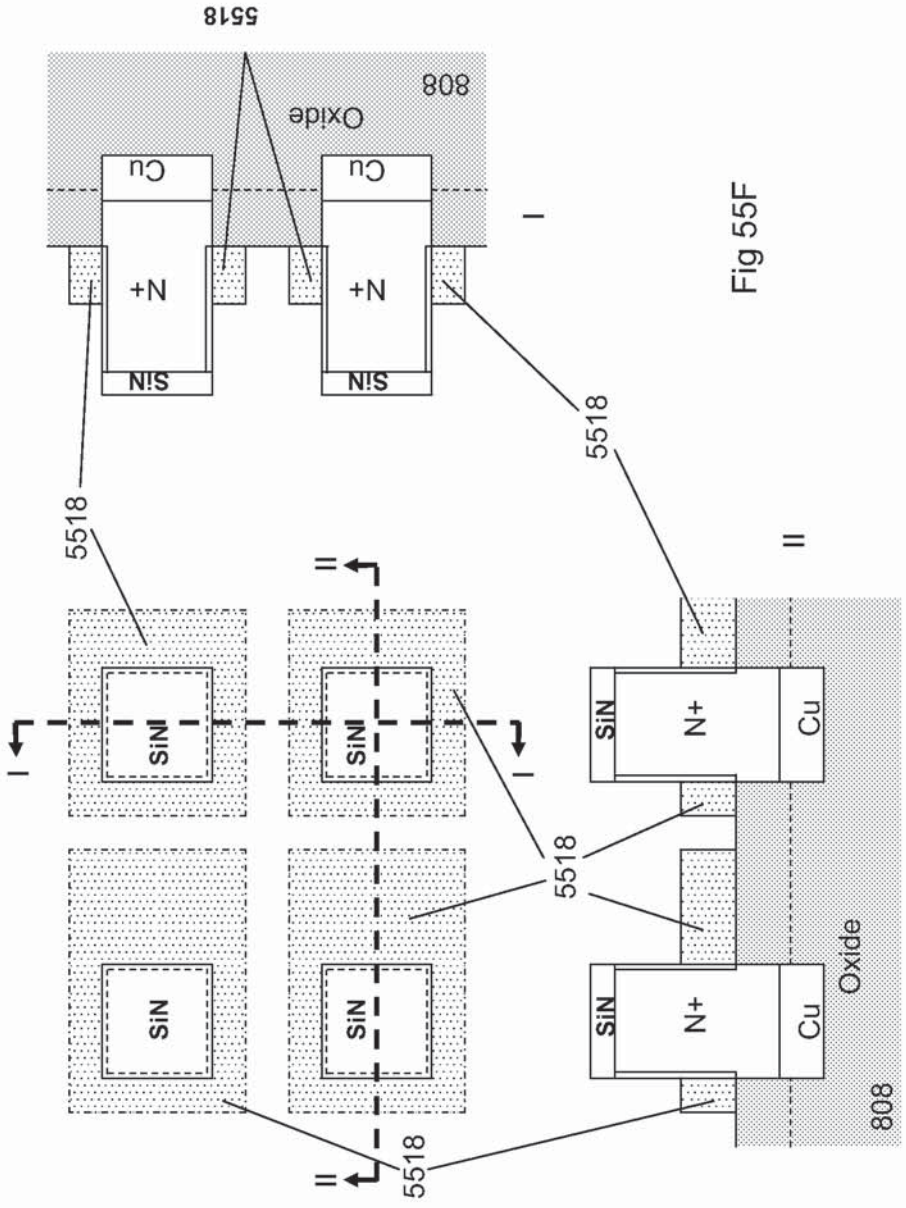

5518
808
Oxide
Cu
N+
SiN
I
II
5518
5518
5518
5518
SiN
N+
Cu
Oxide
808

Fig 55F

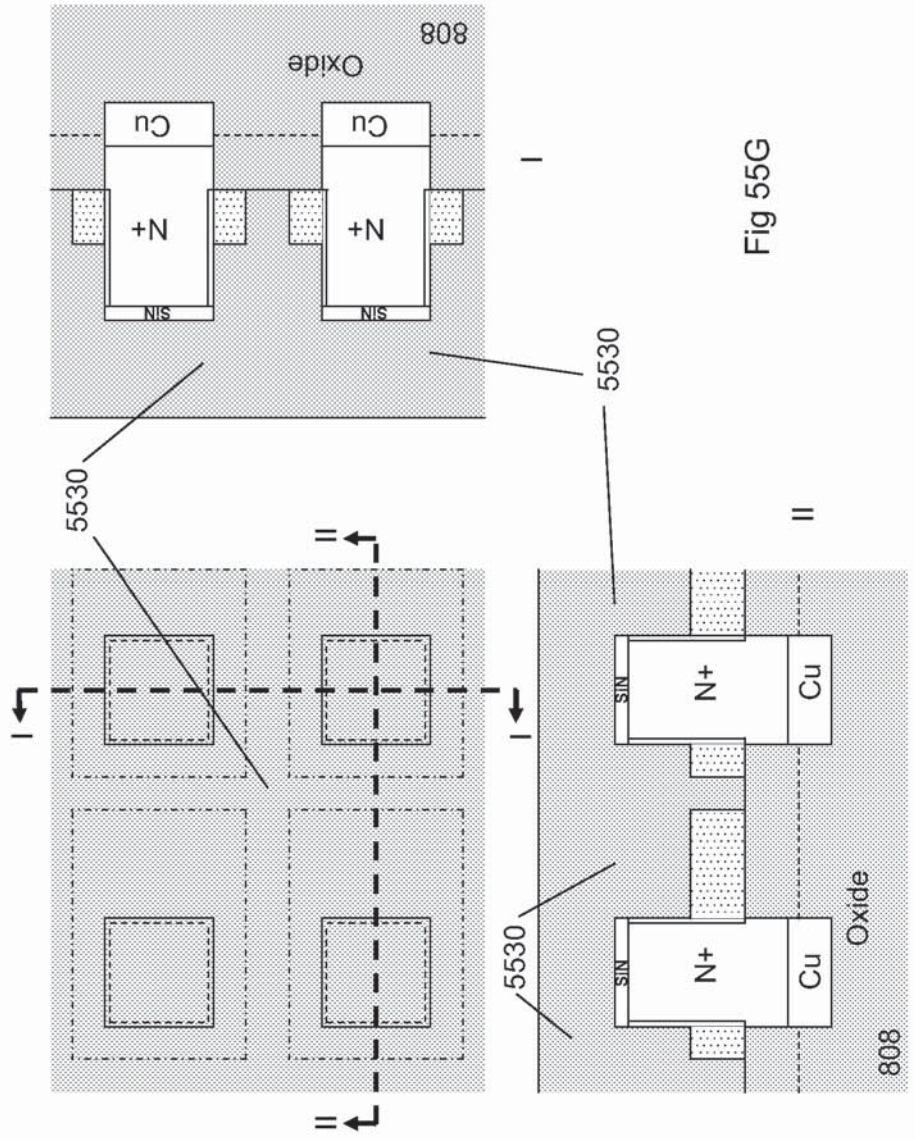

808
Oxide
Cu
Cu
N+
N+
SiN
SiN
I
I
5530
5530
II
II
I
I
SiN
N+
Cu
SiN
N+
Cu
Oxide
808
5530

Fig 55G

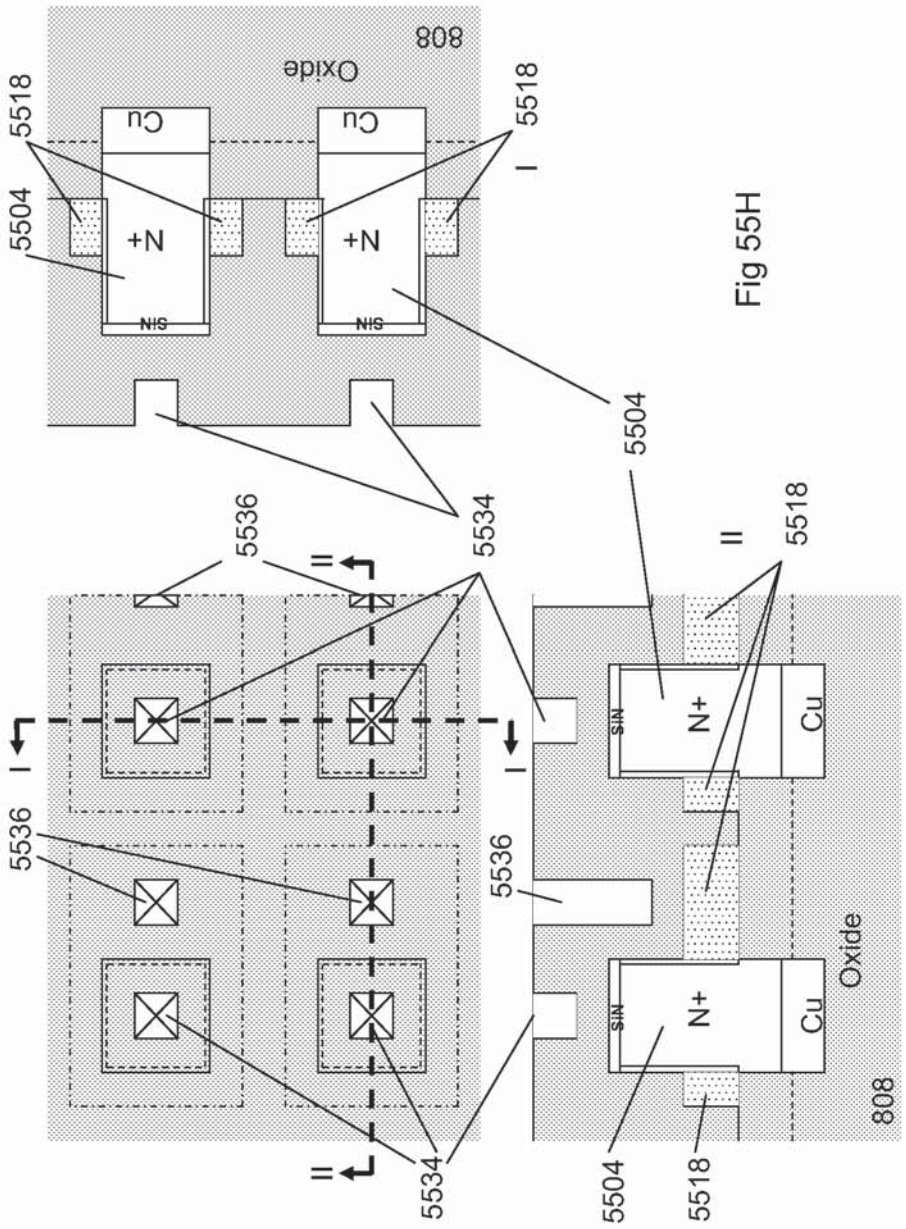

808
Oxide
5518
5518
Cu
Cu
5504
N+
N+
SiN
SiN
I
I
5504
5534
5536
II
5518
II
5536
5534
5536
N+
Cu
SiN
N+
Cu
SiN
Oxide
808
5504
5518

Fig 55H

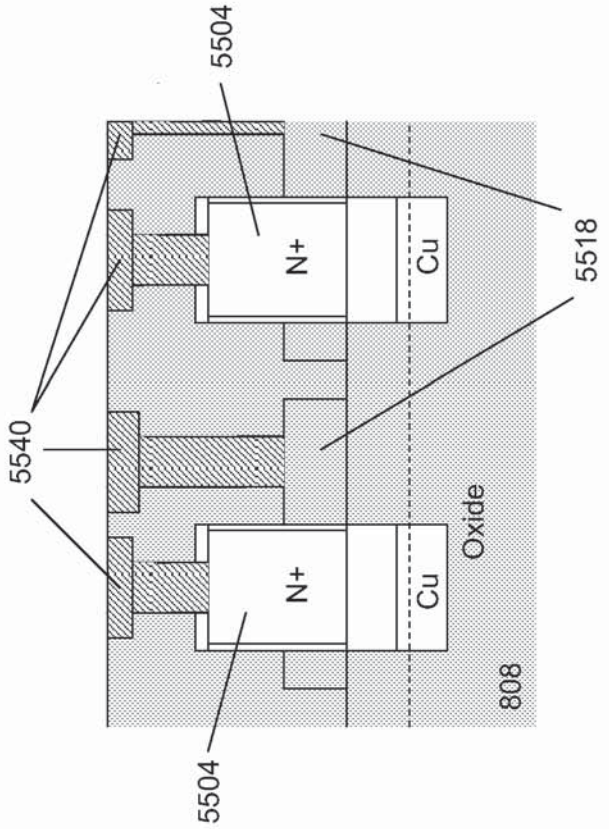


Fig 55I

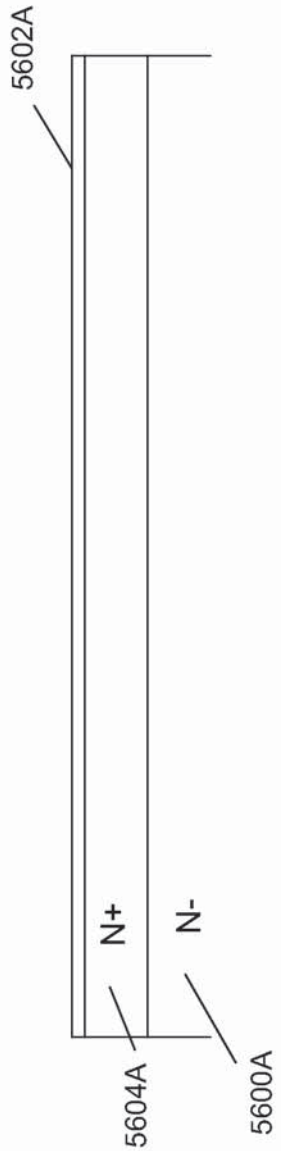


Fig 56A

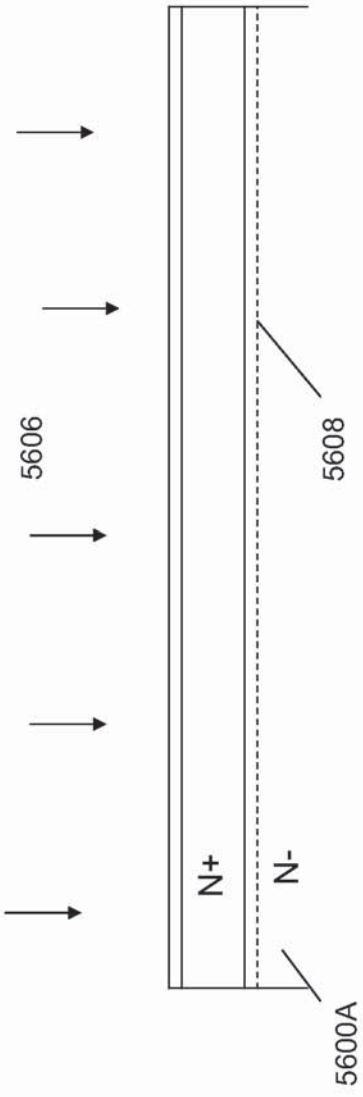


Fig 56B

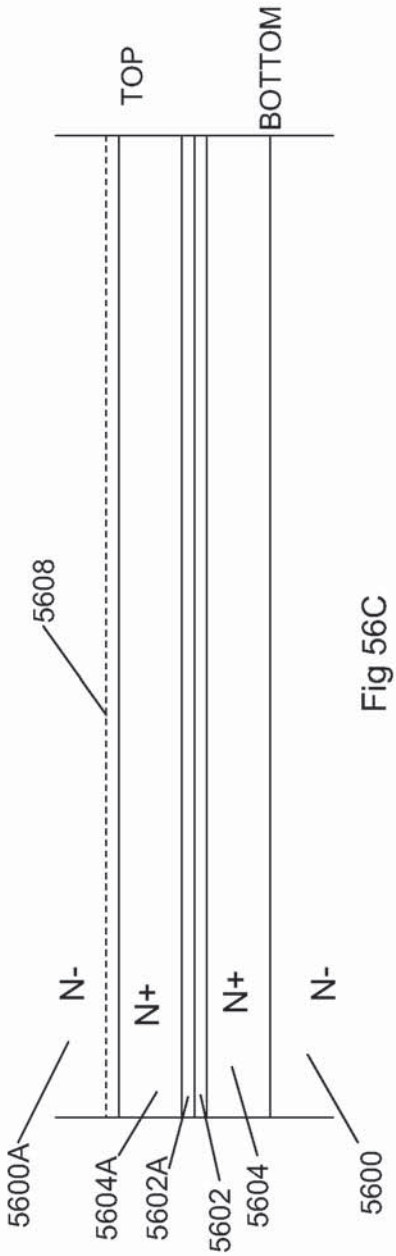


Fig 56C

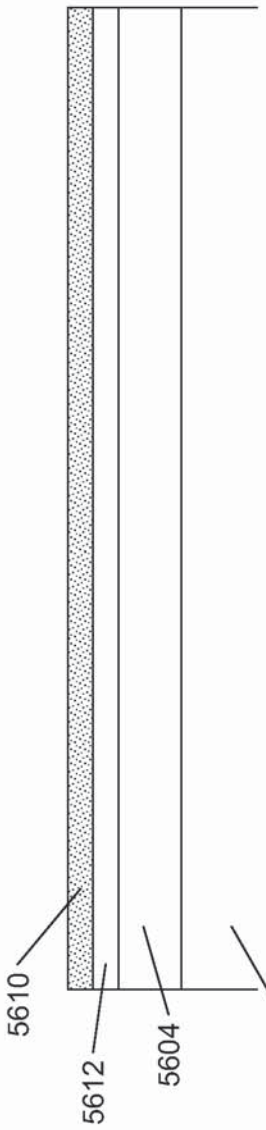


Fig 56D

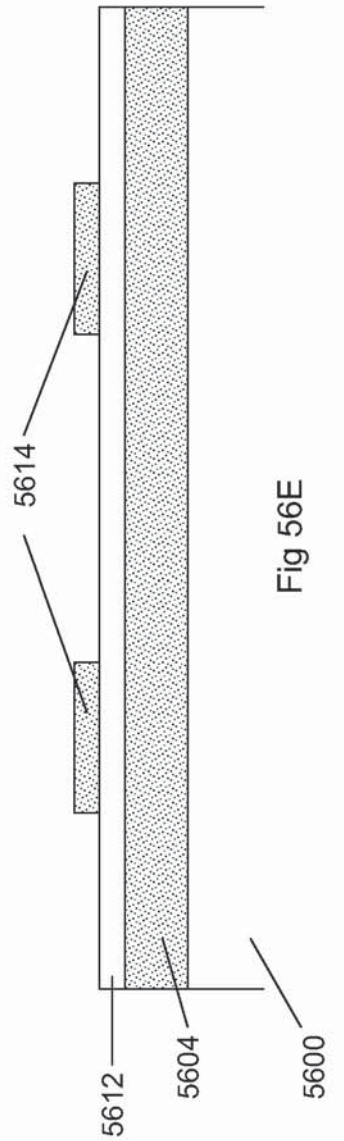


Fig 56E

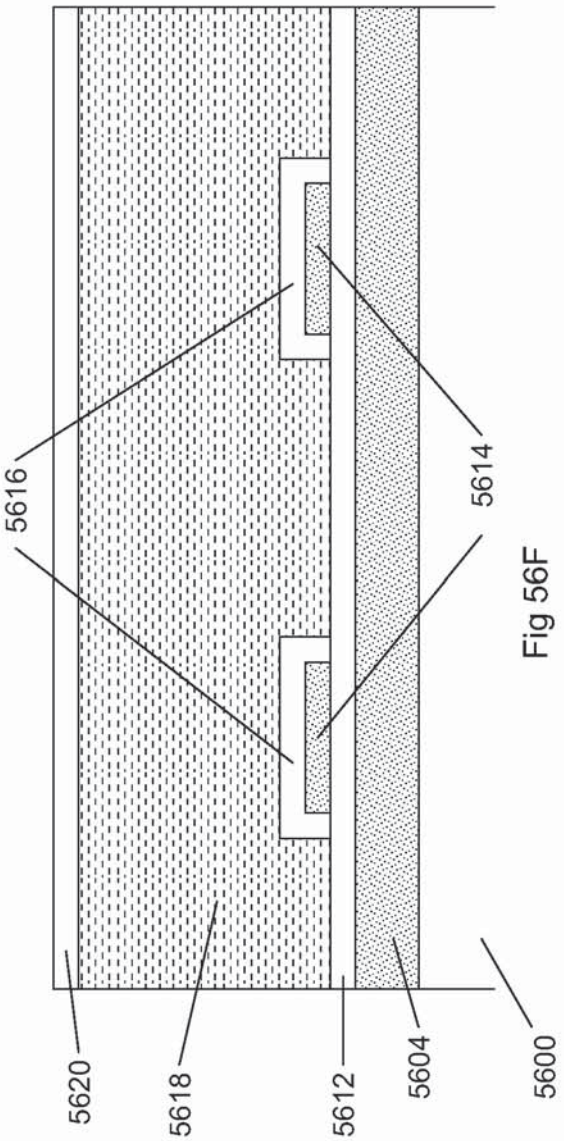


Fig 56F

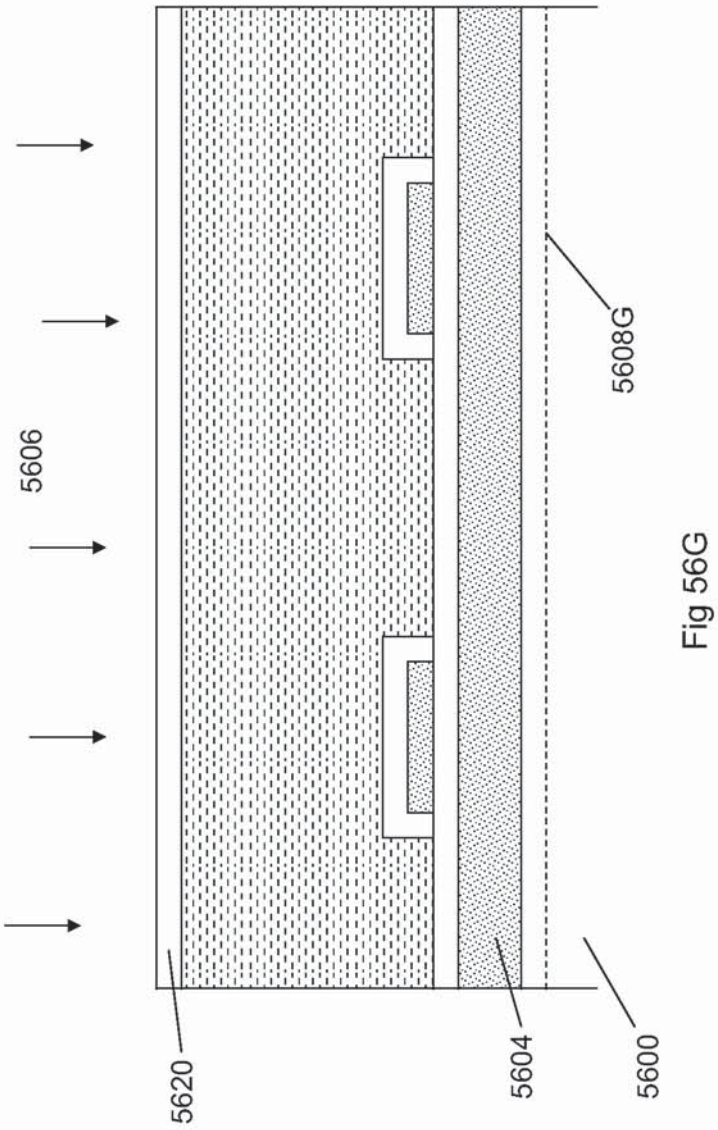


Fig 56G

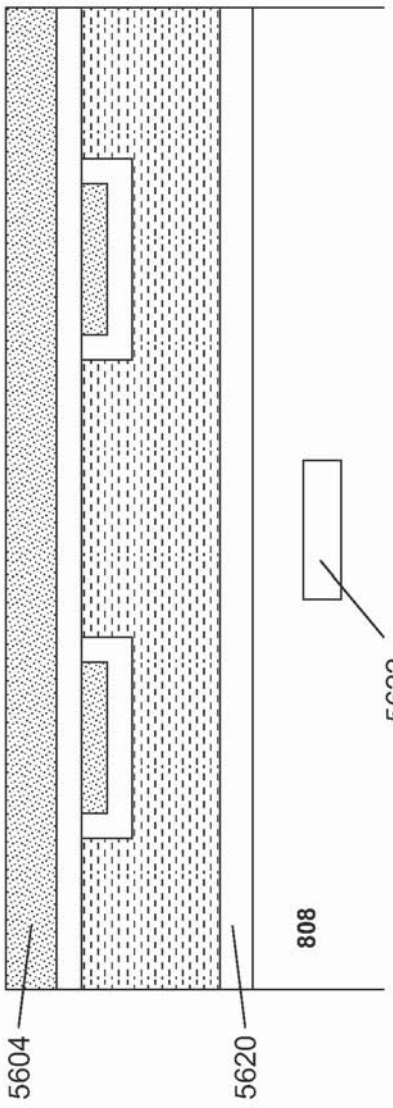


Fig 56H

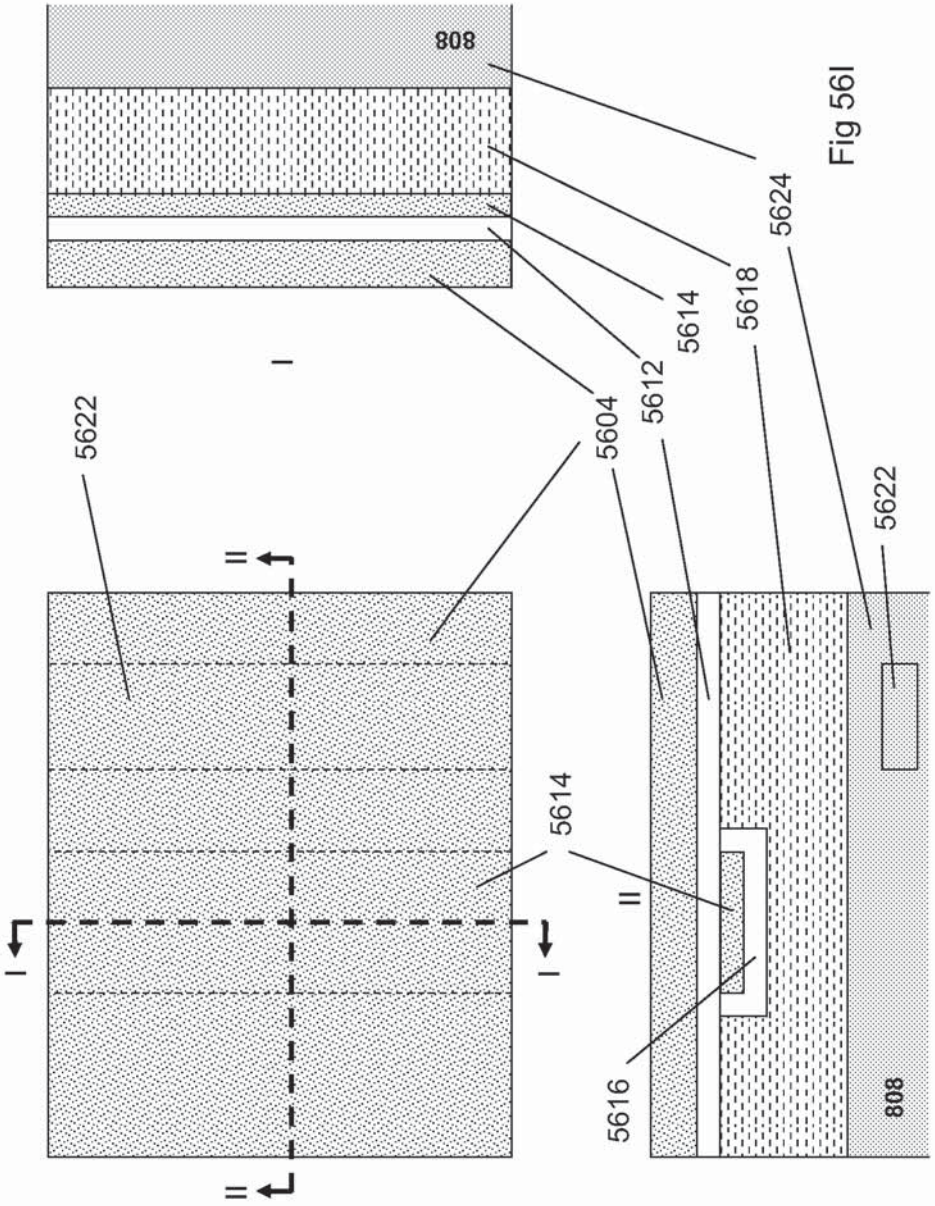


Fig 56I

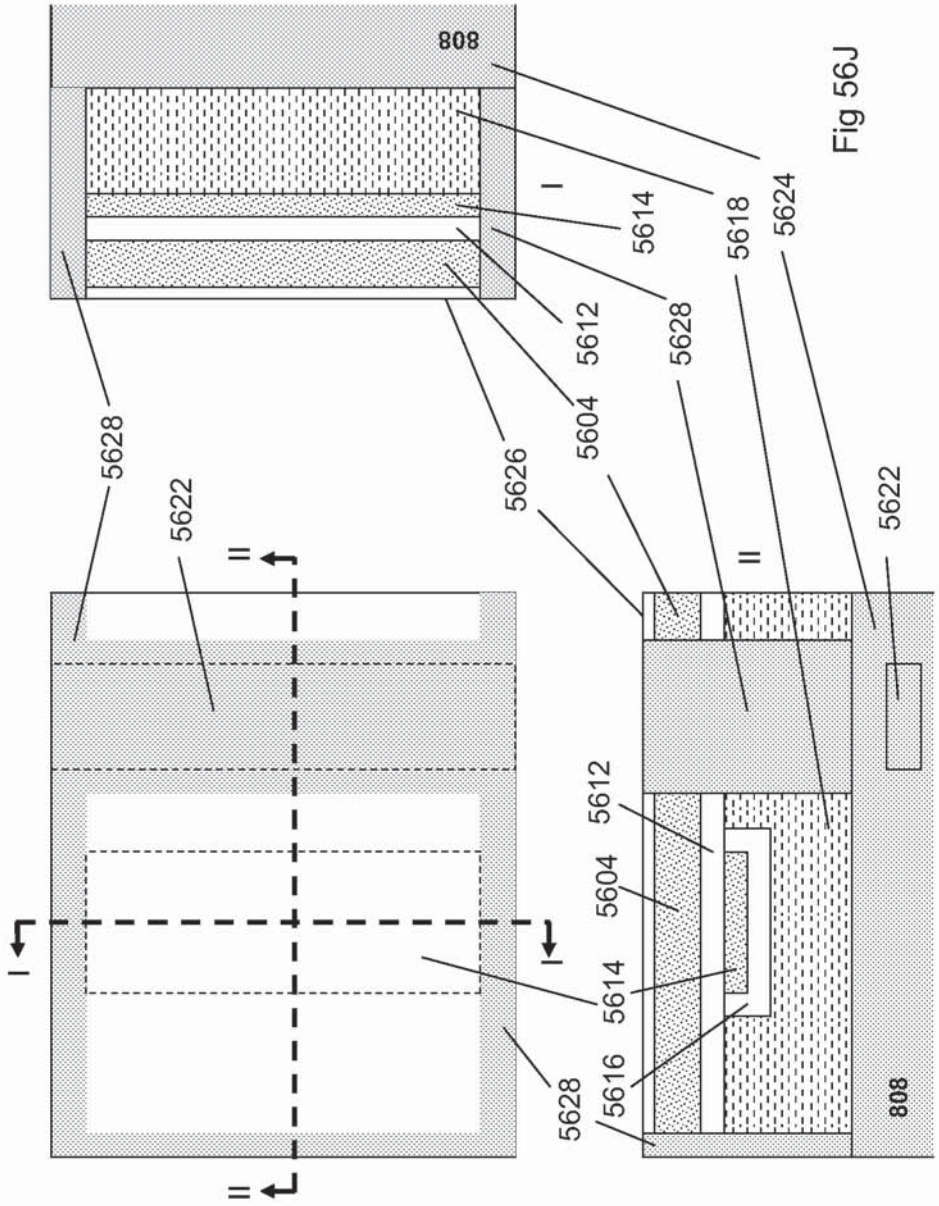

808
I
5614
5618
5624
5612
5628
5604
5628
5626
5622
II
5622
II
5612
5604
I
I
5614
5616
5628
808

Fig 56J

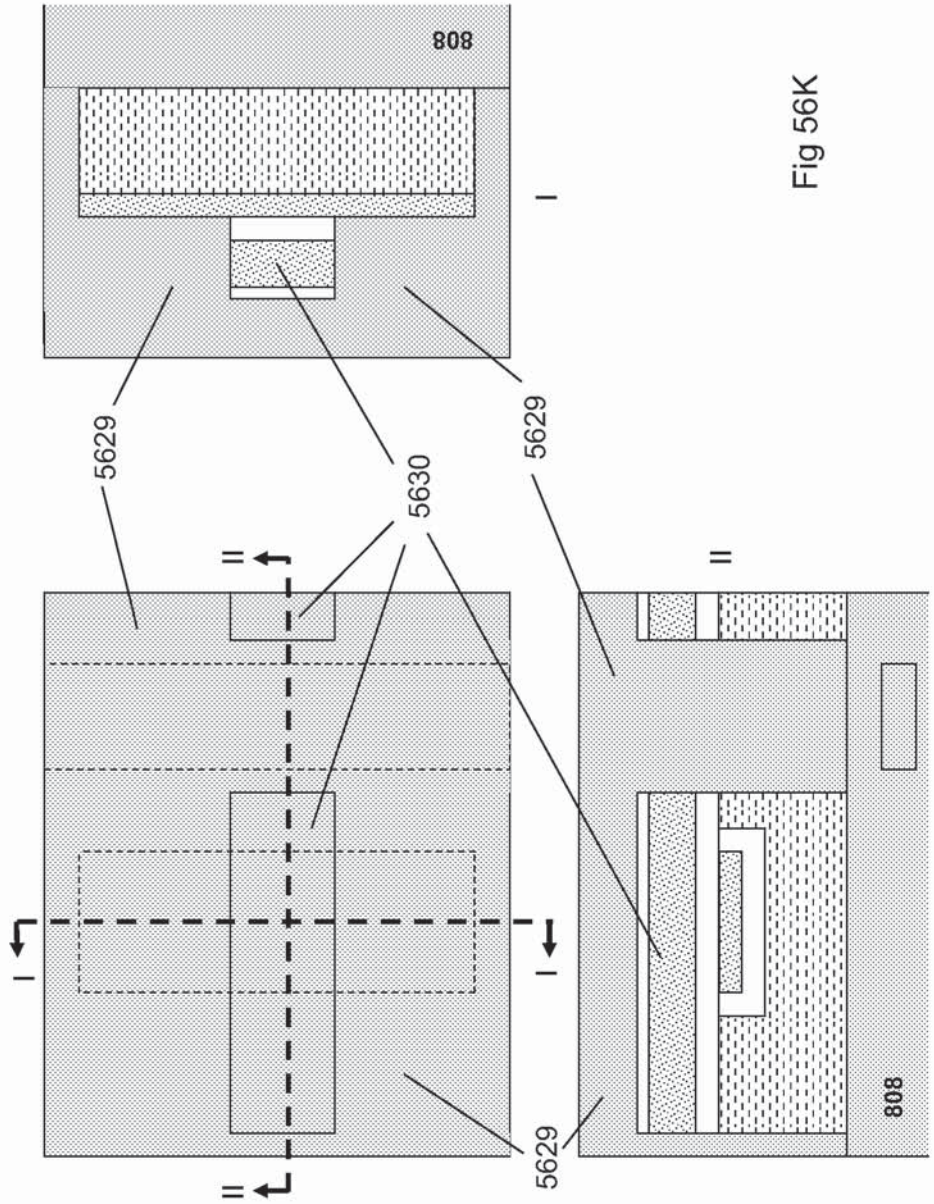


Fig 56K

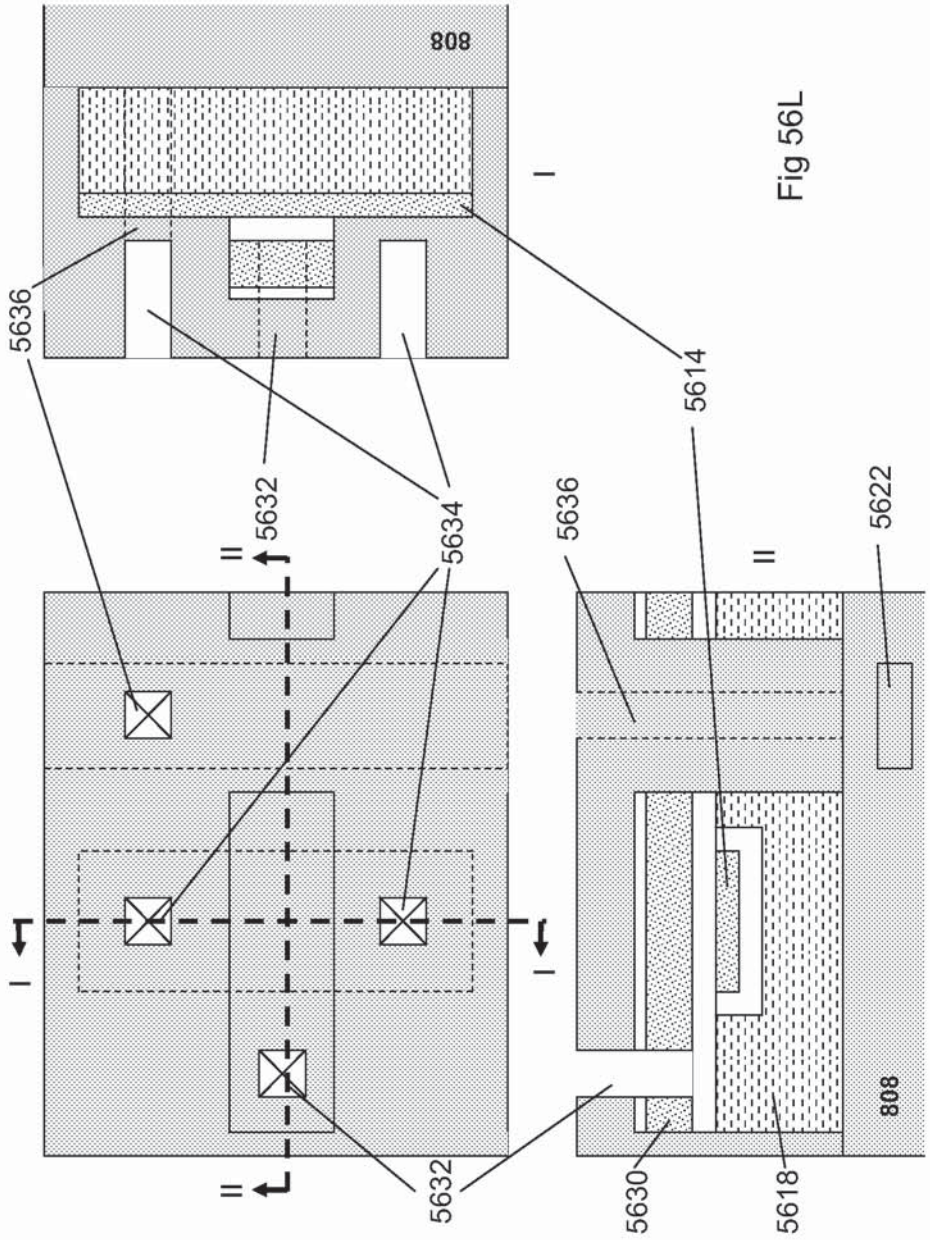


Fig 56L

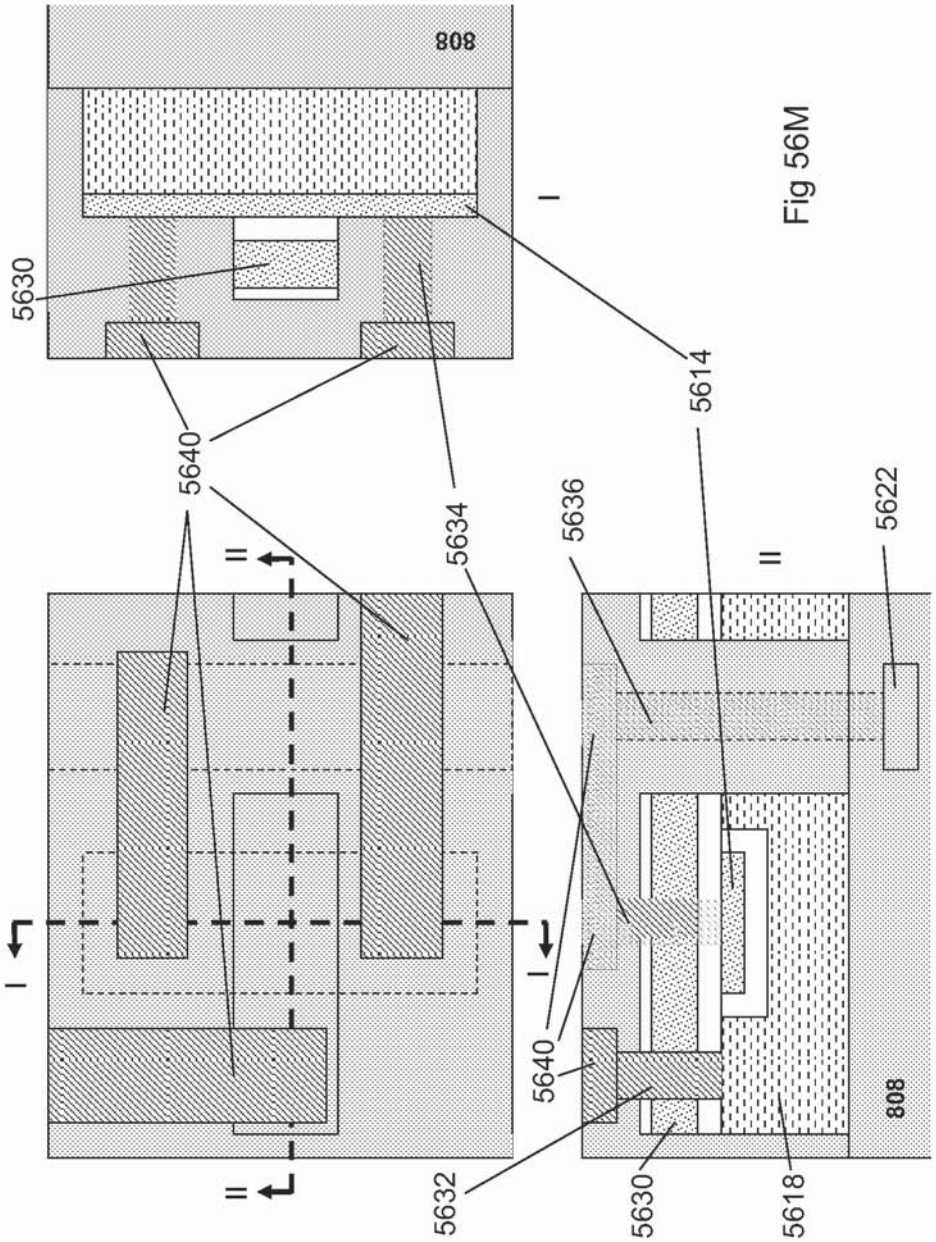


Fig 56M

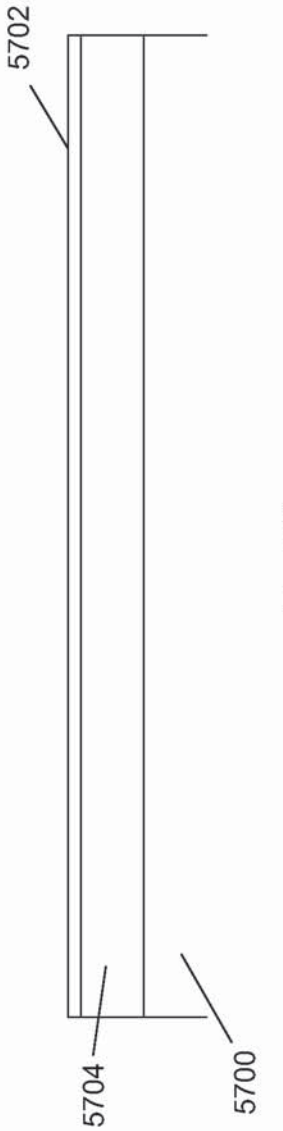


Fig 57A

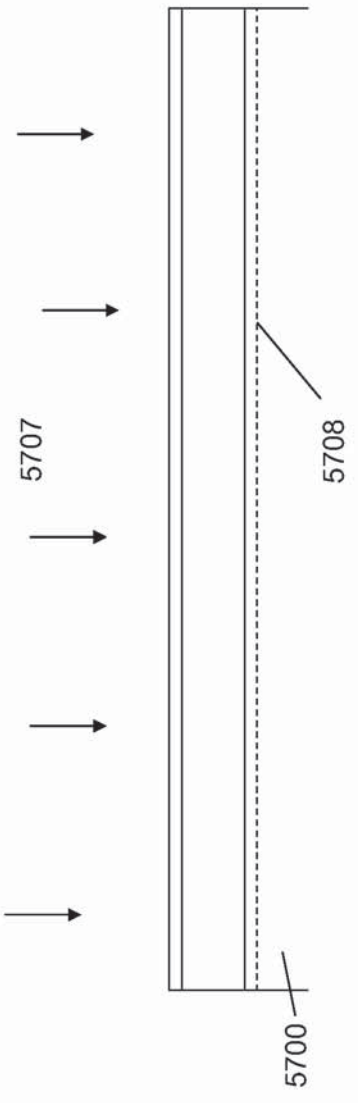


Fig 57B

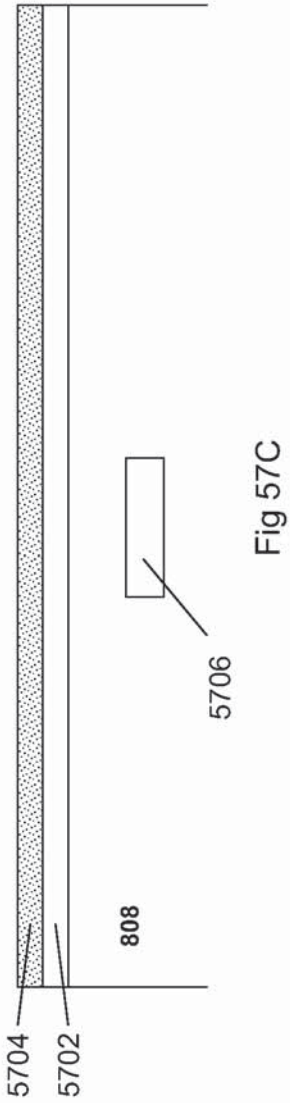


Fig 57C

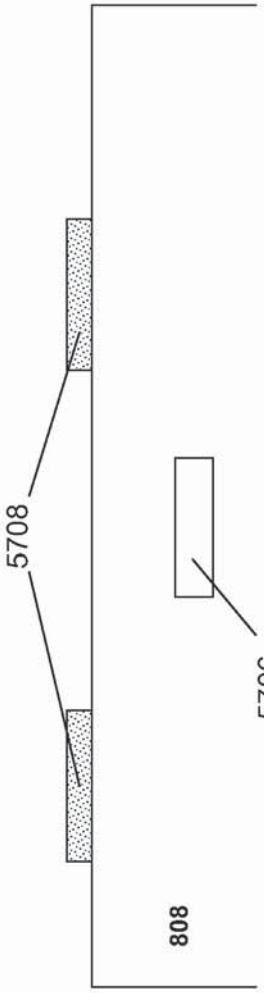


Fig 57D

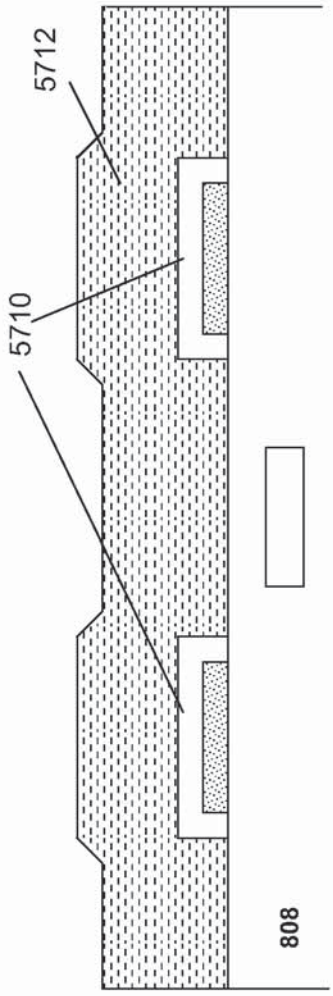


Fig 57E

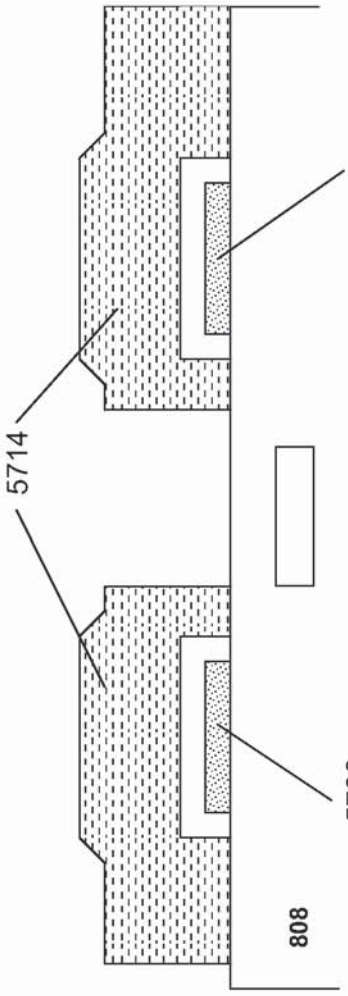


Fig 57F

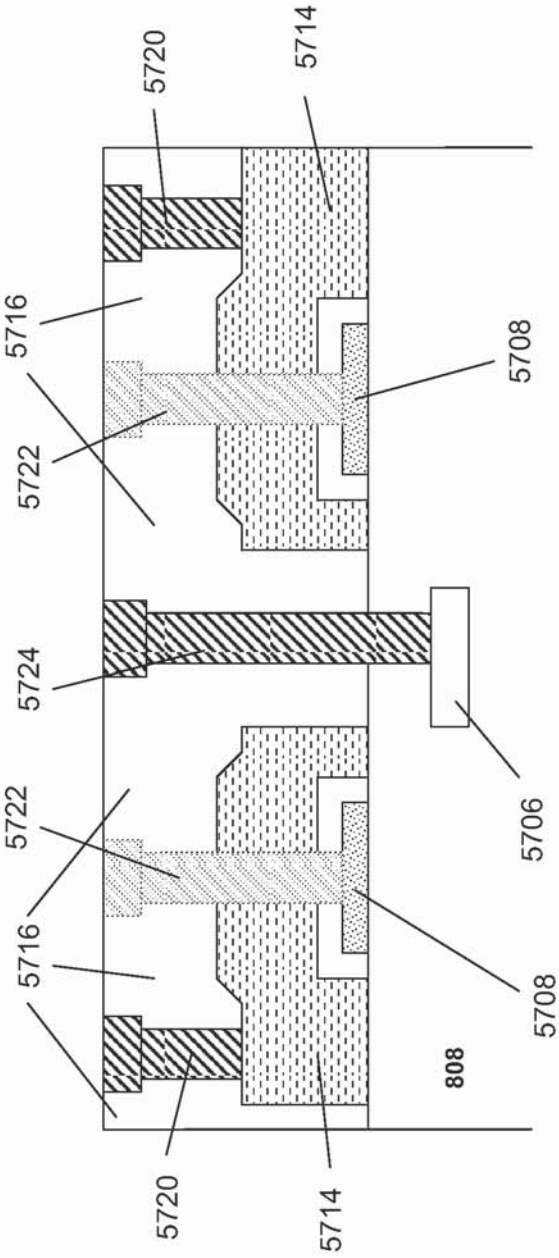

5720
5714
5716
5708
5722
5724
5722
5706
5716
5708
808
5720
5714

Fig 57G

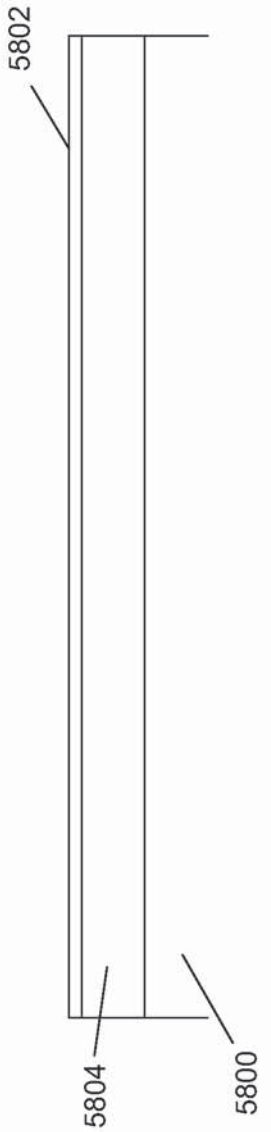


Fig 58A

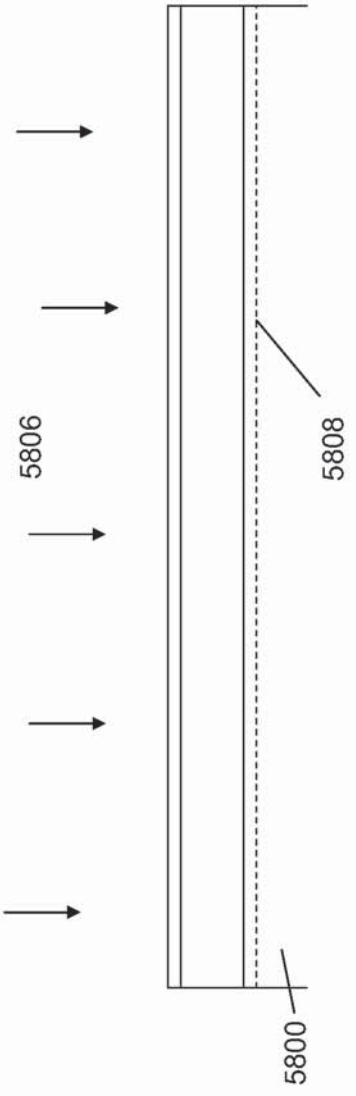


Fig 58B

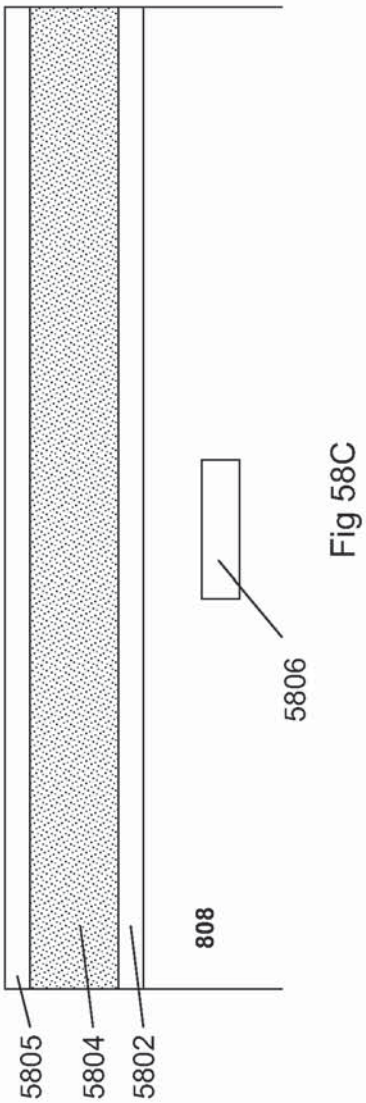


Fig 58C

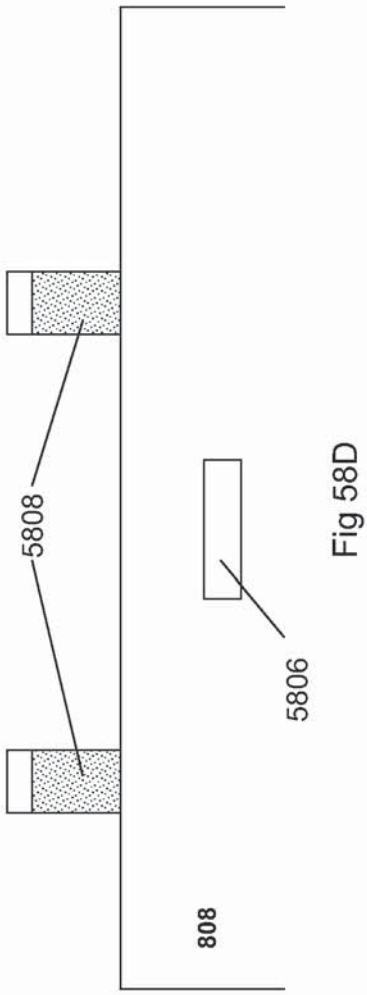


Fig 58D

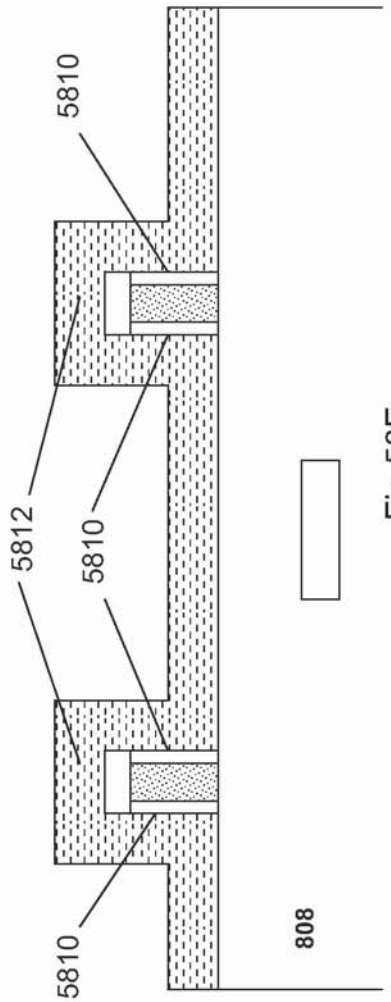


Fig 58E

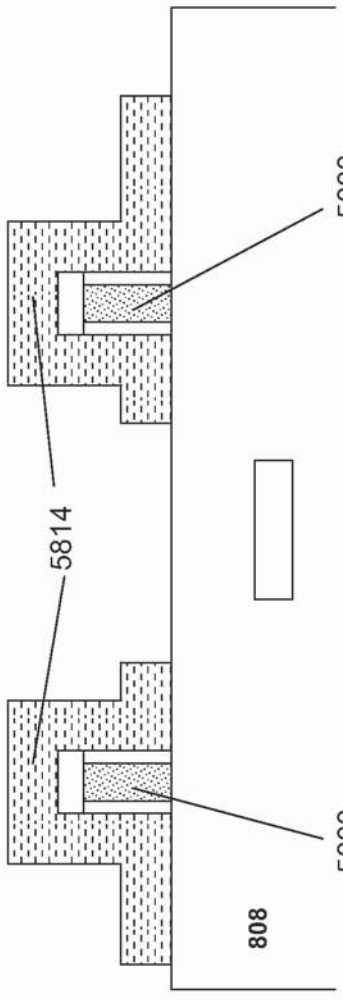


Fig 58F

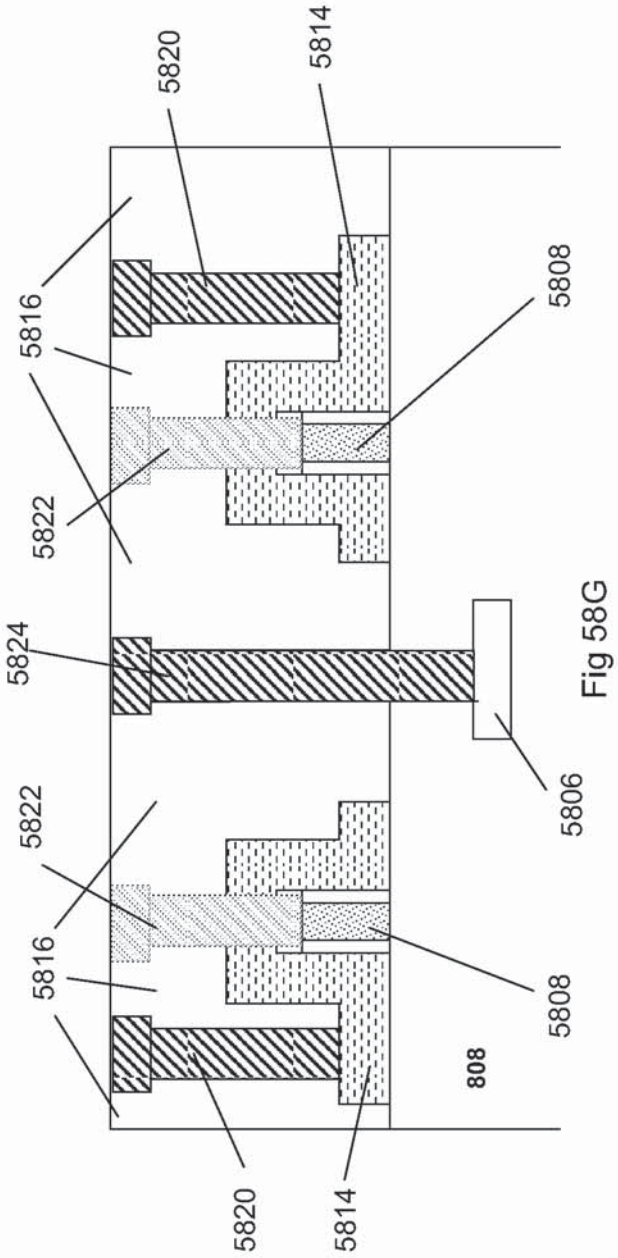
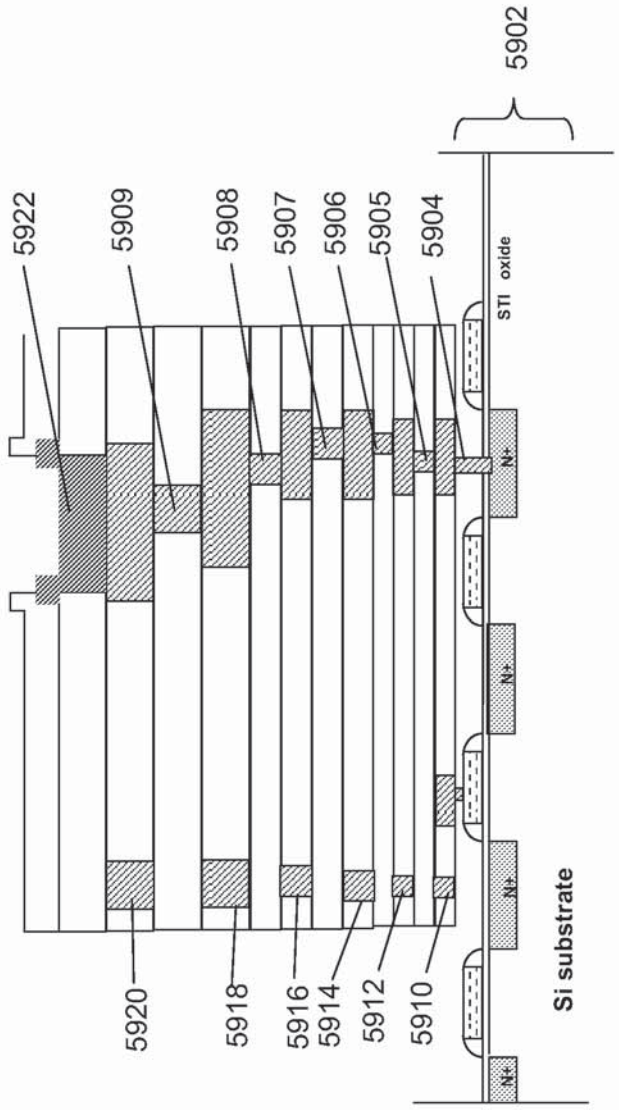

5820
5814
5816
5808
5822
5824
5822
5806
5816
5808
808
5820
5814

Fig 58G



Prior Art

Fig 59

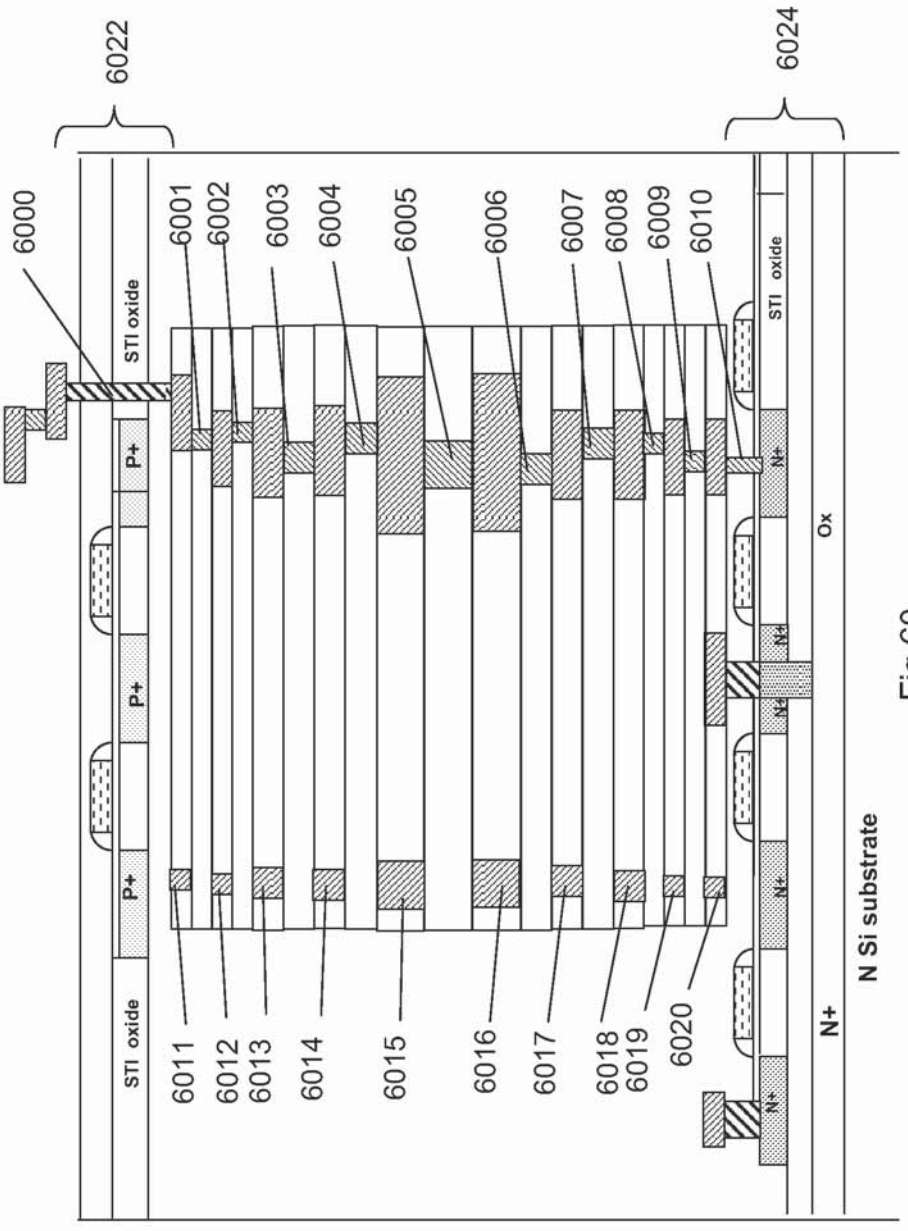

6022
6024
6000
6001
6002
6003
6004
6005
6006
6007
6008
6009
6010
6011
6012
6013
6014
6015
6016
6017
6018
6019
6020
STI oxide
STI oxide
STI oxide
P+
P+
P+
N+
N+
N+
N+
N+
Ox
N Si substrate

Fig 60

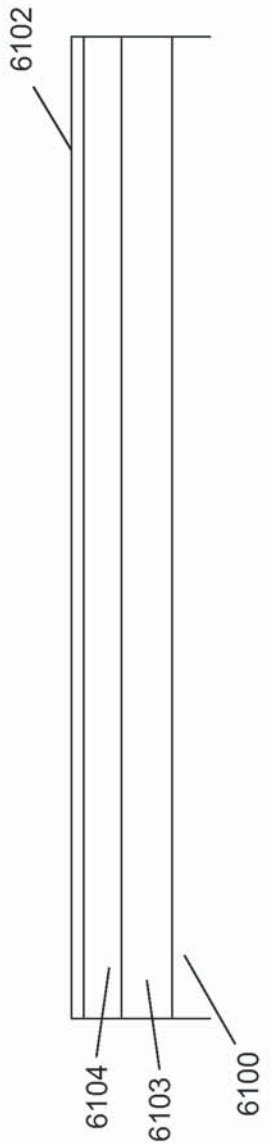


Fig 61A

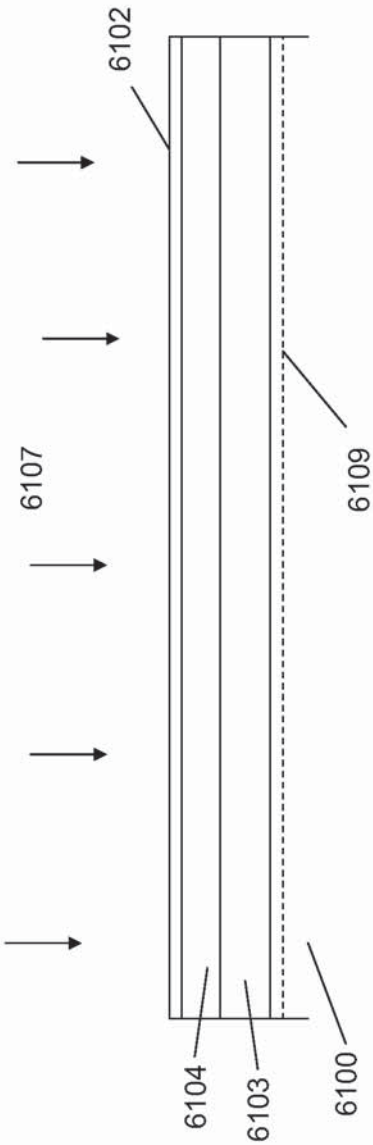


Fig 61B

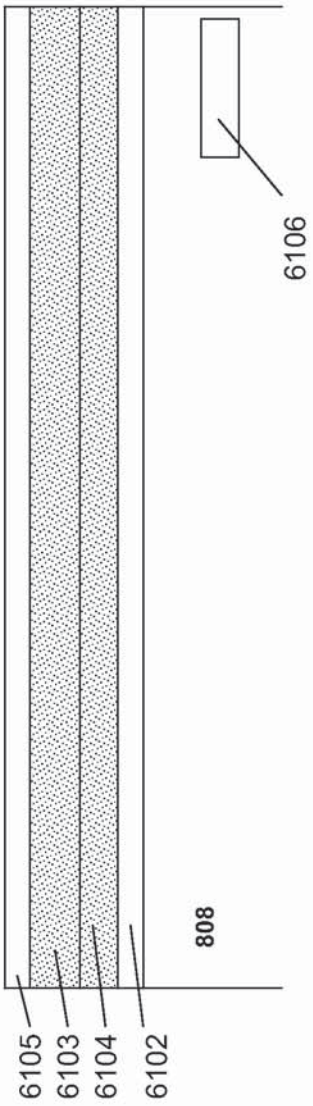


Fig 61C

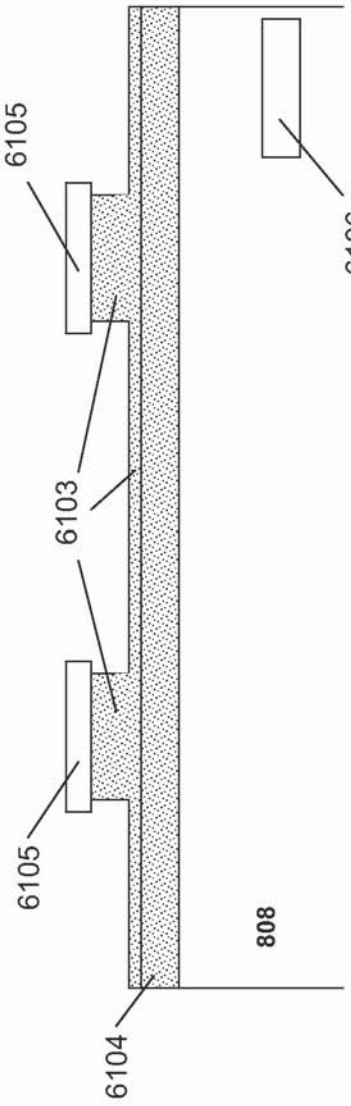


Fig 61D

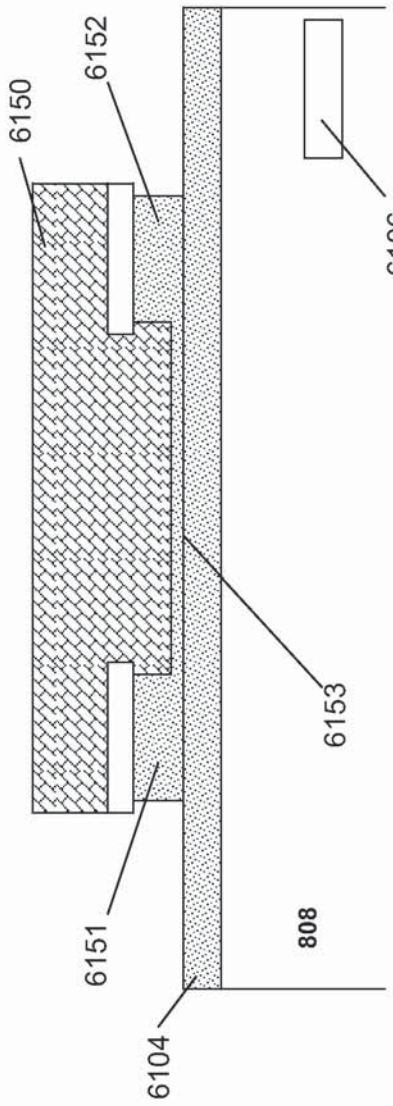


Fig 61E

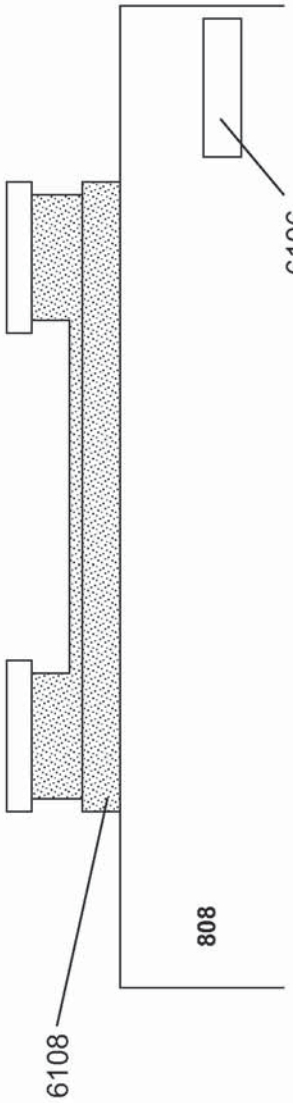


Fig 61F

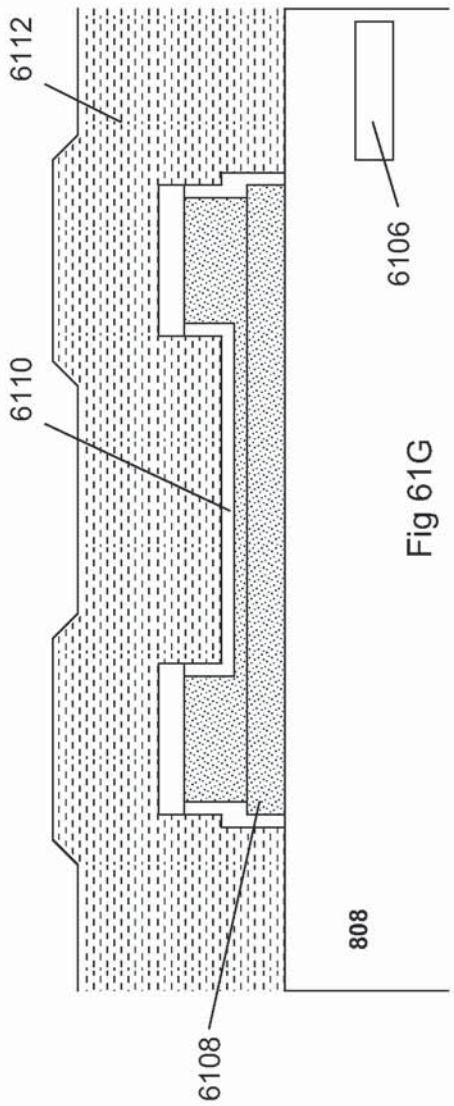


Fig 61G

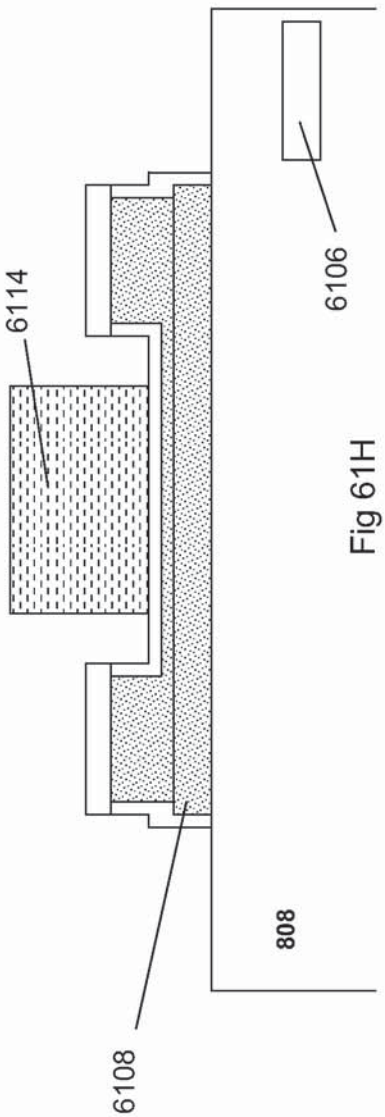


Fig 61H

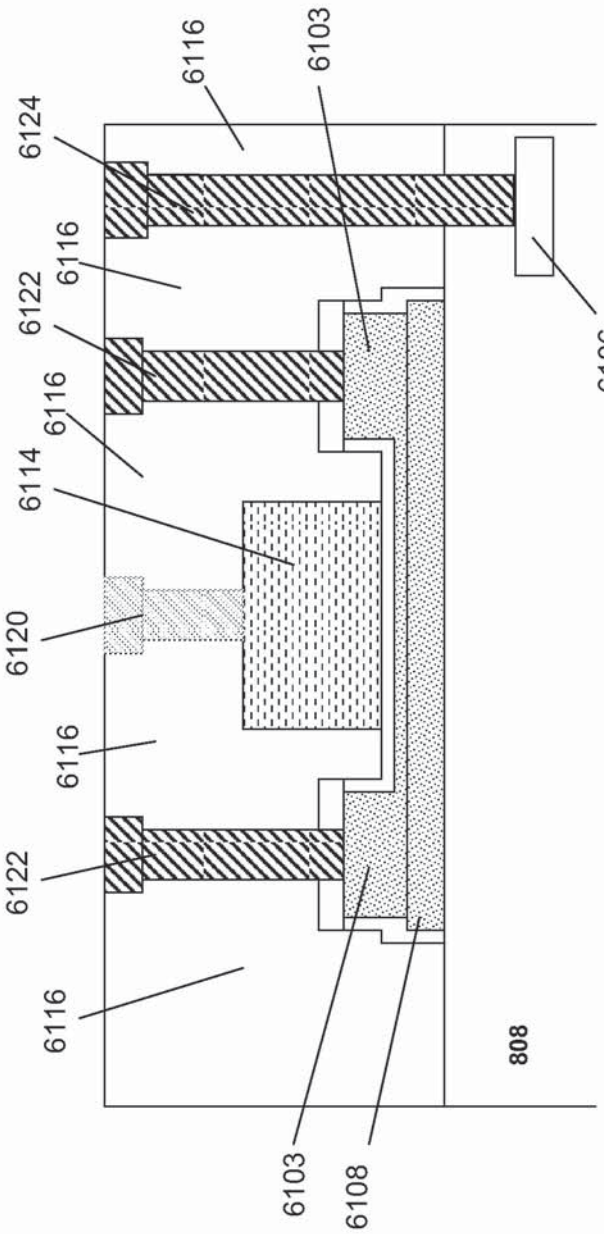

6116
6103
6124
6116
6122
6106
6116
6114
6120
6116
6122
6116
6103
6108
808

Fig 61I

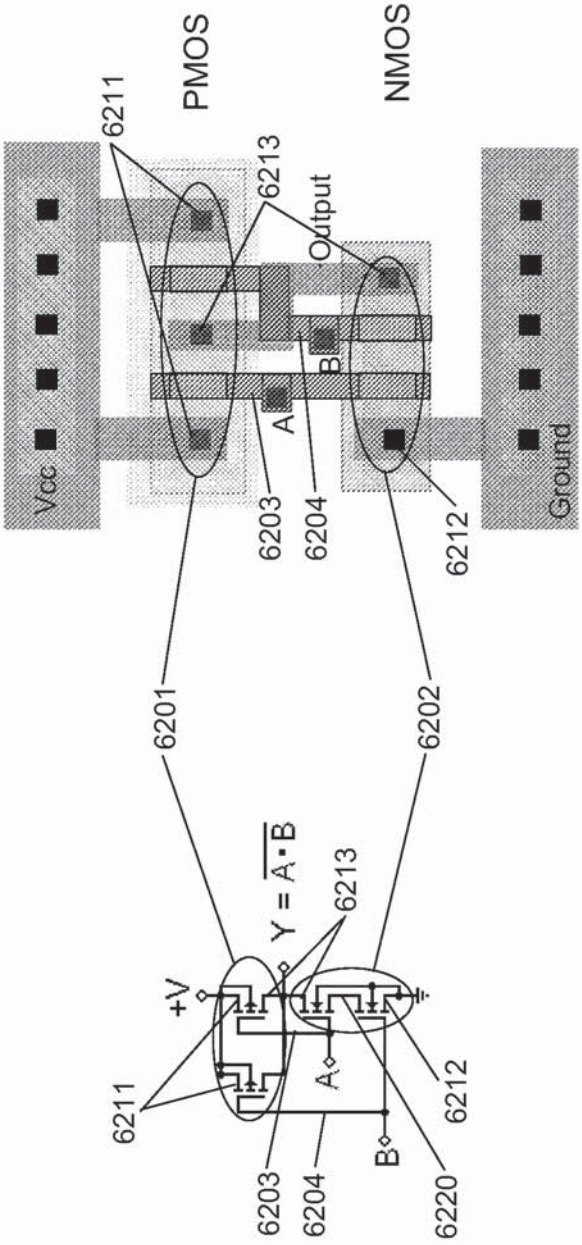

PMOS
NMOS
6211
6213
Output
Vcc
Ground
A
B
6203
6204
6212
6201
6202
$Y = \overline{A \cdot B}$
+V
6211
6203
6204
6220
6212
A
B

Fig 62A

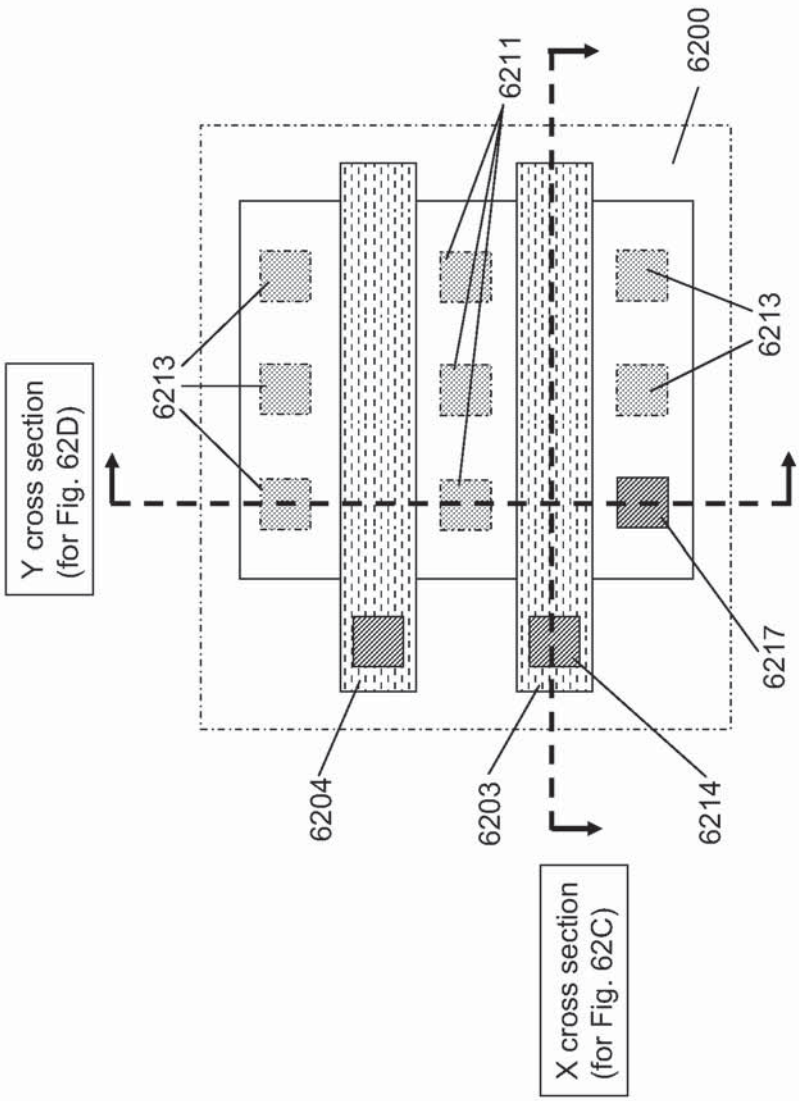

6200
6211
6213
6213
6217
6204
6203
6214
Y cross section
(for Fig. 62D)
X cross section
(for Fig. 62C)

Fig 62B

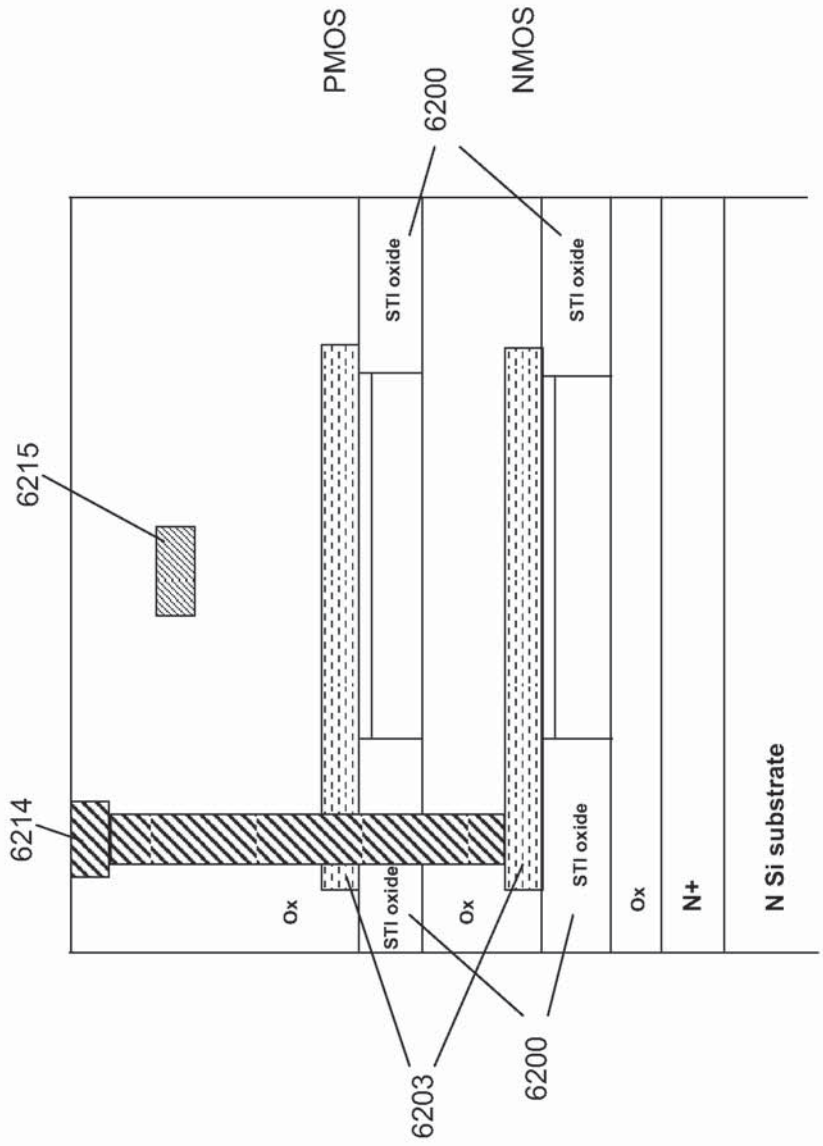

PMOS
NMOS
6200
STI oxide
STI oxide
6215
6214
STI oxide
Ox
STI oxide
Ox
Ox
N+
N Si substrate
6203
6200

Fig 62C

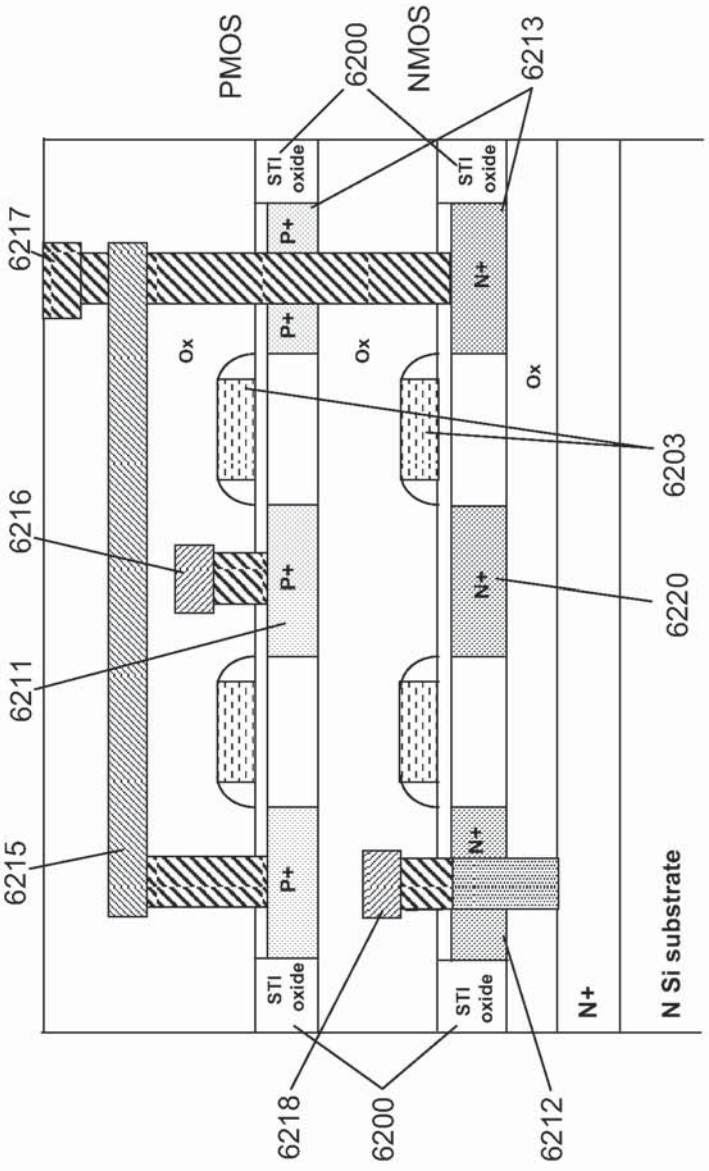

PMOS
6200
NMOS
6213
6217
6216
6211
6215
6203
6220
6218
6200
6212
STI oxide
P+
N+
Ox
N Si substrate

Fig 62D

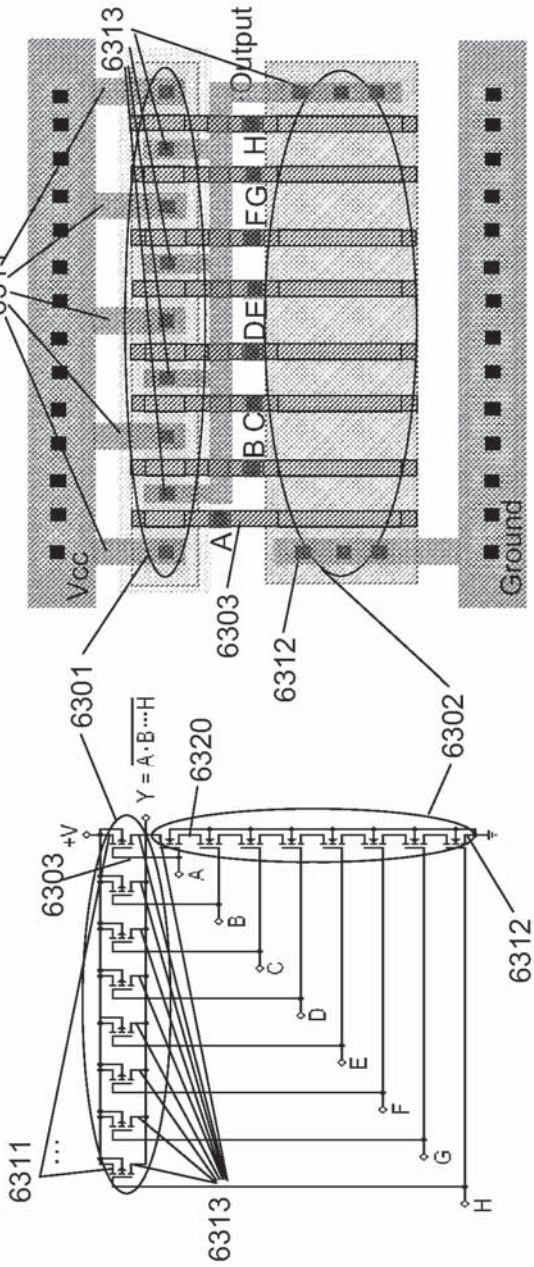

6313
Output
H
FG
DE
BC
A
6311
Vcc
Ground
6303
6312
6301
6302
6320
Y = A·B···H
+V
6303
A
B
C
D
E
F
G
H
6312
6311
6313

Fig 63A

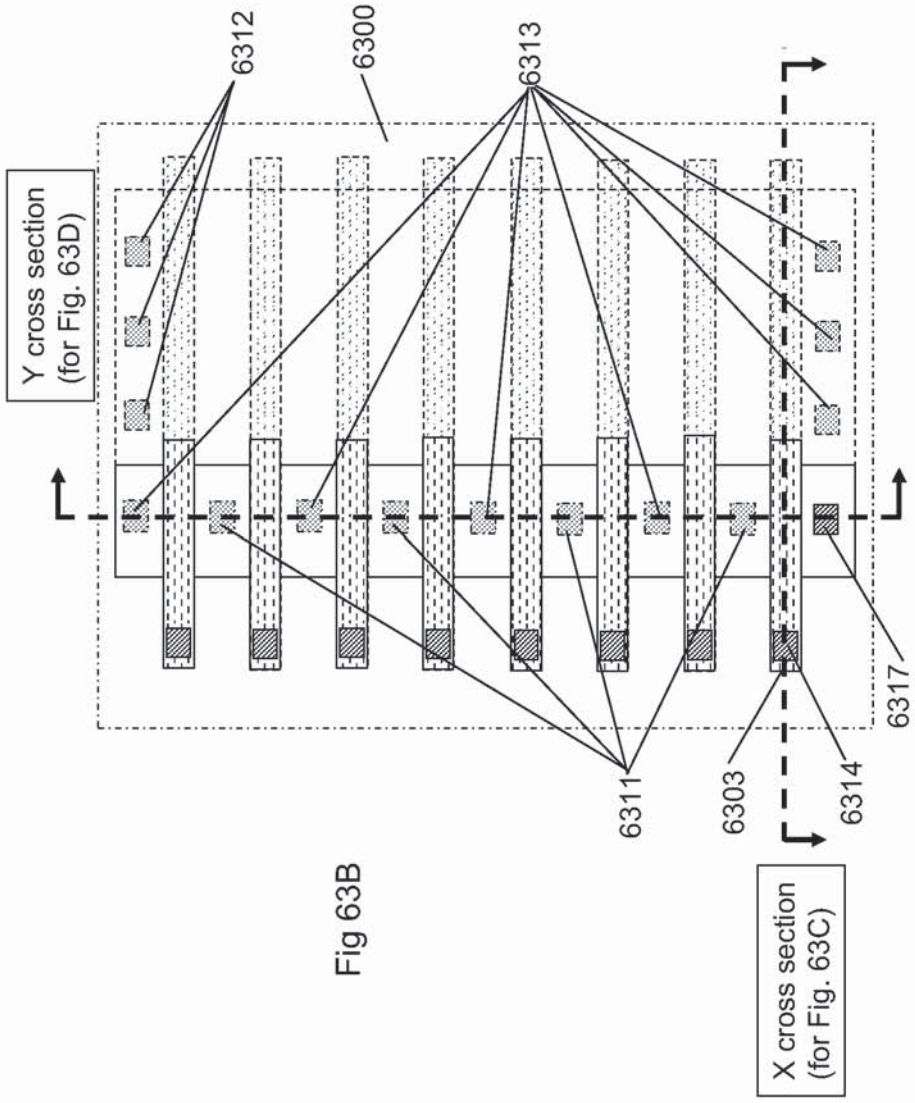

6312
6300
6313
Y cross section
(for Fig. 63D)
6311
6303
6314
6317
X cross section
(for Fig. 63C)

Fig 63B

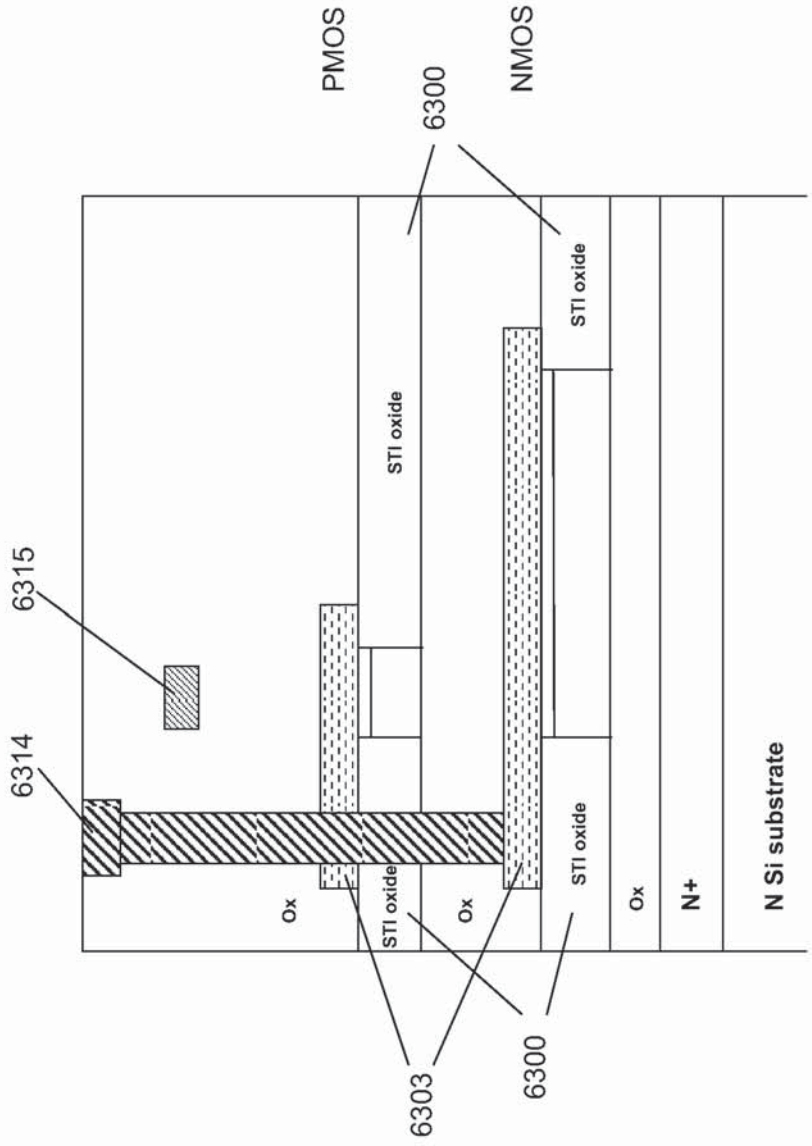

PMOS
NMOS
6300
STI oxide
STI oxide
6315
6314
STI oxide
STI oxide
Ox
Ox
Ox
N+
N Si substrate
6303
6300

Fig 63C

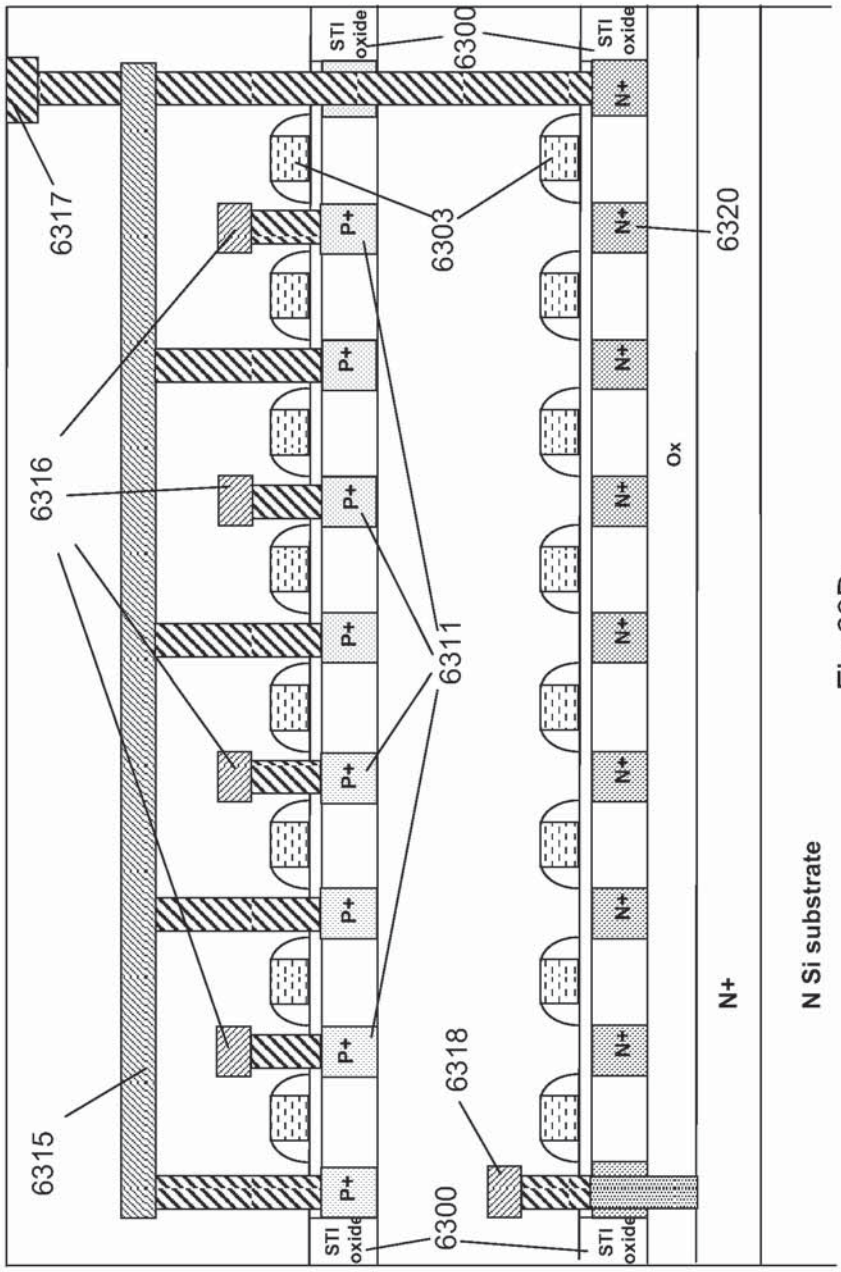

6317
6316
6315
6303
6311
6318
6300
6320
STI oxide
P+
N+
Ox
N+
N Si substrate

Fig 63D

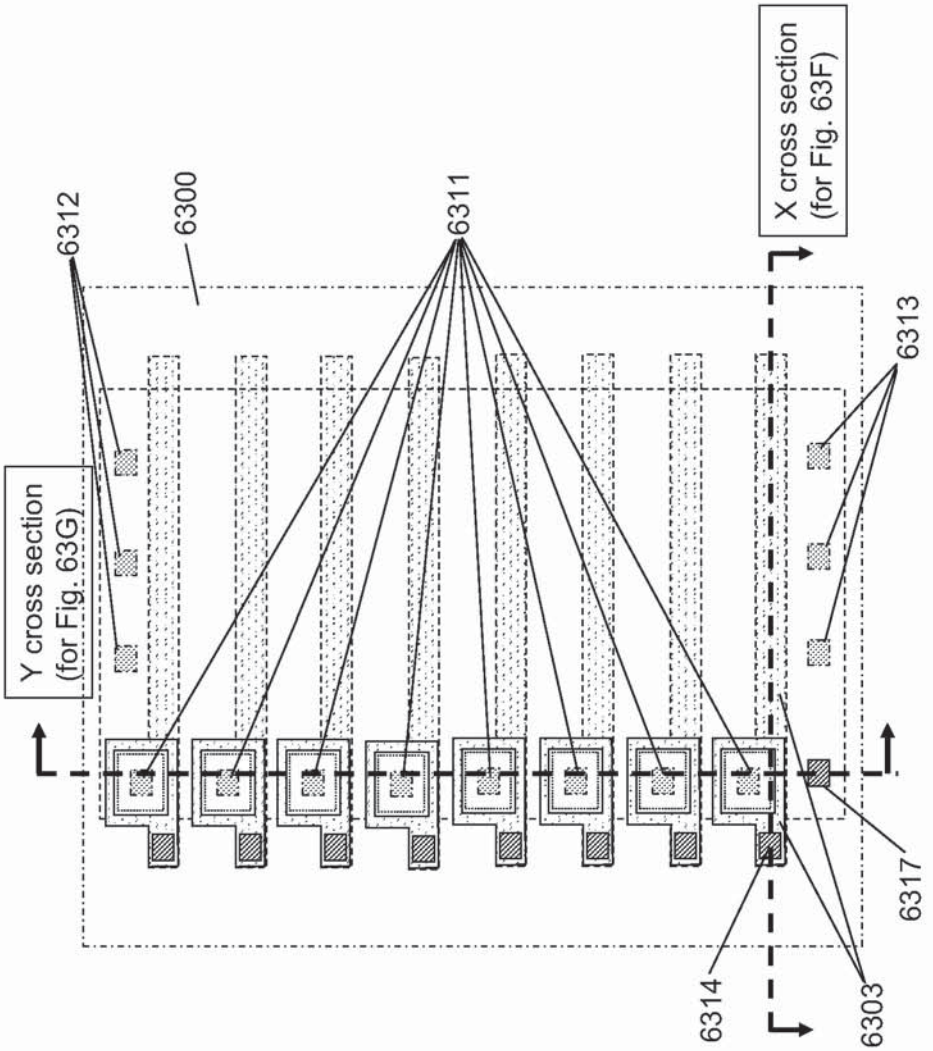

Y cross section
(for Fig. 63G)
X cross section
(for Fig. 63F)
6312
6300
6311
6313
6317
6314
6303

Fig 63E

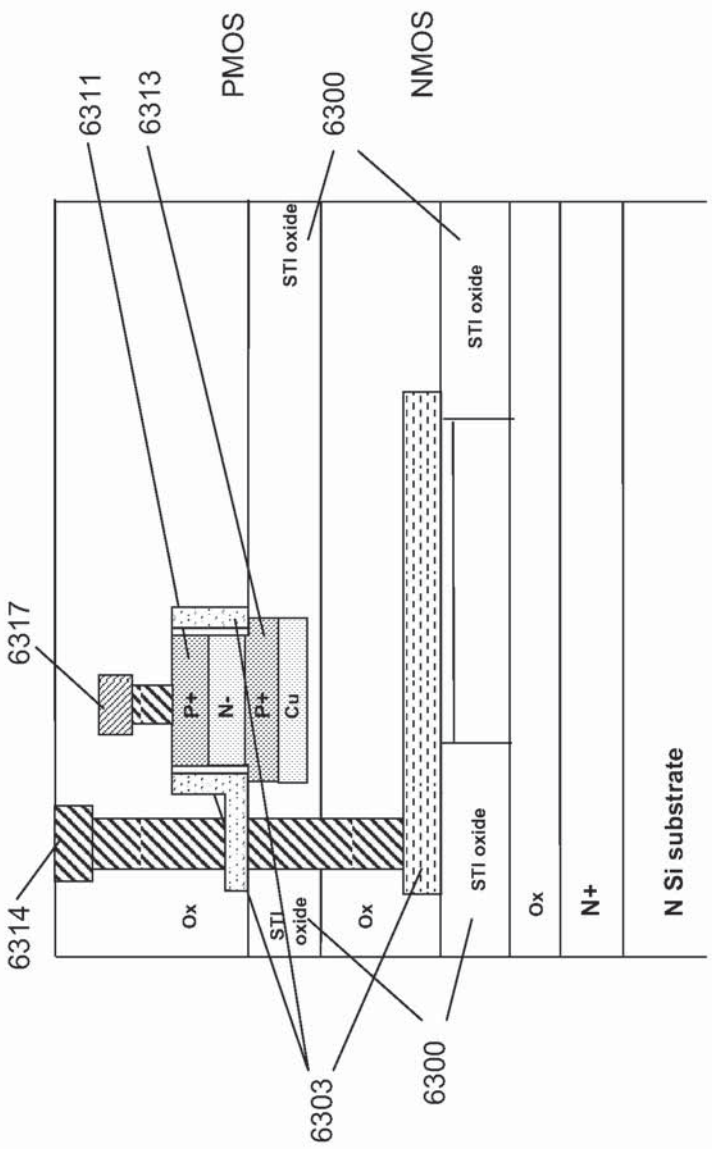

6311
6313
PMOS
6300
NMOS
6317
6314
6303
6300
STI oxide
STI oxide
STI oxide
STI oxide
P+
N-
P+
Cu
Ox
Ox
Ox
N+
N Si substrate

Fig 63F

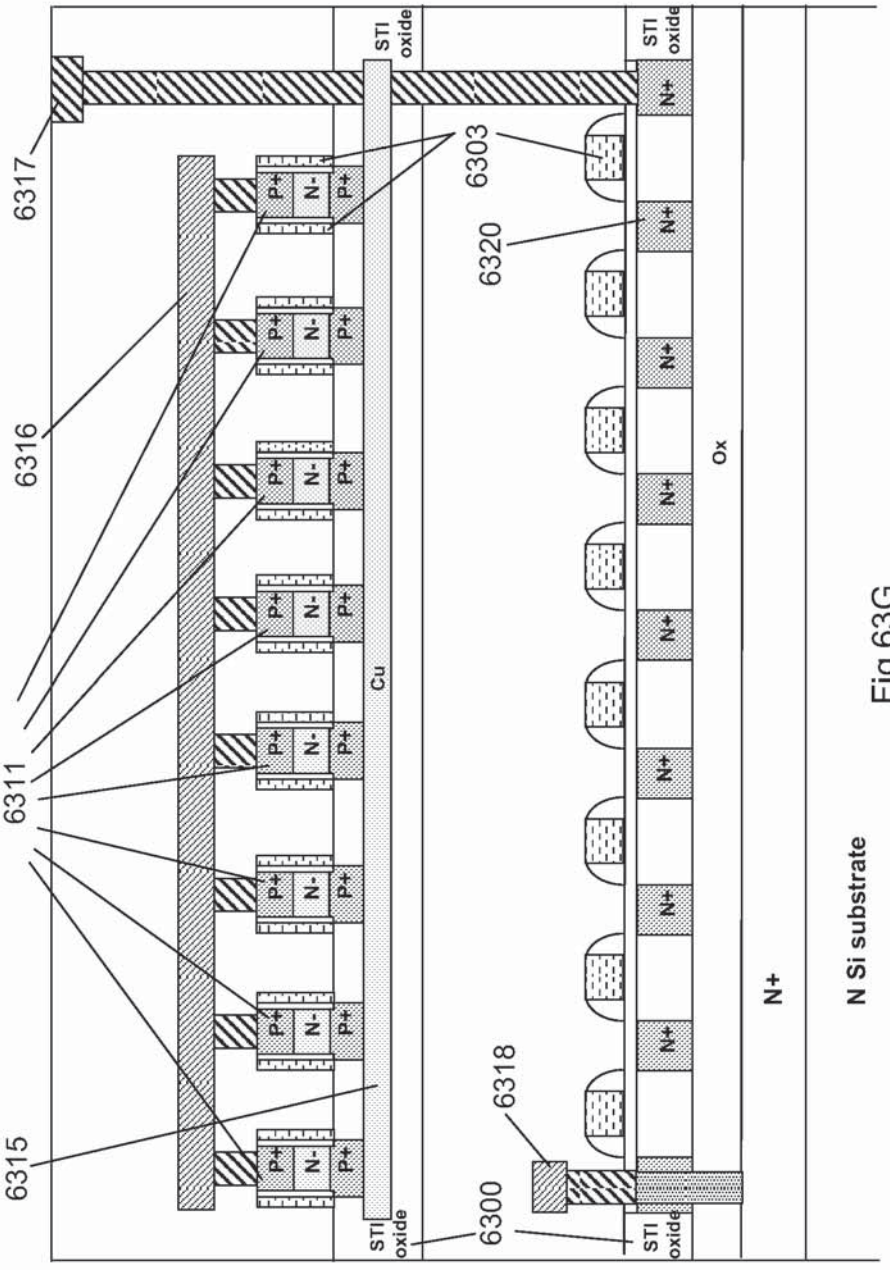

6317
6316
6311
6315
6303
6320
6318
6300
STI oxide
Cu
P+
N-
N+
Ox
N+
N Si substrate

Fig 63G

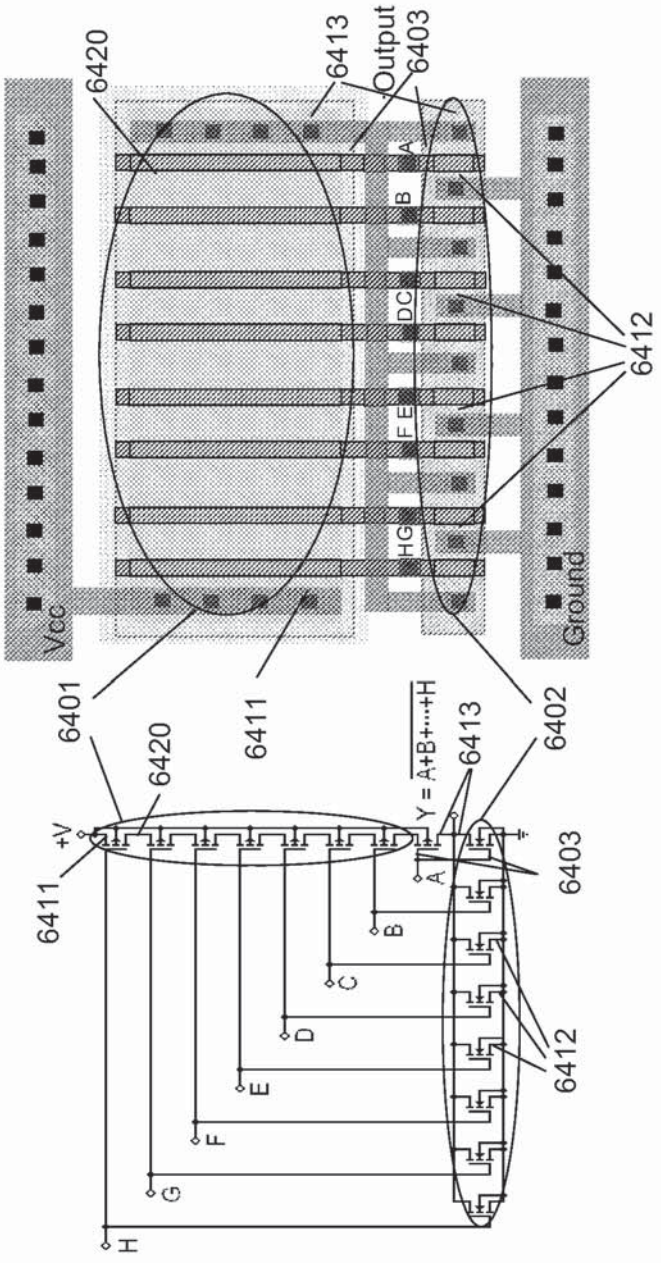

6420
6413
Output
6403
Vcc
Ground
A
B
DC
F E
HG
6412
6401
6411
6402
+V
$Y = \overline{A+B+\cdots+H}$
C
D
E
F
G
H

Fig 64A

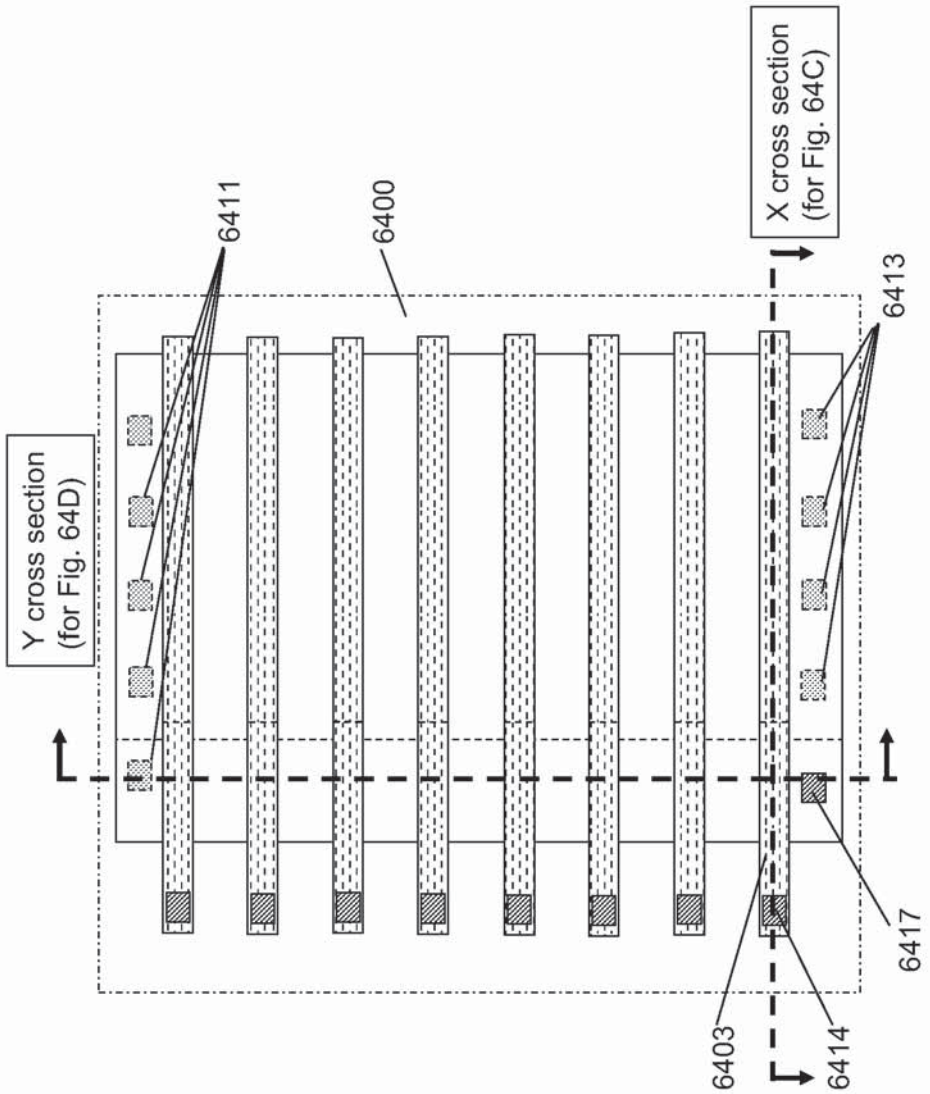

Y cross section
(for Fig. 64D)
6411
6400
X cross section
(for Fig. 64C)
6413
6417
6403
6414

Fig 64B

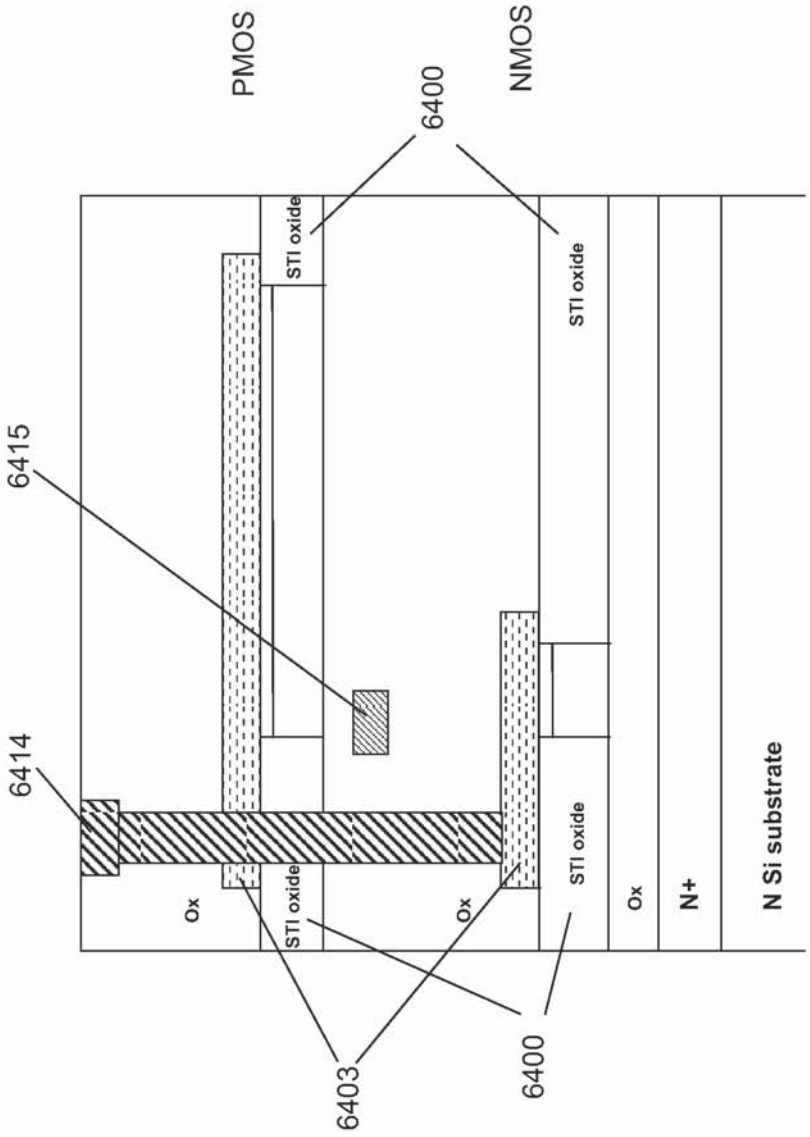

PMOS
NMOS
6400
STI oxide
STI oxide
6415
6414
Ox
STI oxide
Ox
STI oxide
Ox
N+
N Si substrate
6403
6400

Fig 64C

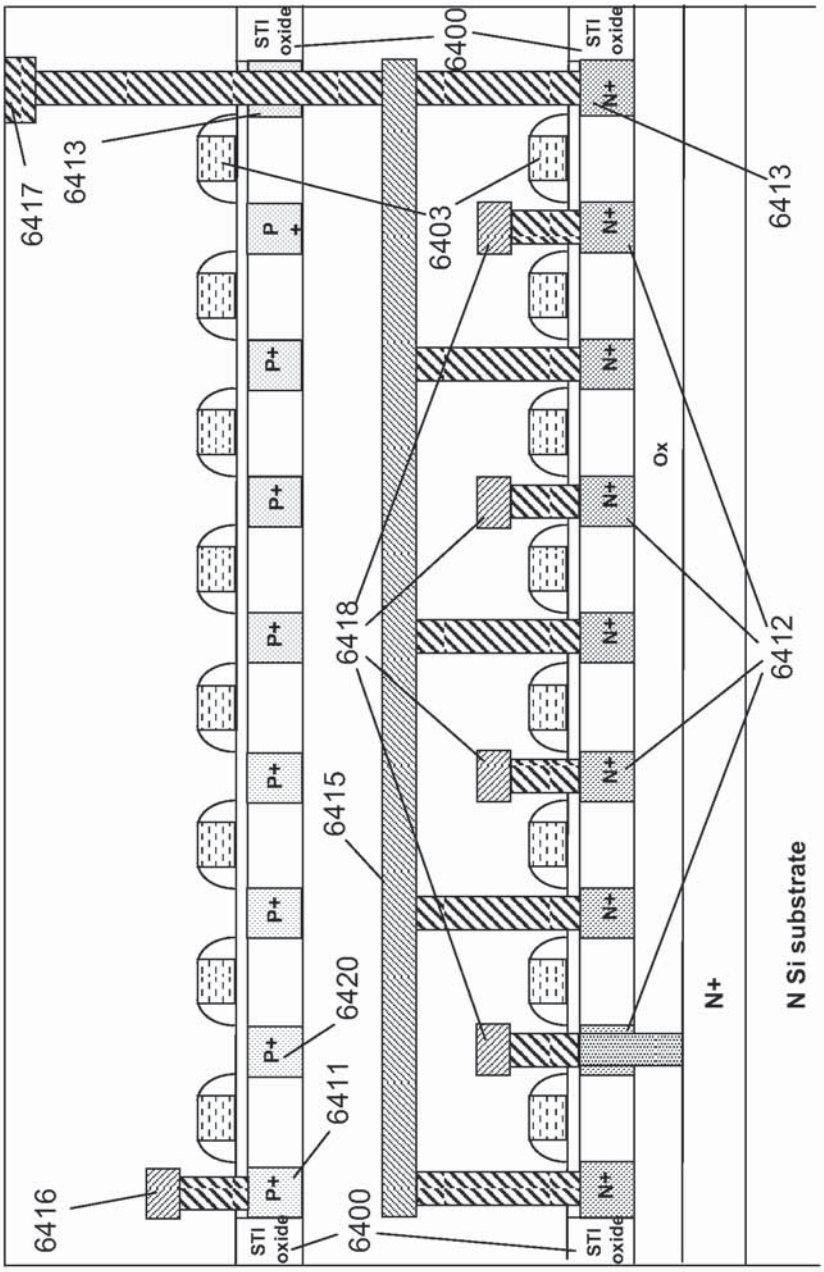
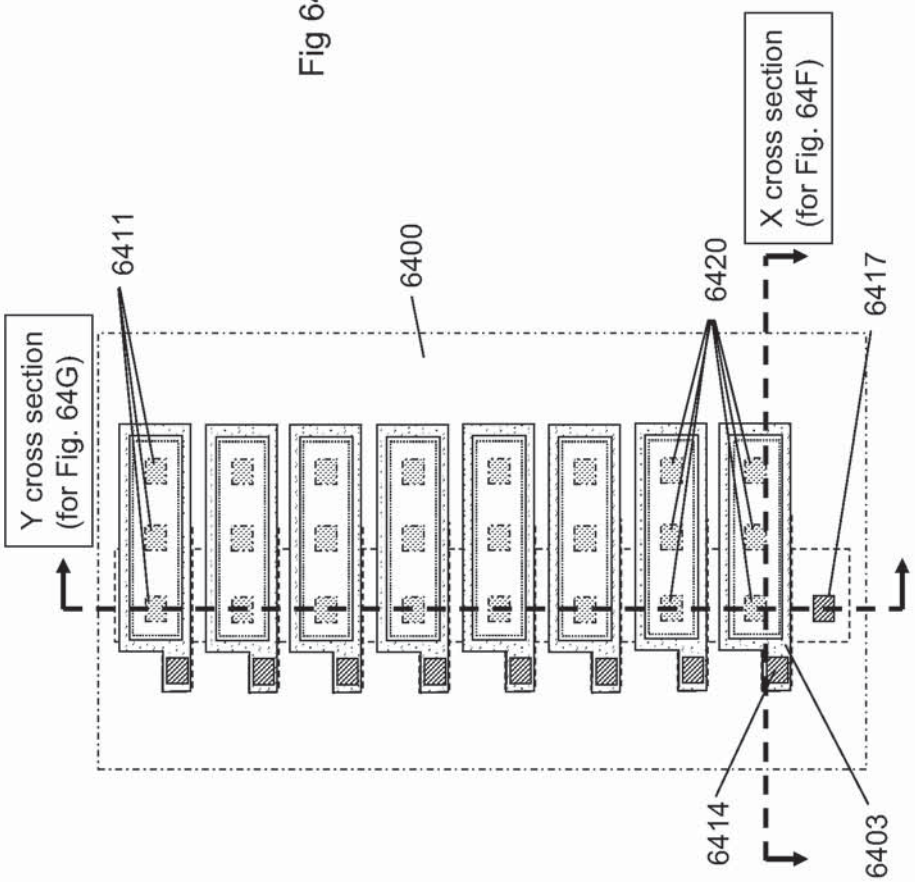

STI oxide
6400
6417
6413
6403
P+
N+
6418
6415
6420
6411
6416
6412
Ox
N+
N Si substrate

Fig 64D

Fig 64E


Y cross section
(for Fig. 64G)
6411
6400
6420
X cross section
(for Fig. 64F)
6417
6414
6403

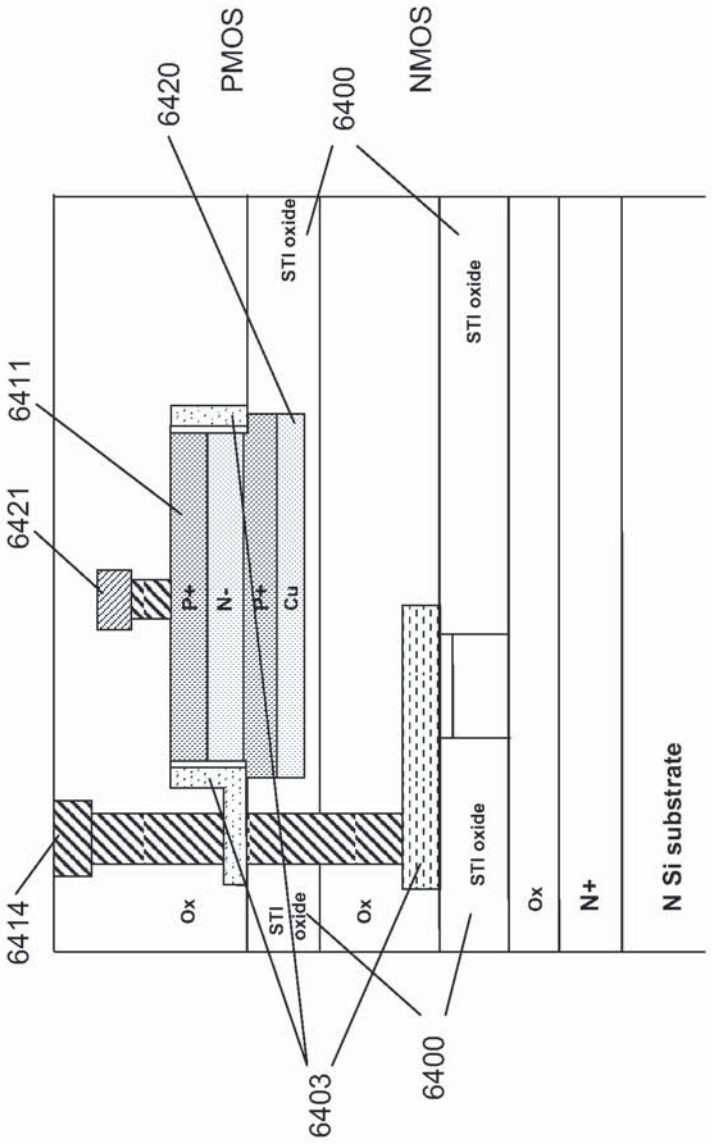

6420
PMOS
6400
NMOS
6411
6421
6414
6403
6400
STI oxide
STI oxide
P+
N-
P+
Cu
Ox
STI oxide
Ox
STI oxide
Ox
N+
N Si substrate

Fig 64F

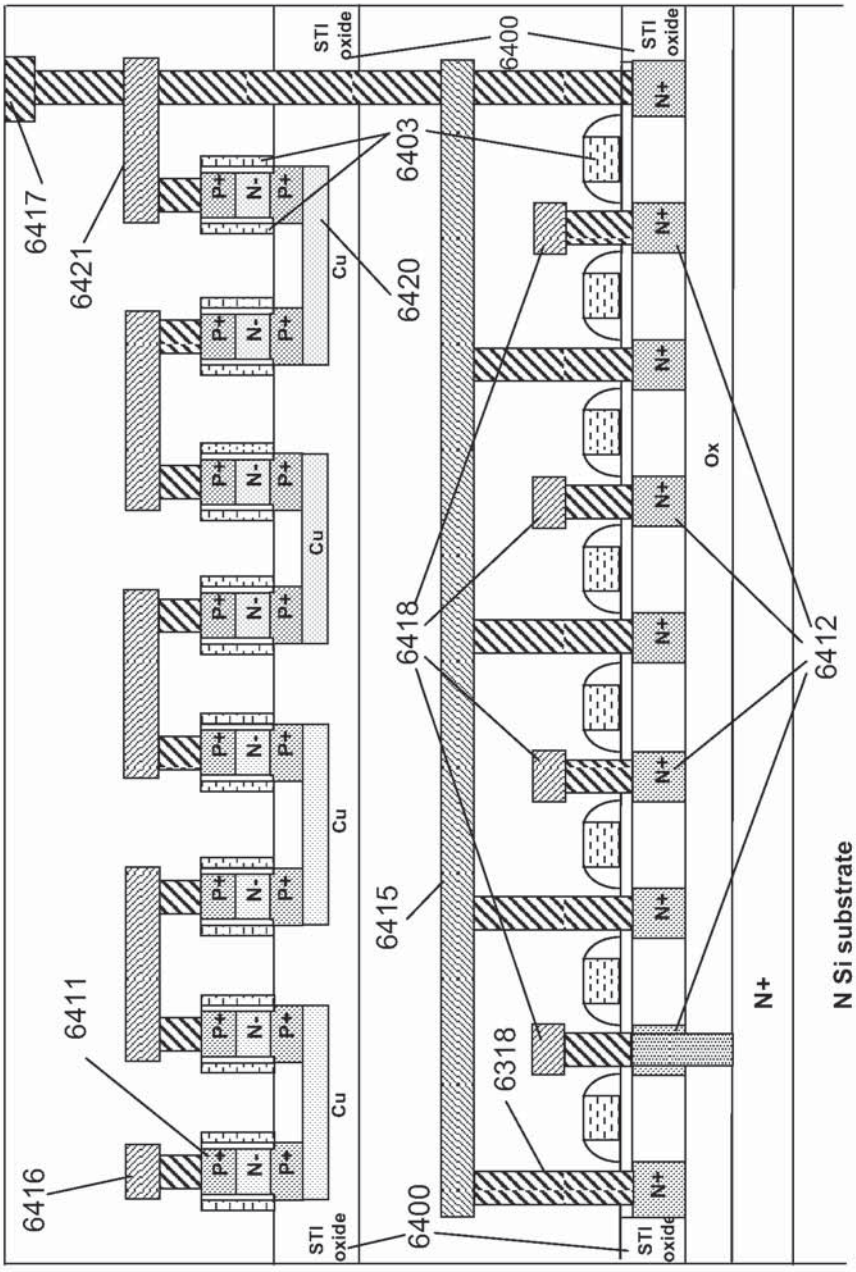

6417
6421
6411
6416
6403
6420
6418
6415
6400
6318
6412
STI oxide
Cu
P+
N-
N+
Ox
N+
N Si substrate

Fig 64G

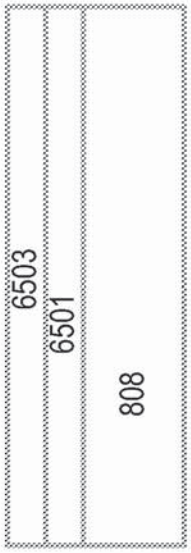


Fig. 65A

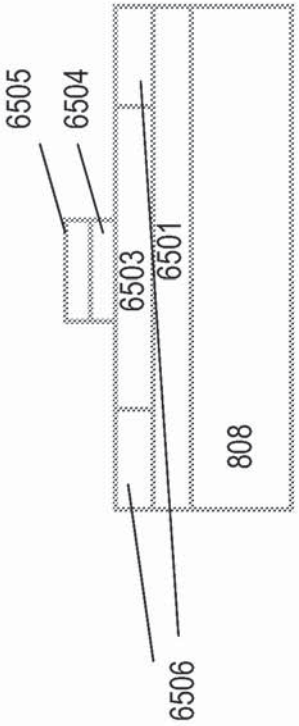


Fig. 65B

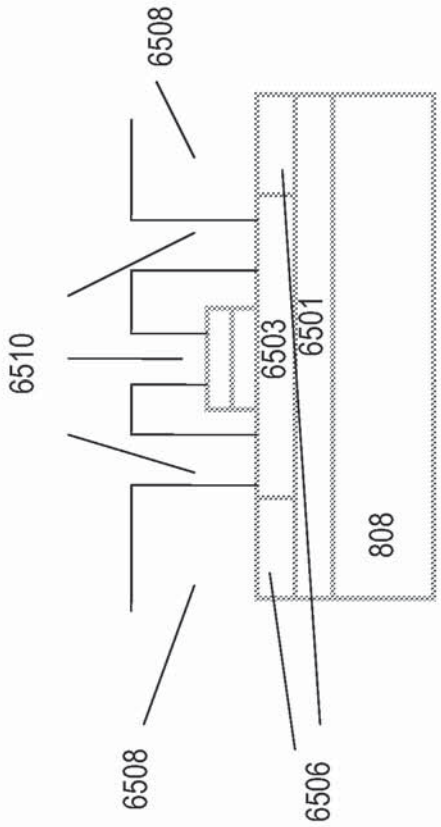
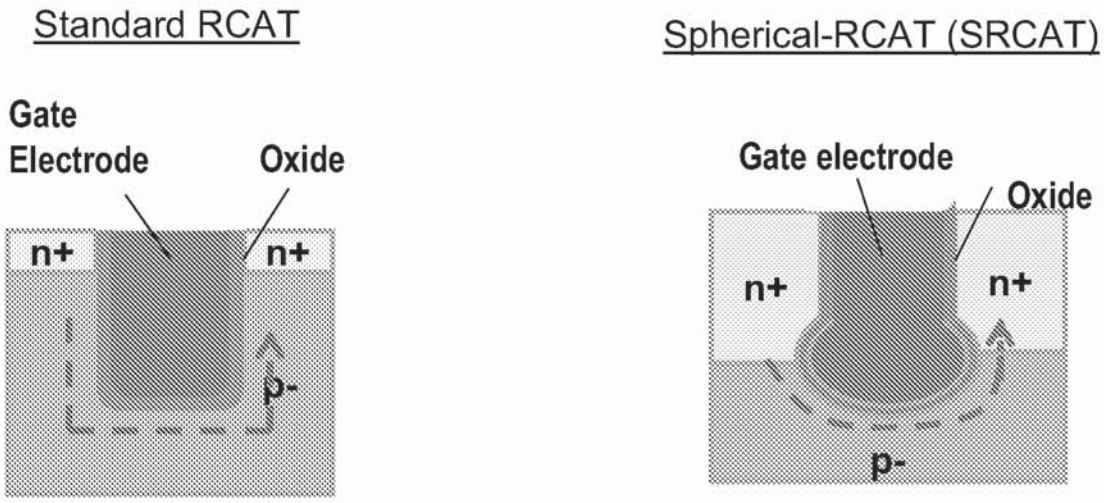


Fig. 65C



Current flow in two dimensional plane, indicated by - - ->

Prior Art

Fig. 66



Figure 67A

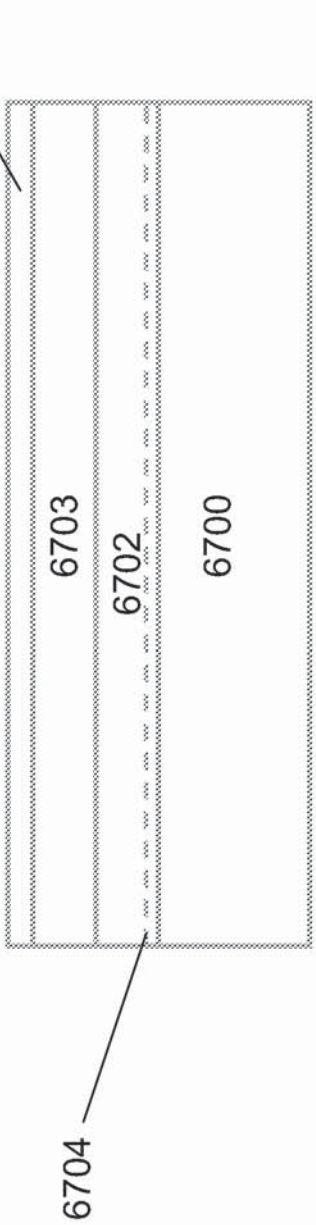


Figure 67B



Figure 67C

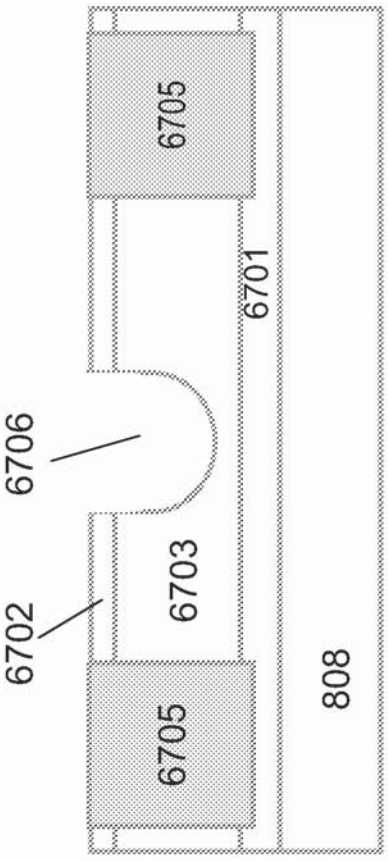


Figure 67D

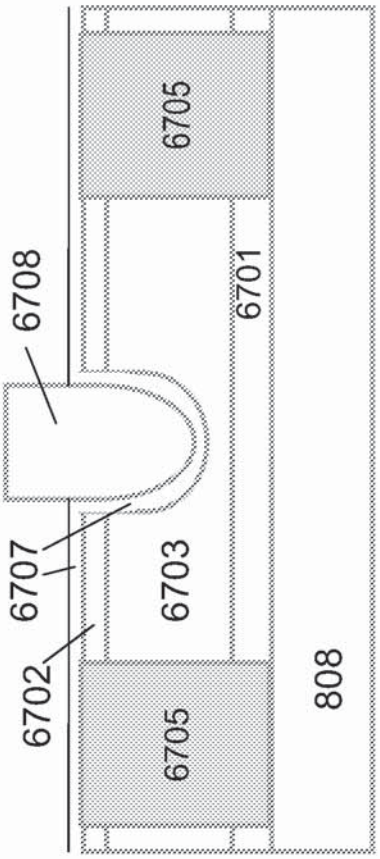


Figure 67E

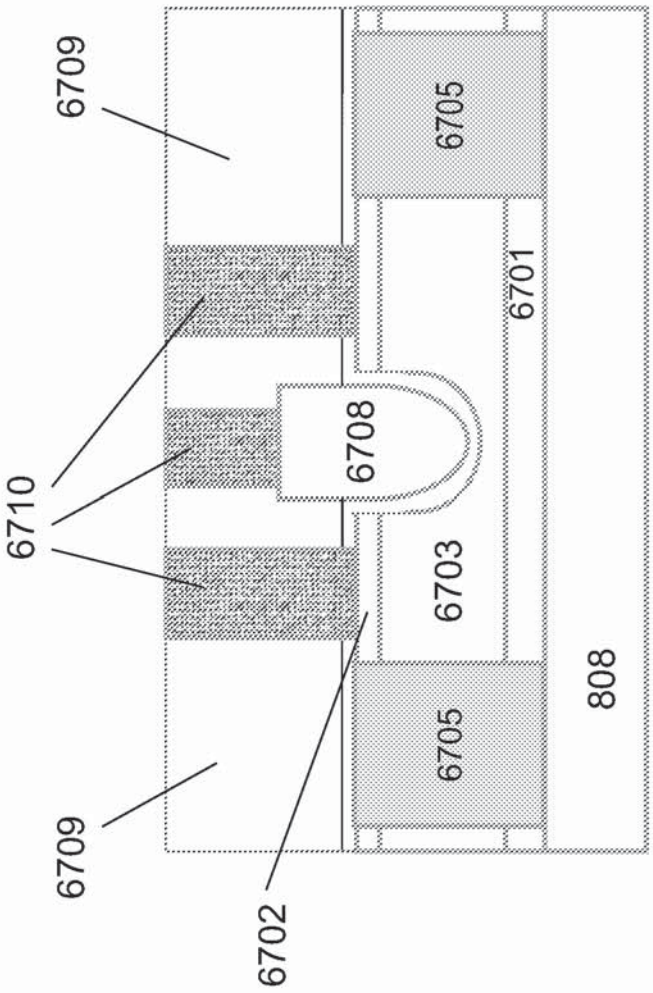


Figure 67F



Figure 68A

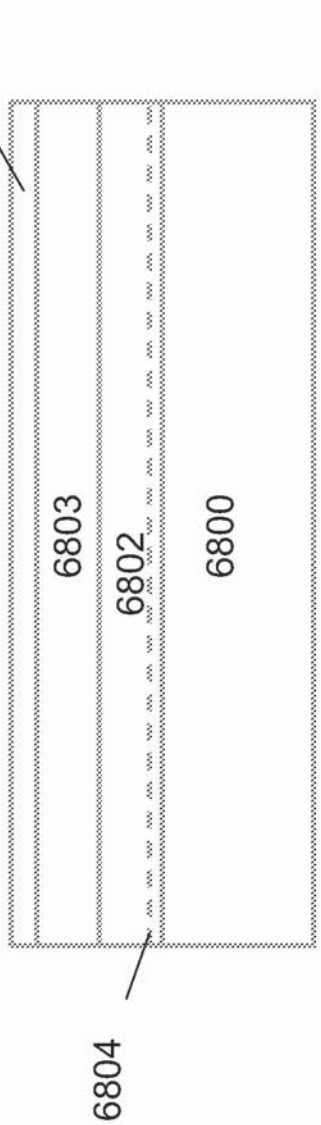


Figure 68B



Figure 68C

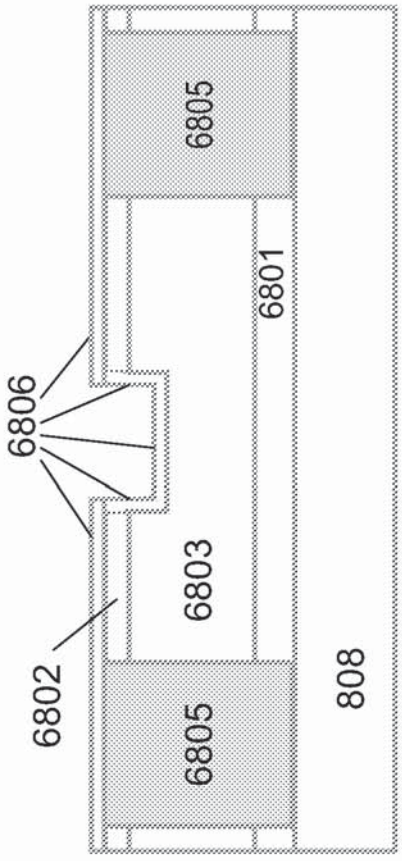


Figure 68D

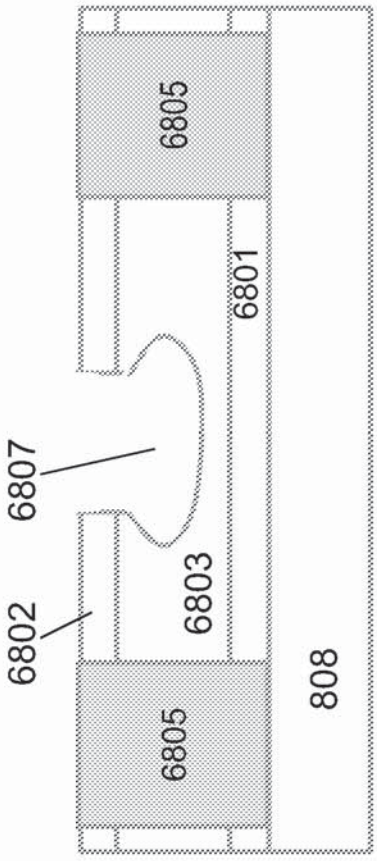


Figure 68E

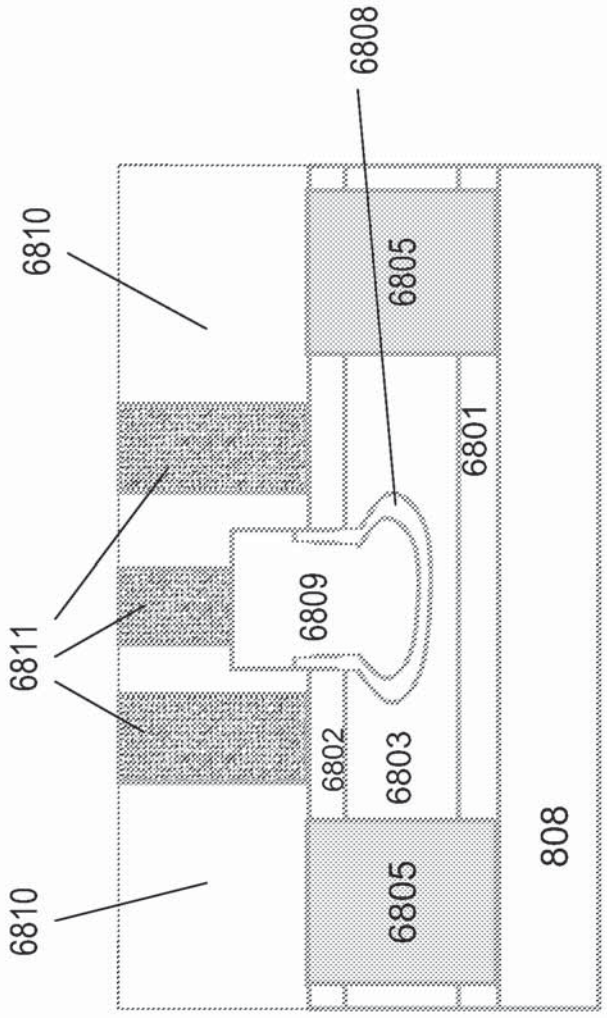


Figure 68F

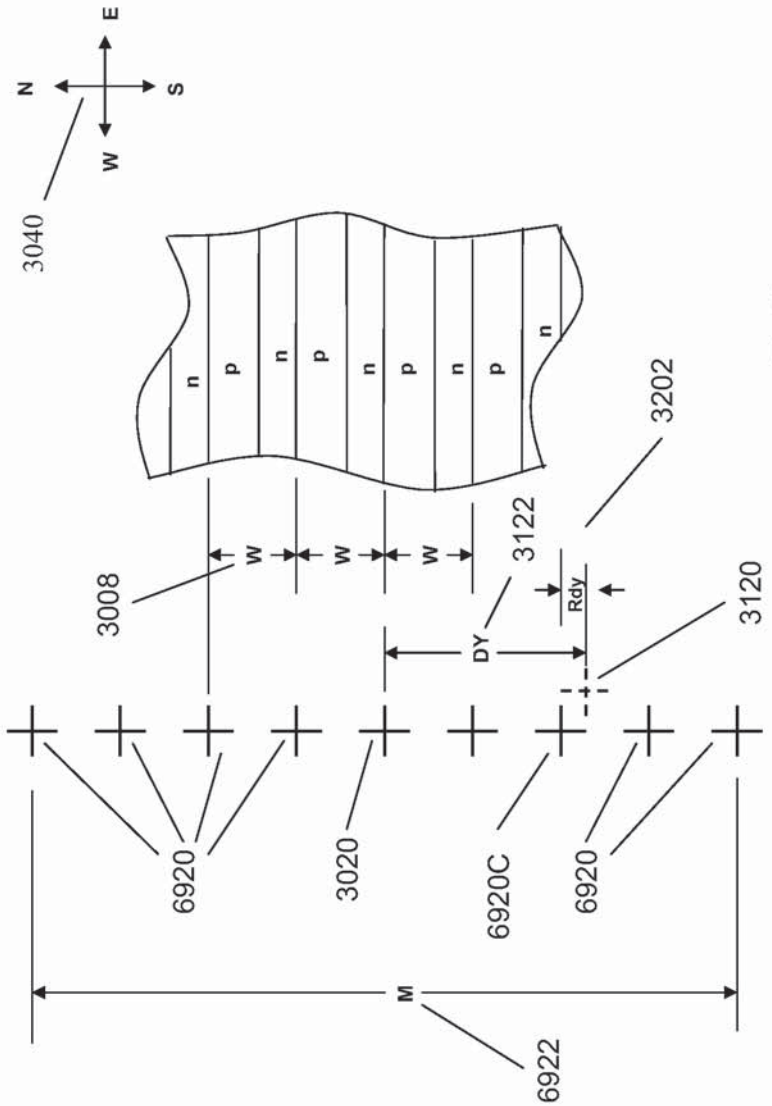
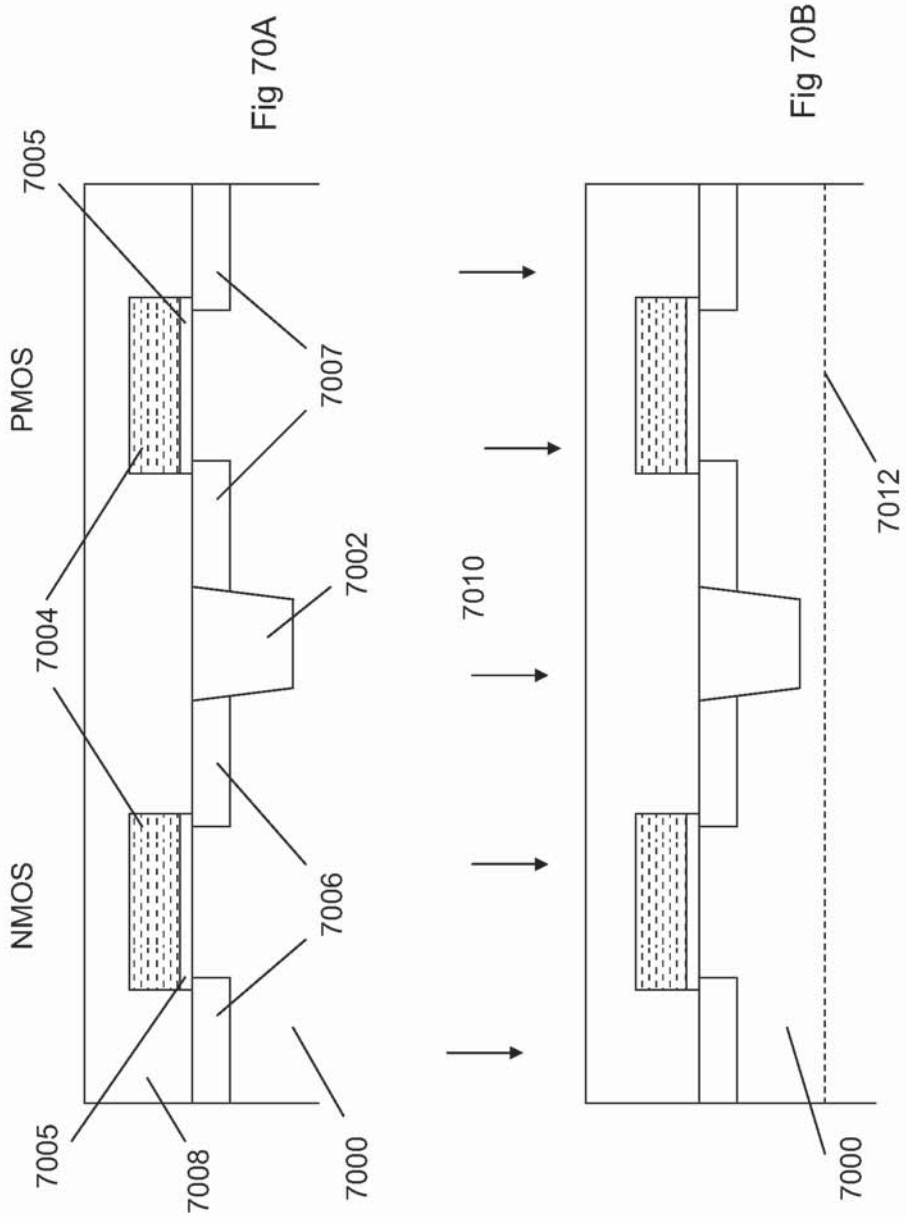

N
E
S
W
3040
n
p
n
p
n
p
n
p
n
3008
W
W
W
3122
3202
Rdy
DY
3120
6920
3020
6920C
6920
M
6922

Fig 69


Fig 70A
Fig 70B
PMOS
NMOS
7005
7004
7007
7002
7006
7008
7000
7010
7012

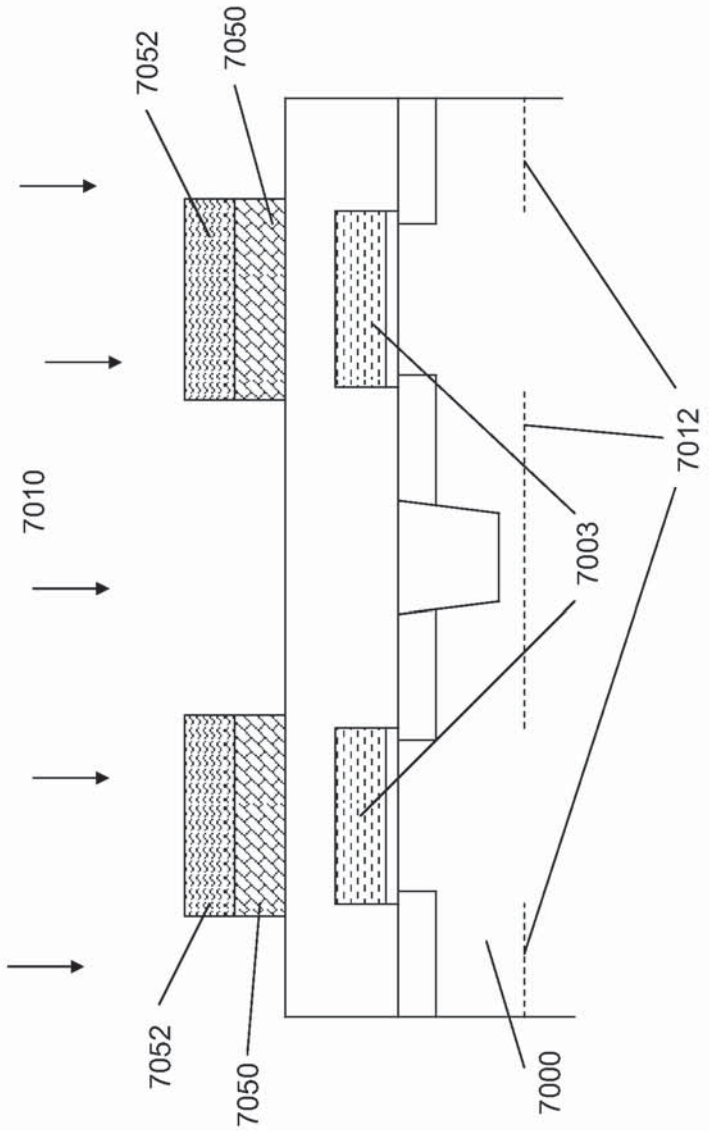


Fig 70B-1

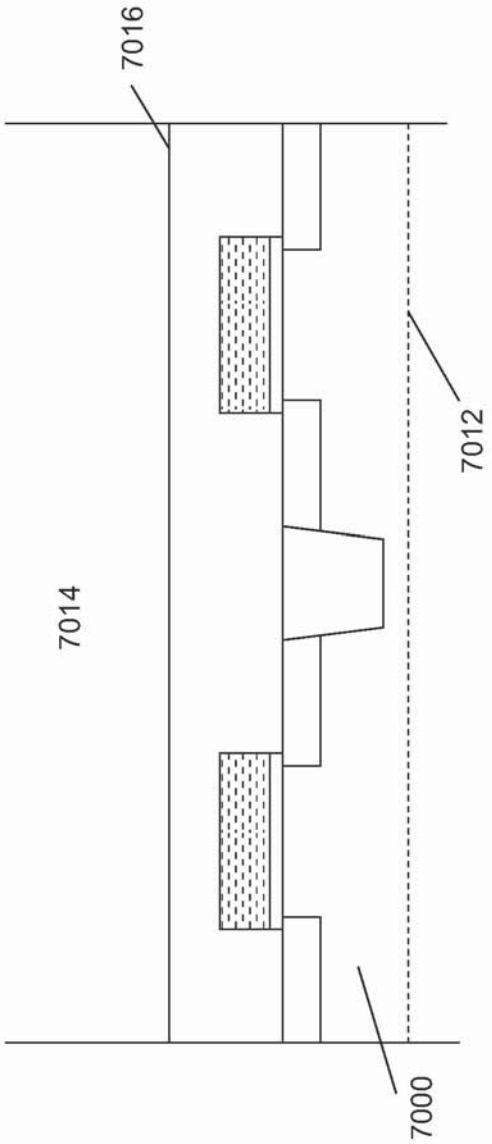


Fig 70C

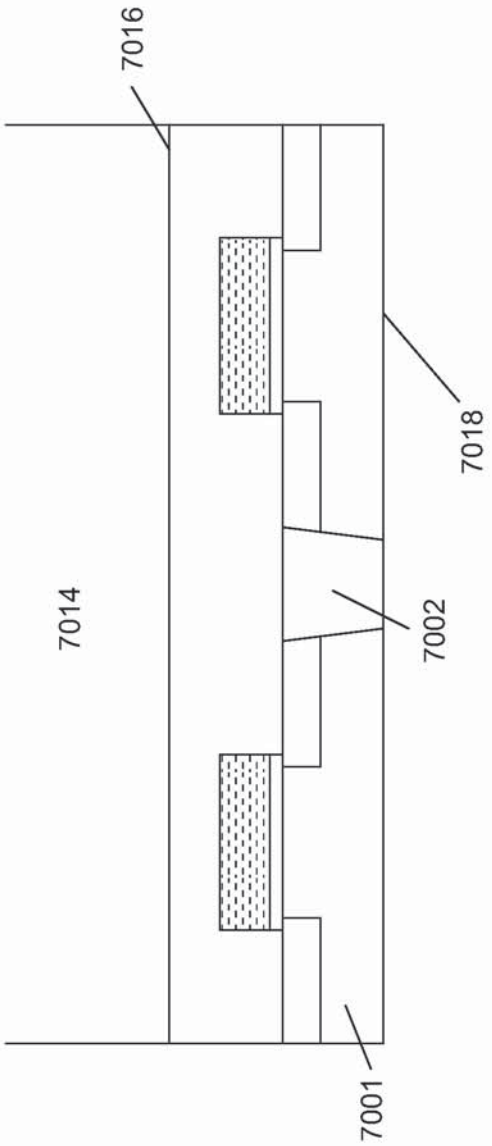


Fig 70D

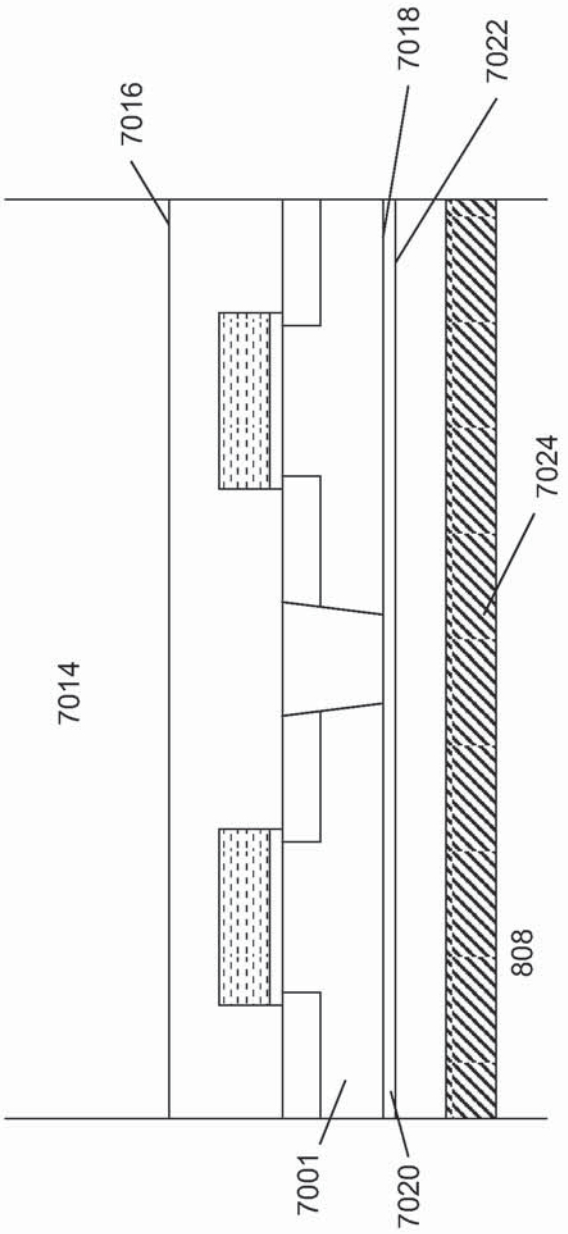


Fig 70E

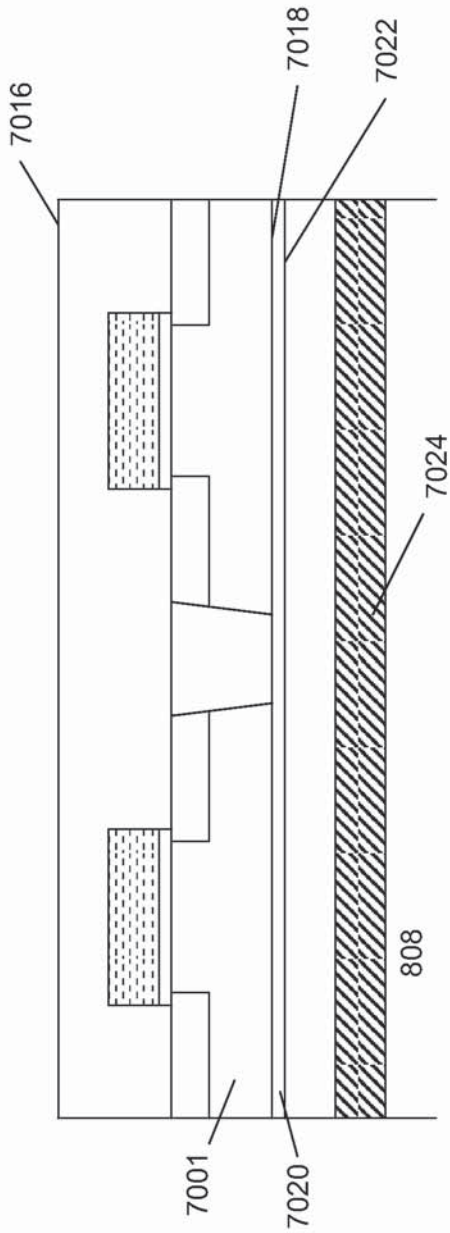


Fig 70F

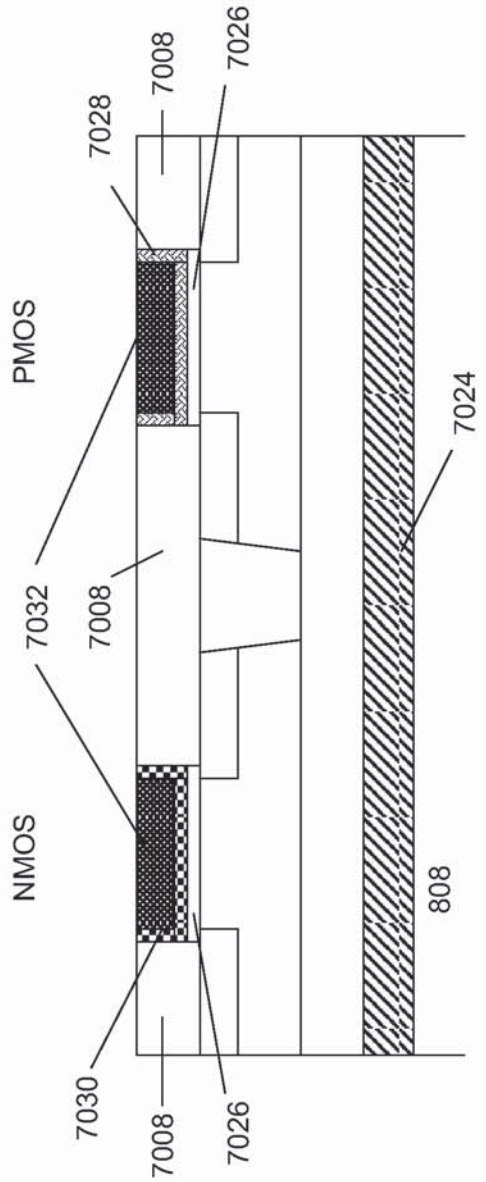


Fig 70G

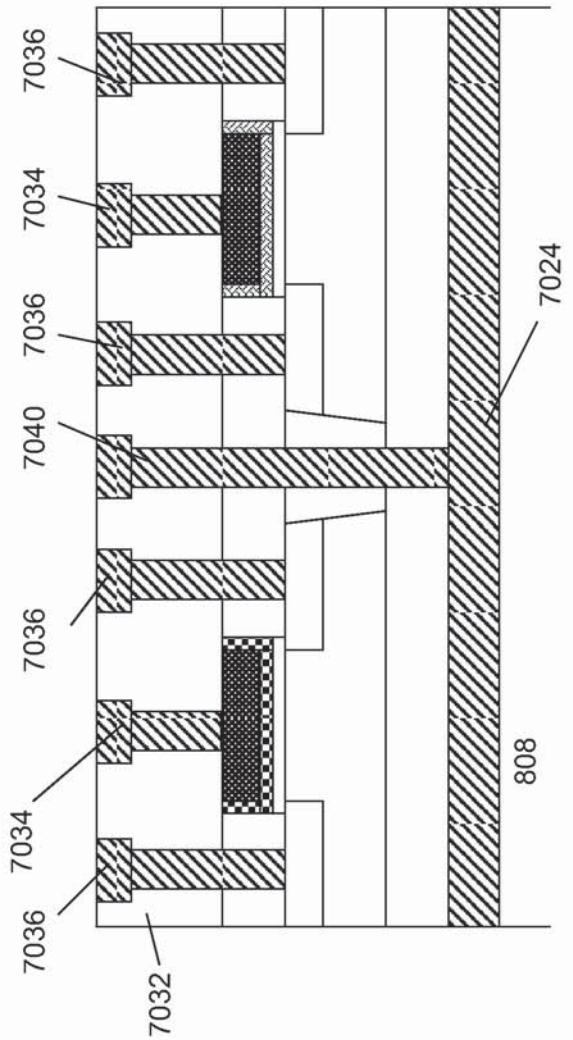


Fig 70H

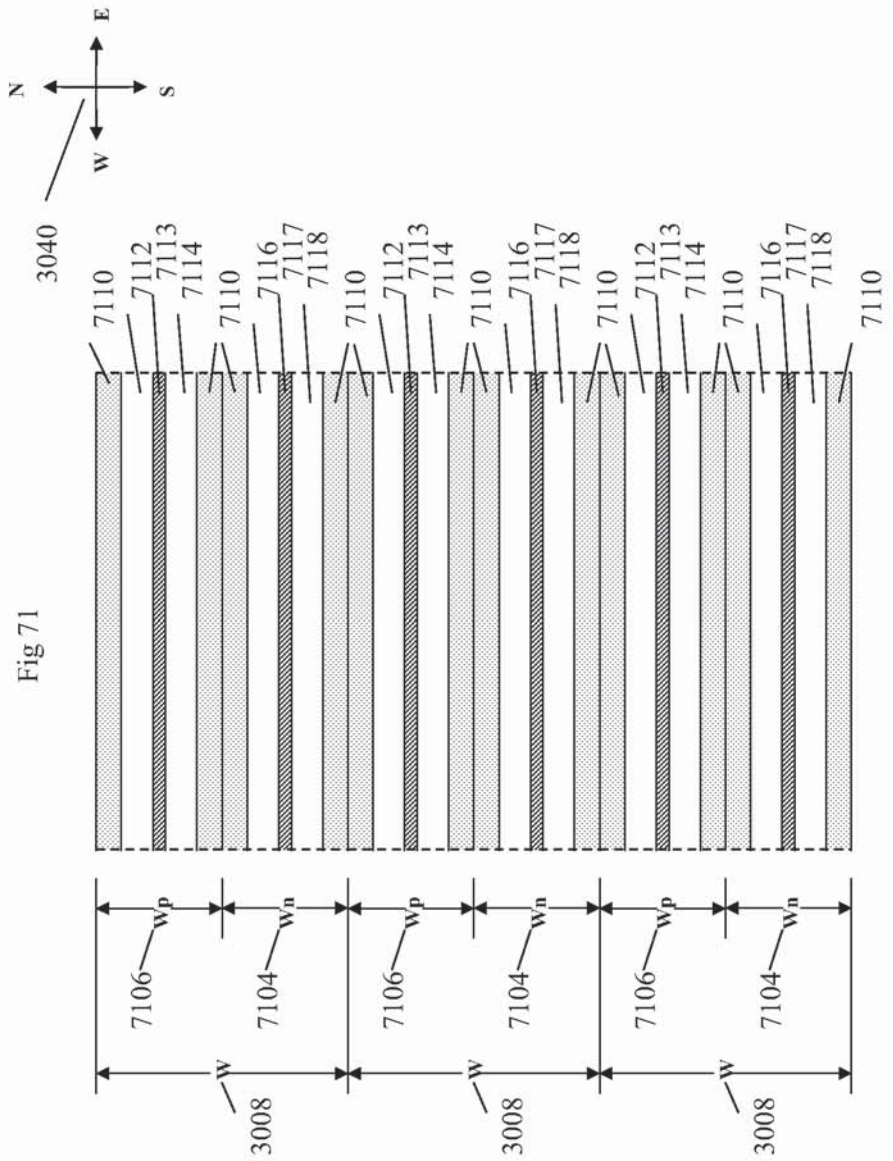

N
E
S
W
3040
7110
7112
7113
7114
7116
7117
7118
7106
7104
wp
wn
w
3008

Fig 71

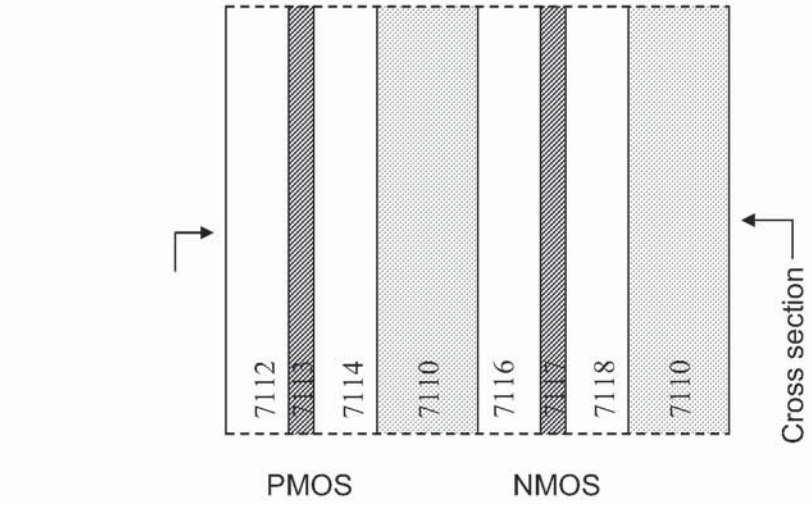
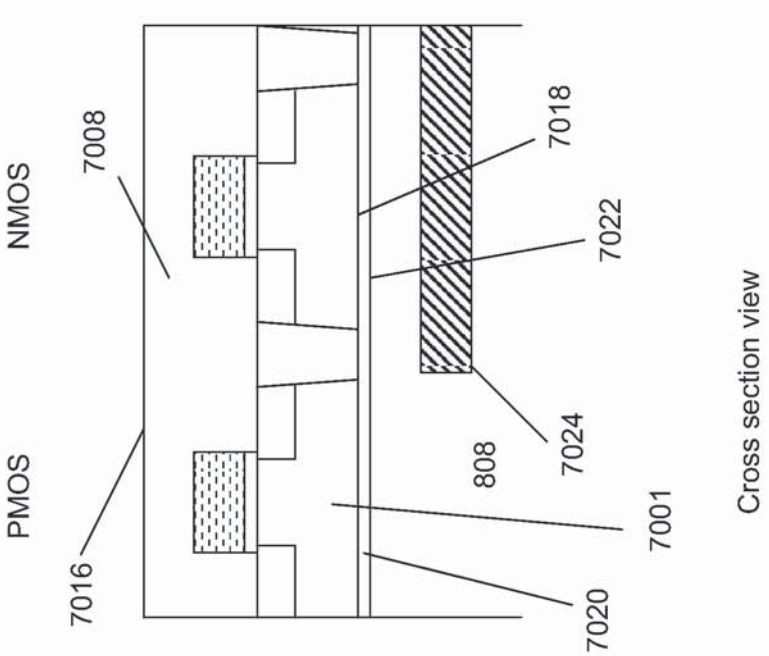

7112
7113
7114
7110
7116
7117
7118
7110
Cross section
PMOS
NMOS

Fig 72A


7008
7018
7022
7024
808
7001
7016
7020
PMOS
NMOS
Cross section view

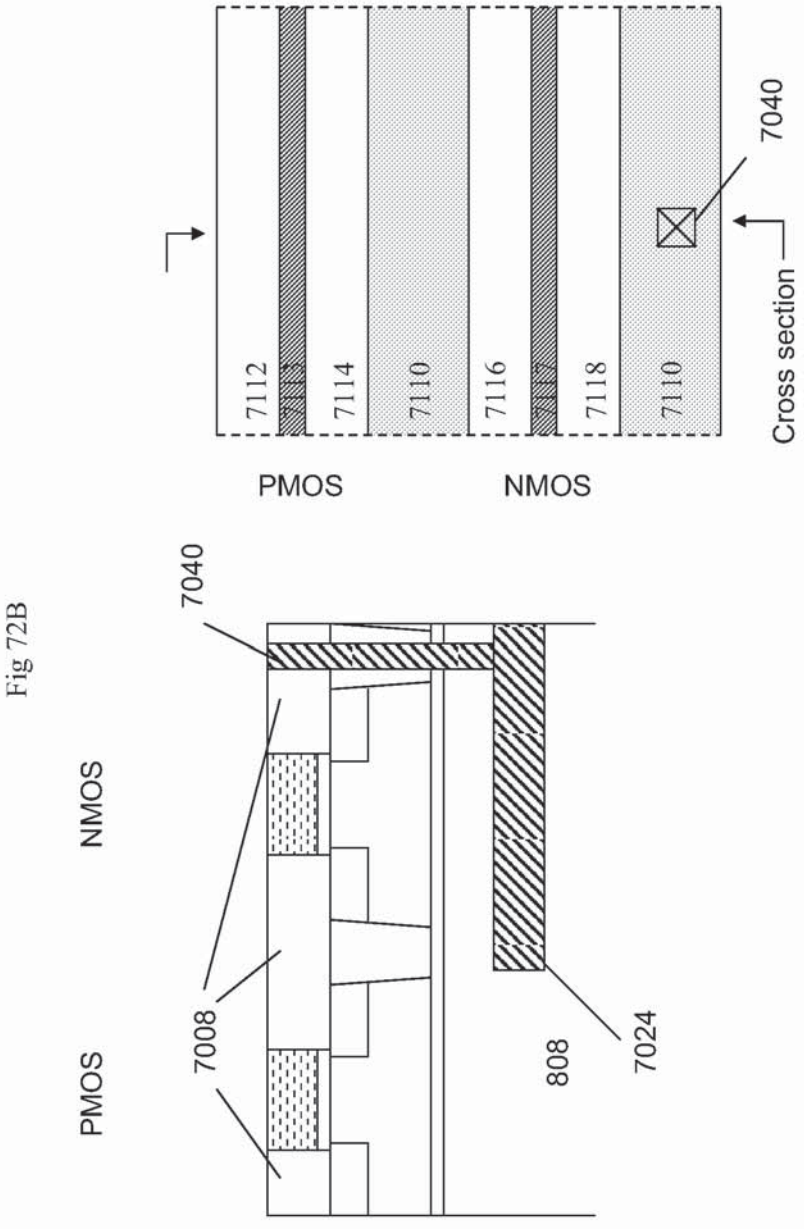
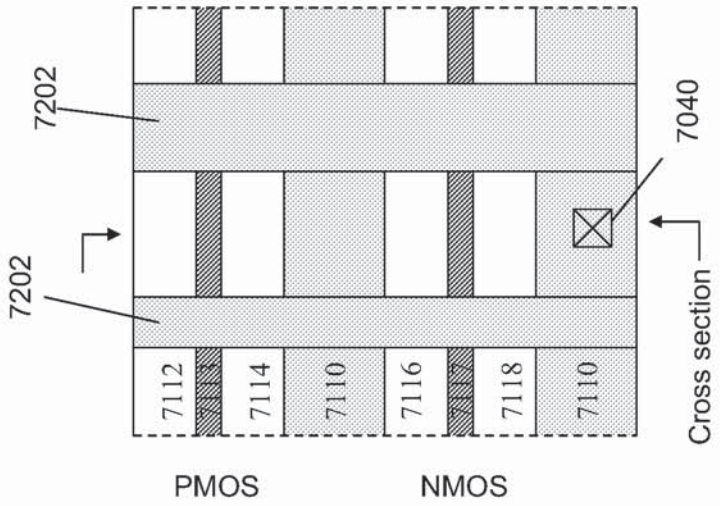

7040
Cross section
7112
7113
7114
7110
7116
7117
7118
7110
PMOS
NMOS
7040
NMOS
PMOS
7008
808
7024
Cross section view

Fig 72B


7202
7202
7040
Cross section
7112
7113
7114
7110
7116
7117
7118
7110
PMOS
NMOS

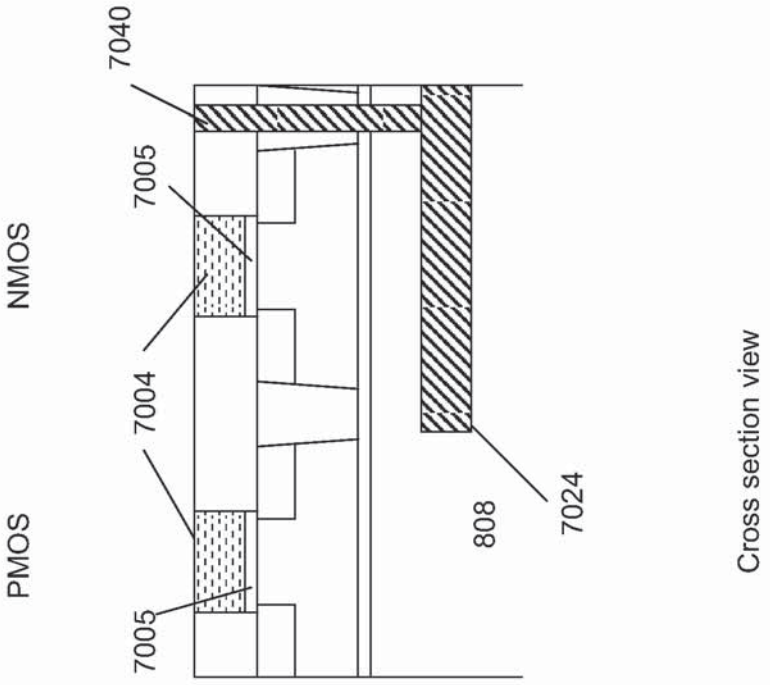

7040
7005
NMOS
7004
PMOS
7005
808
7024
Cross section view

Fig 72C

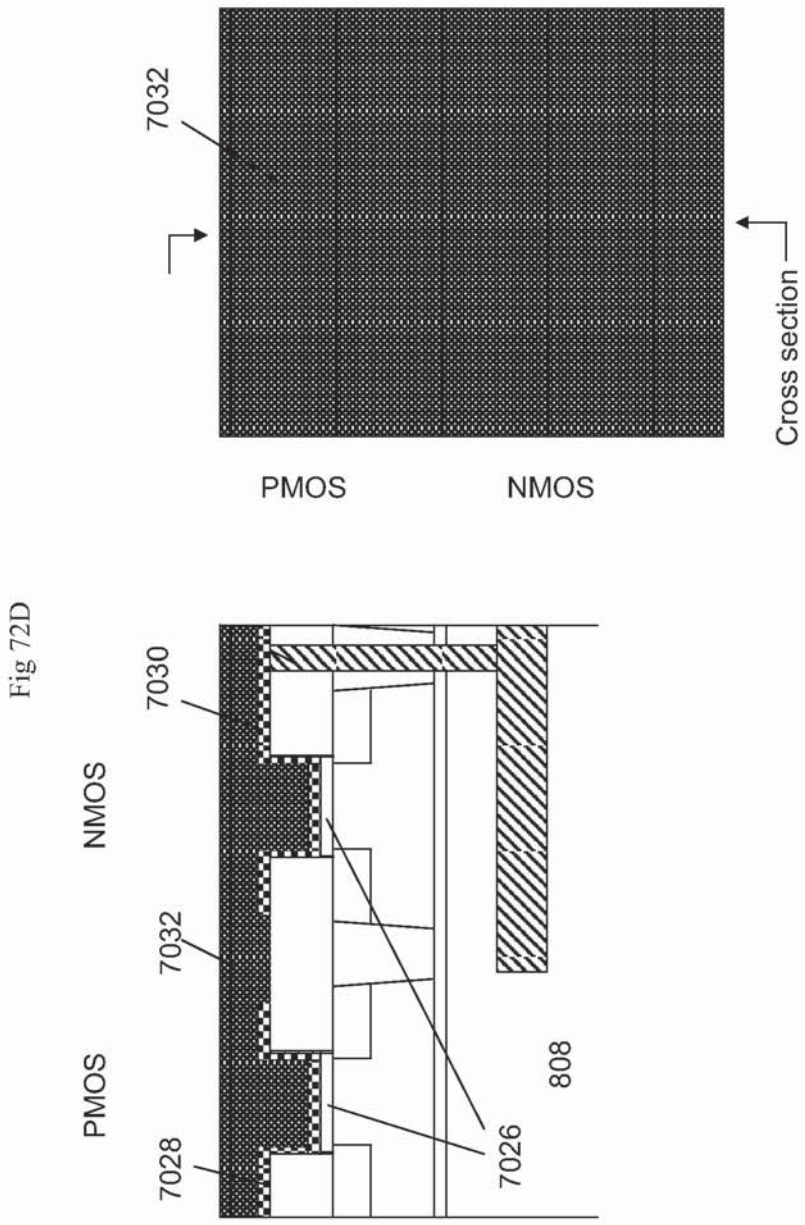

7032
Cross section
PMOS
NMOS
7030
NMOS
7032
PMOS
7028
7026
808
Cross section view

Fig 72D

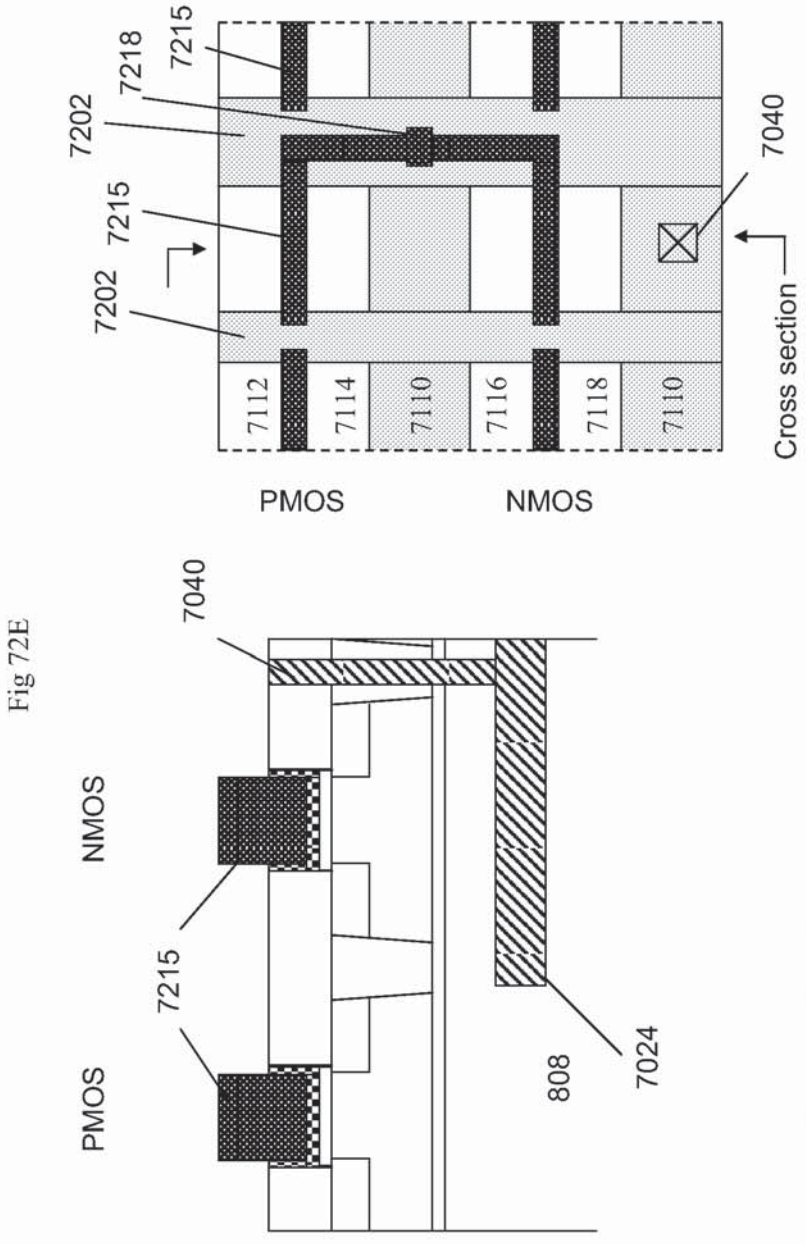

7215
7218
7202
7215
7202
7040
Cross section
7112
7114
7110
7116
7118
7110
PMOS
NMOS
7040
NMOS
7215
PMOS
808
7024
Cross section view

Fig 72E

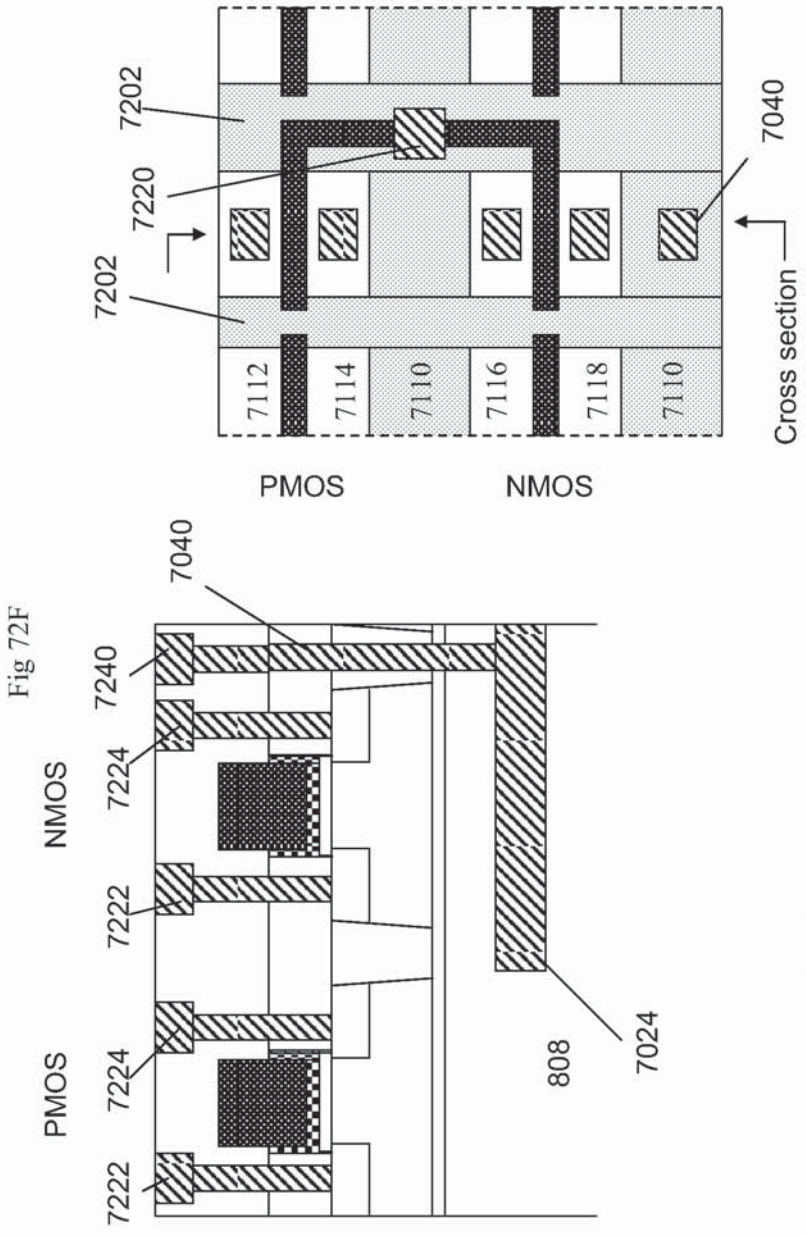

7202
7220
7202
7040
Cross section
7112
7114
7110
7116
7118
7110
PMOS
NMOS
7040
7240
7224
7222
7224
7222
NMOS
PMOS
808
7024
Cross section view

Fig 72F

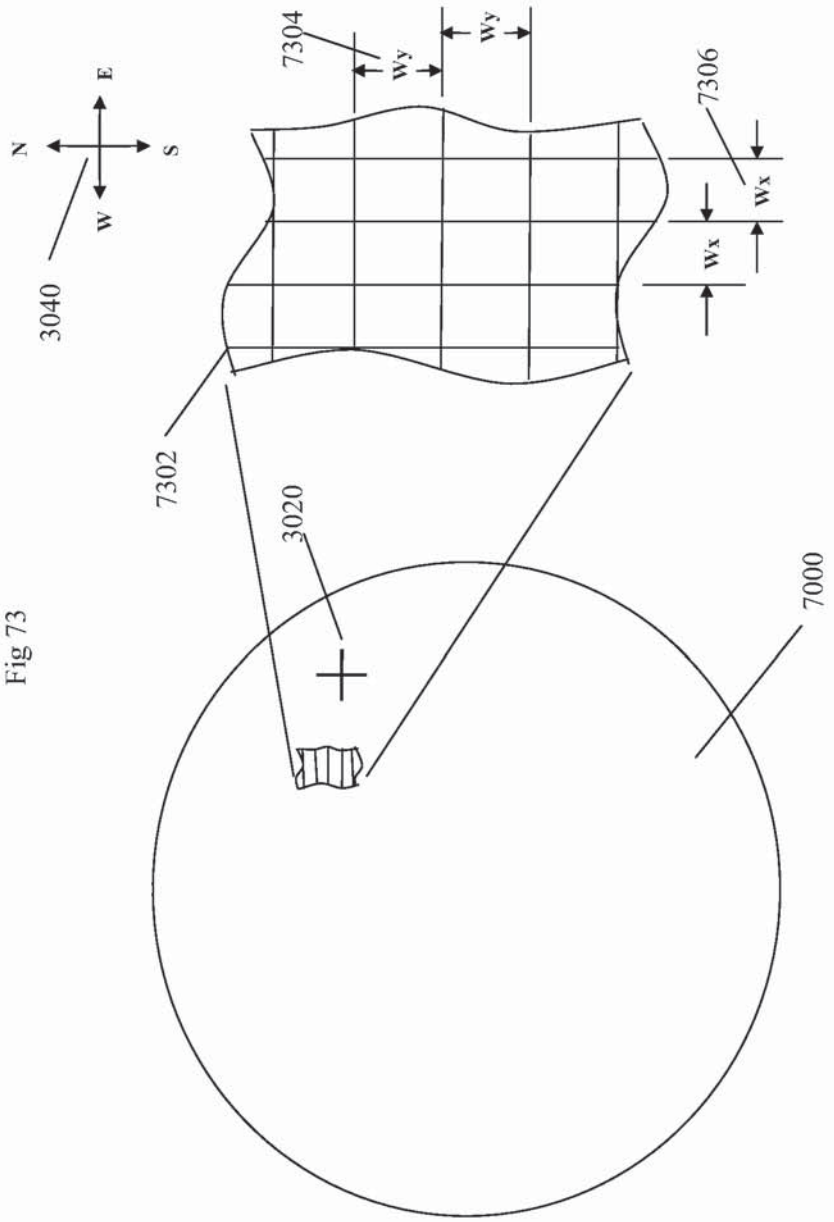


Fig 73

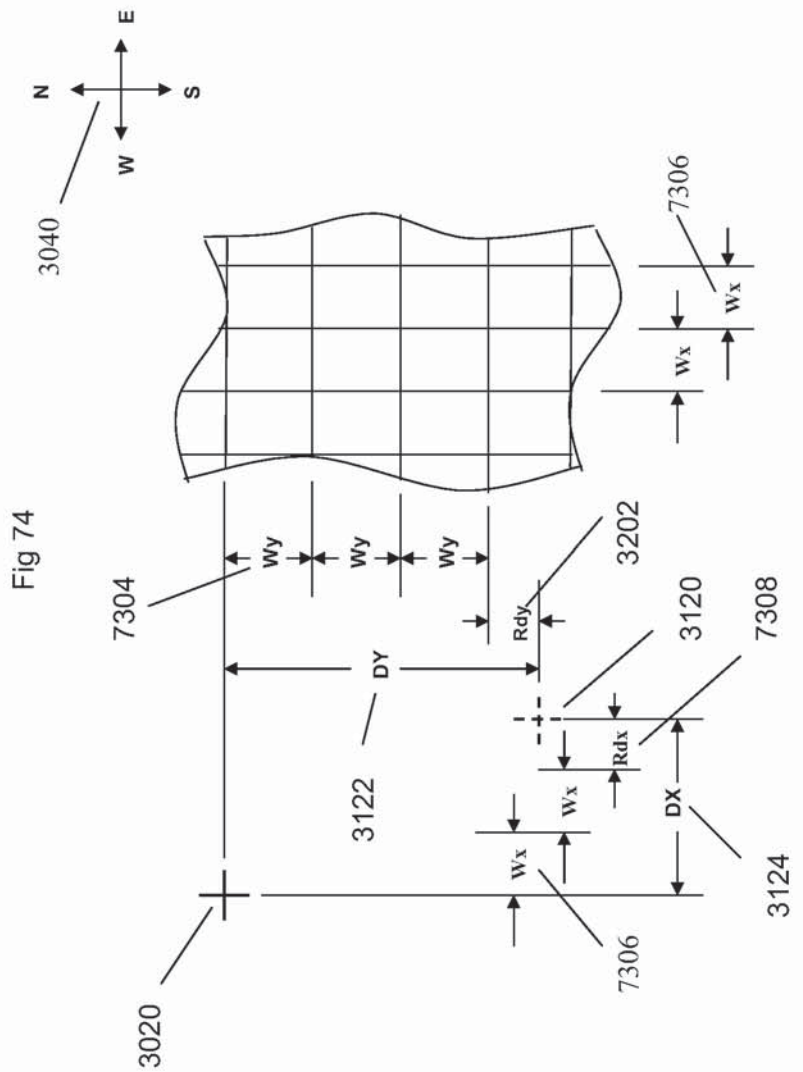

N
E
S
W
3040
7306
Wx
Wx
Wy
Wy
Wy
3202
7304
Rdy
3120
7308
DY
Rdx
3122
Wx
DX
Wx
3124
7306
3020

Fig 74

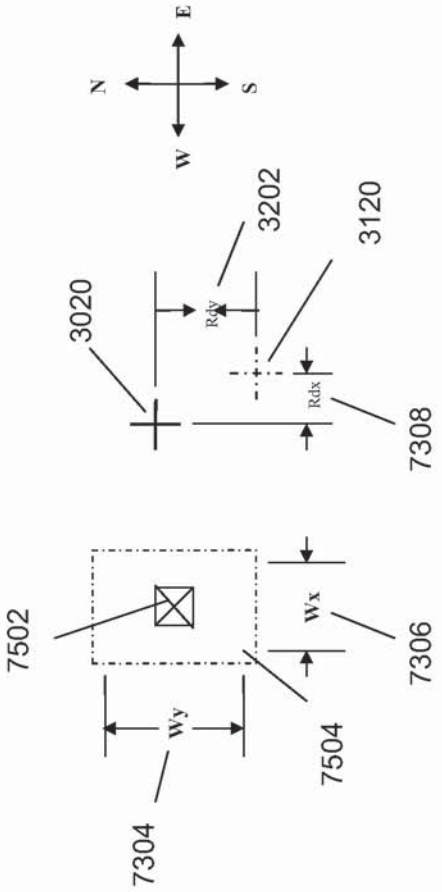


Fig 75

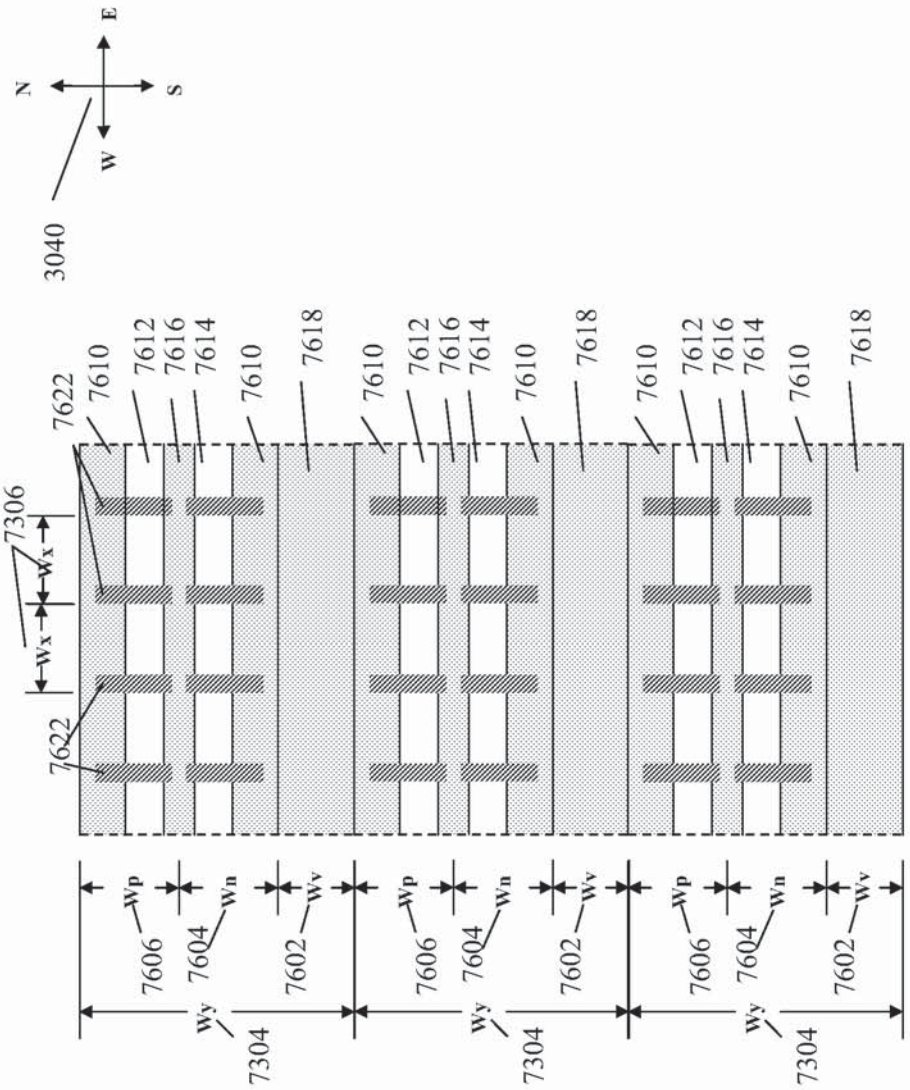

N
E
S
W
3040
7622
7306
Wx
Wx
7622
7610
7612
7616
7614
7610
7618
7610
7612
7616
7614
7610
7618
7610
7612
7616
7614
7610
7618
7610
7612
7616
7614
7610
7618
Wp
Wn
Wv
7606
7604
7602
Wy
7304

Fig 76

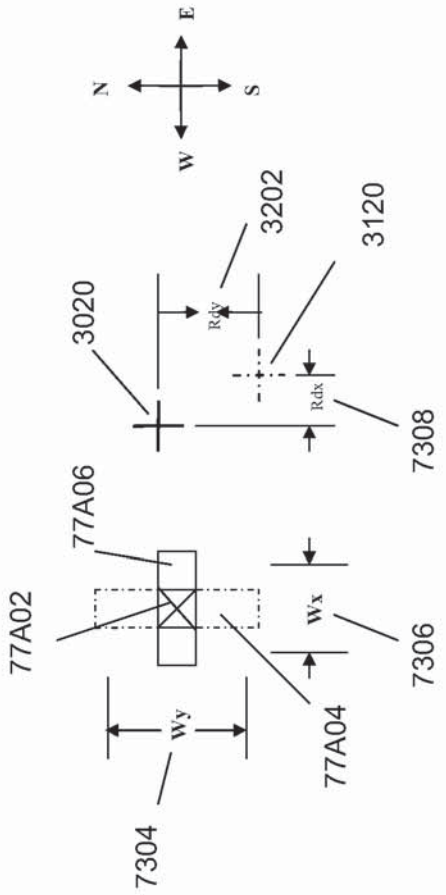

N
E
S
W
3202
3120
3020
Rdy
Rdx
7308
77A06
77A02
Wx
7306
Wy
77A04
7304

Fig 77

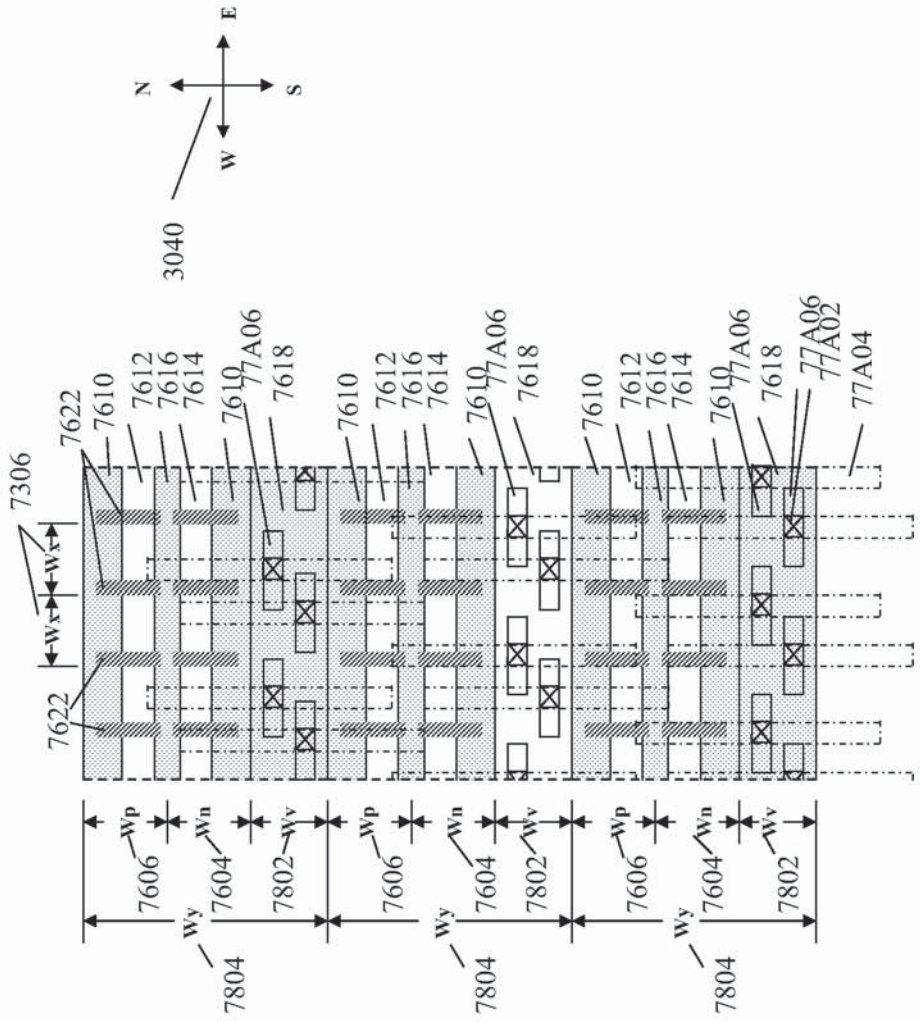

N
E
S
W
3040
7306
7622
7610
7612
7616
7614
77A06
7618
77A02
77A04
Wx
Wp
Wn
Wv
Wy
7606
7604
7802
7804

Fig 78A

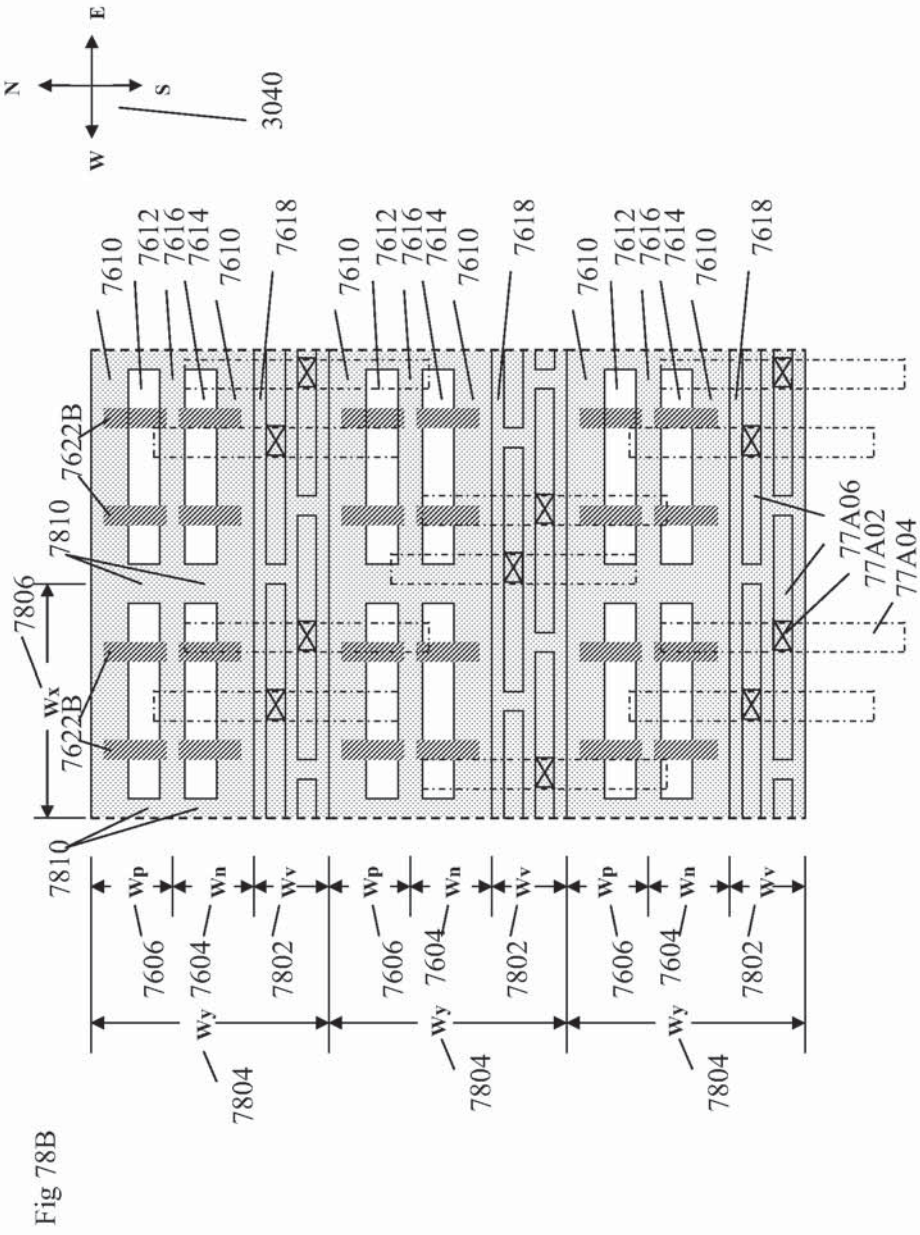

N
E
S
W
3040
7610
7612
7616
7614
7618
7622B
7810
7806
Wx
77A06
77A02
77A04
Wp
Wn
Wv
Wy
7606
7604
7802
7804

Fig 78B

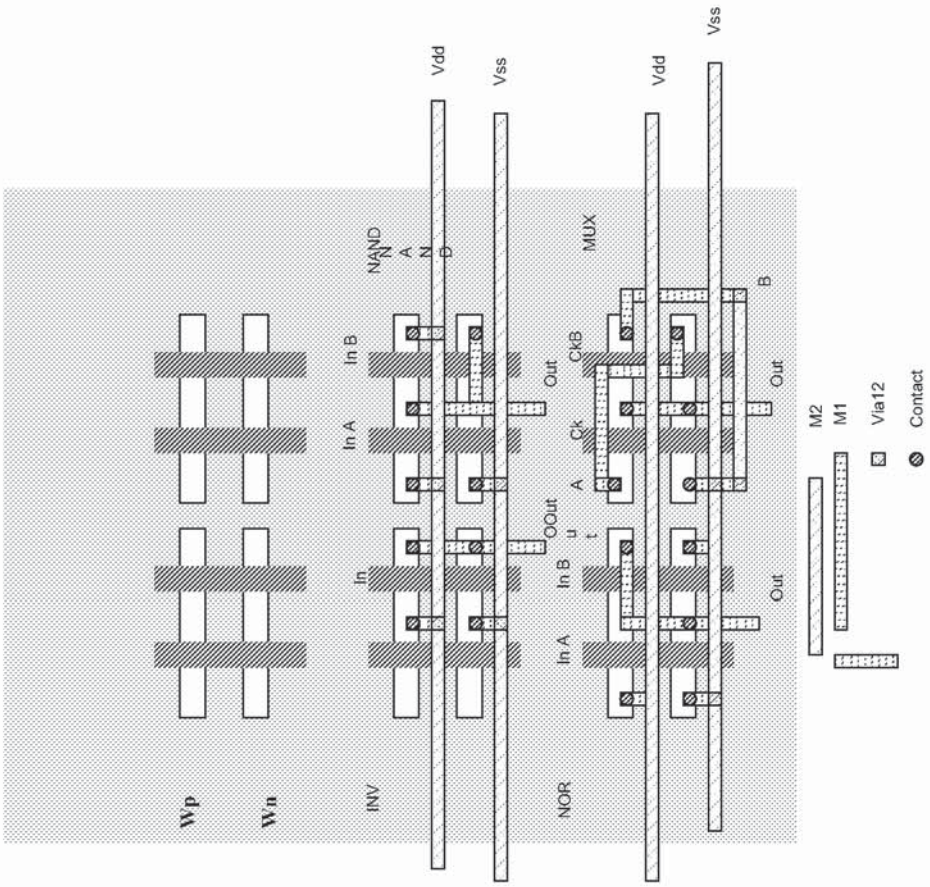
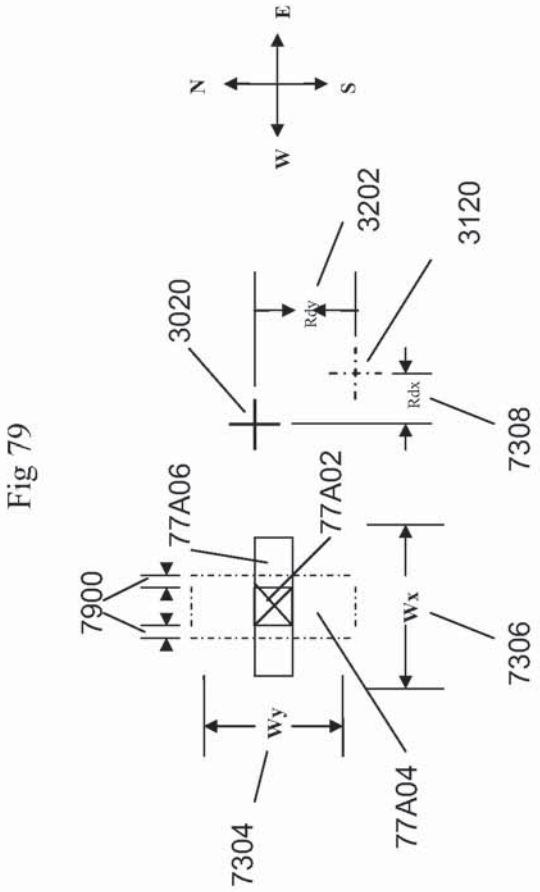

Wp
Wn
INV
In
In A
In B
NAND
Out
Vdd
Vss
NOR
OOut
MUX
Ck
CkB
A
B
M2
M1
Via12
Contact

FIG. 78C

Fig 79


E
N
S
W
3202
3120
3020
Rdy
Rdx
7308
77A06
77A02
7900
Wx
7306
Wy
7304
77A04

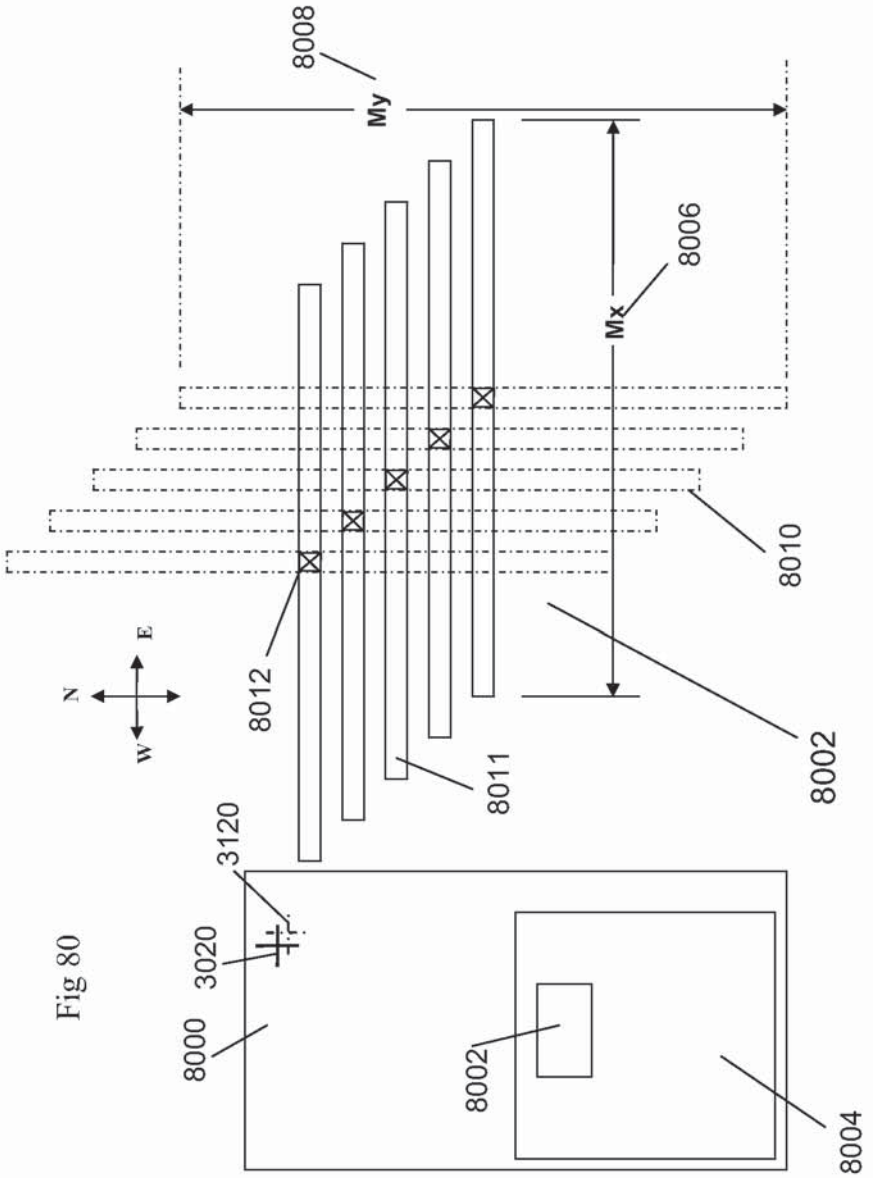

8008
My
8006
Mx
8010
8012
8002
8011
N
E
W
3120
3020
8000
8002
8004

Fig 80

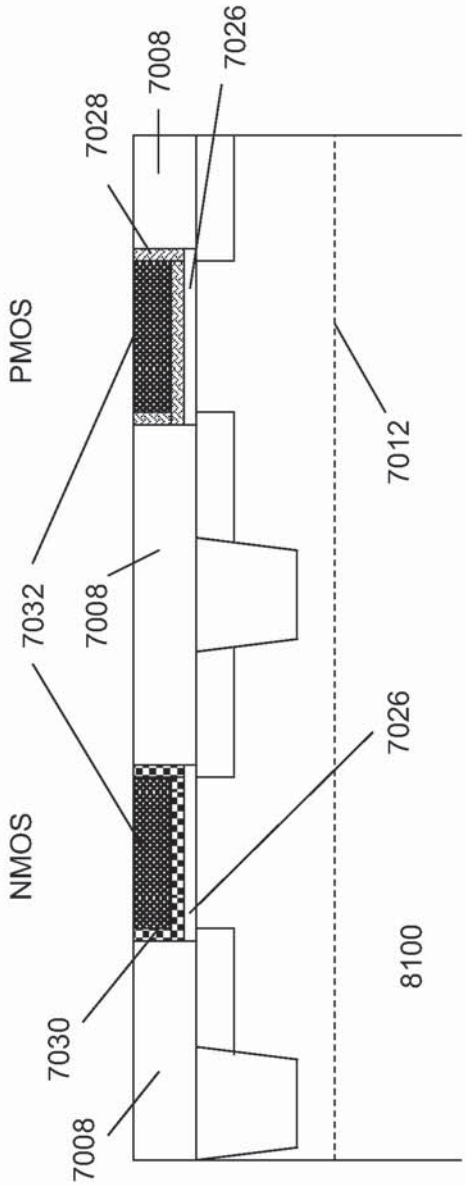


Fig 81A

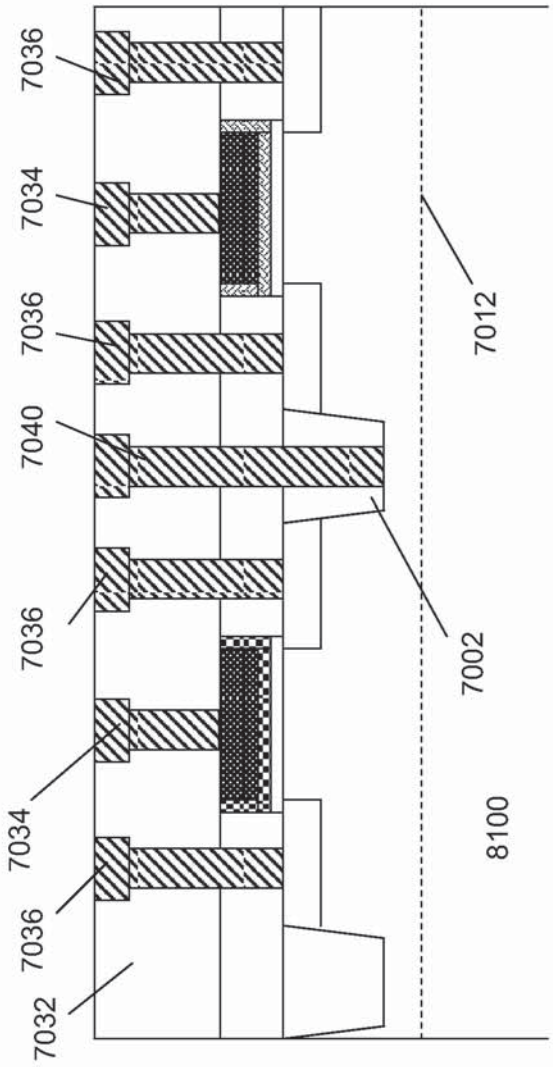


Fig 81B

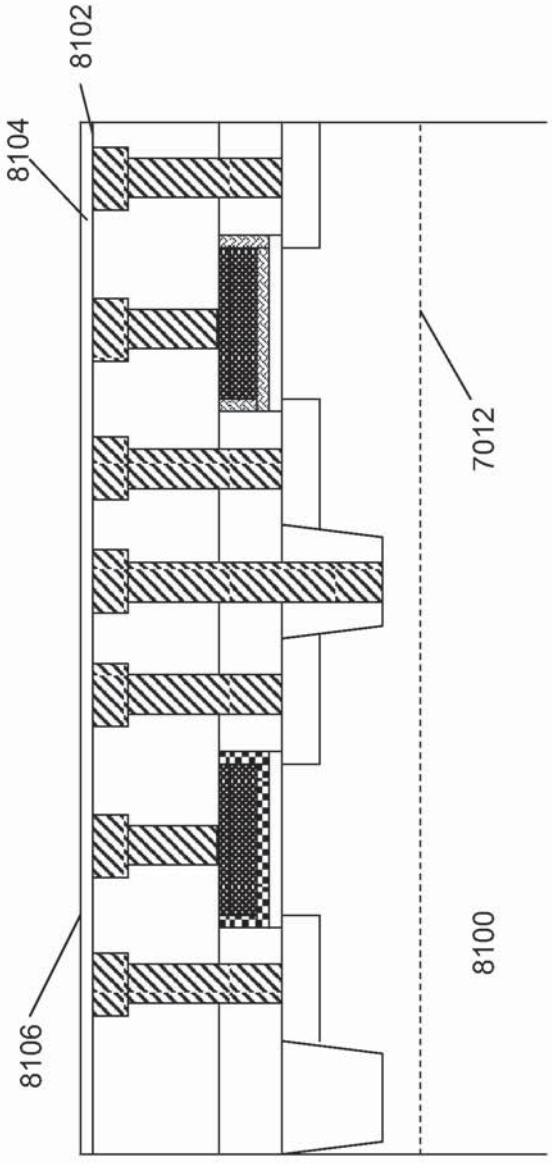


Fig 81C

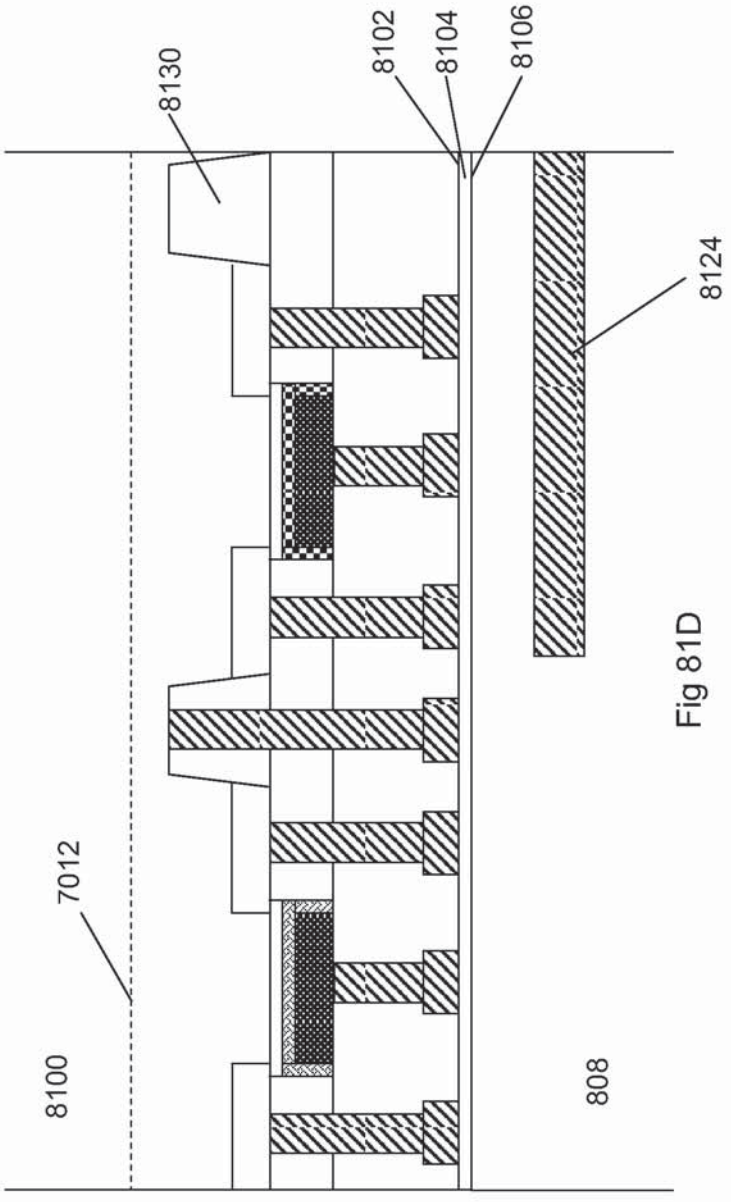


Fig 81D

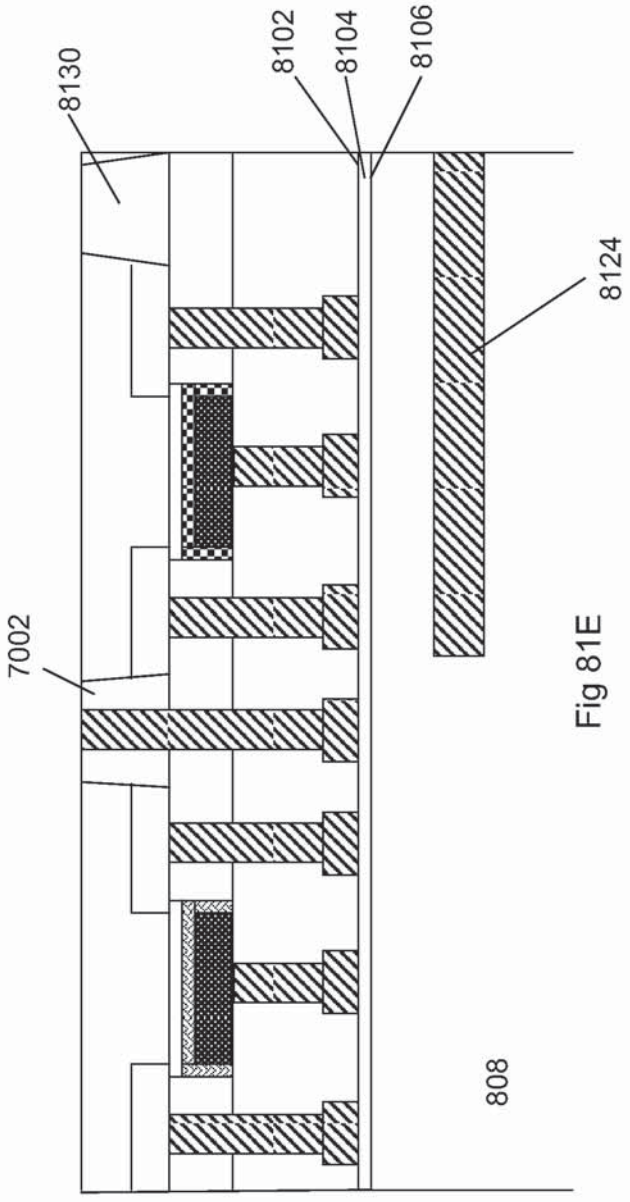


Fig 81E

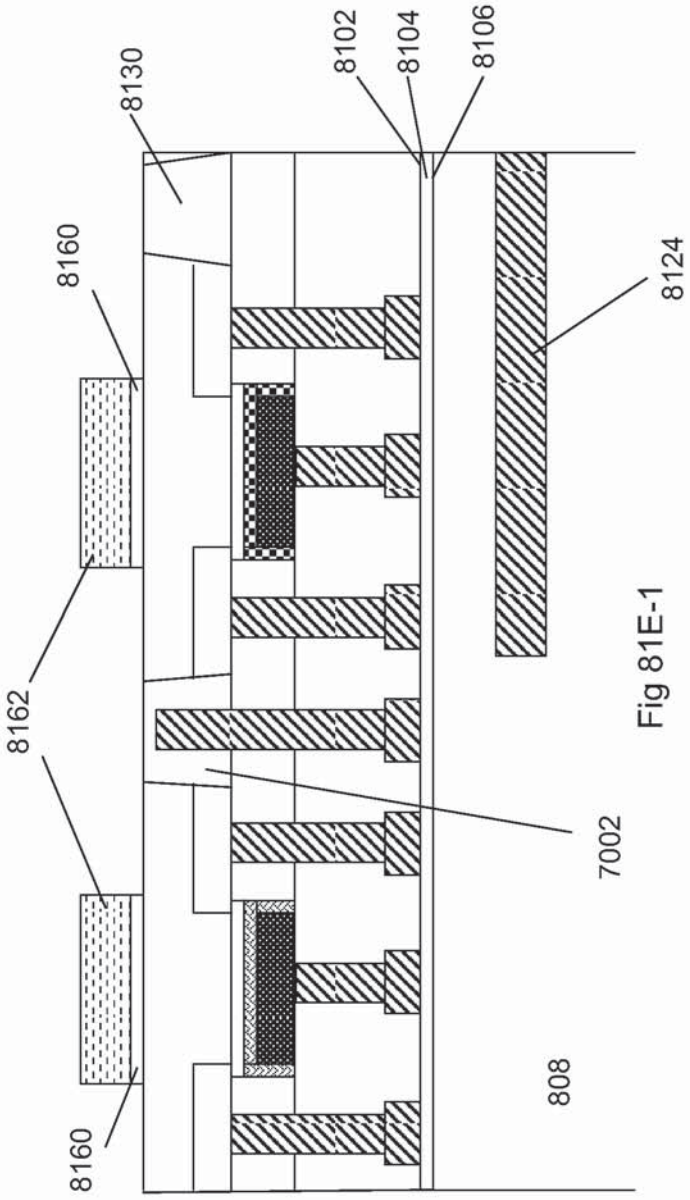


Fig 81E-1

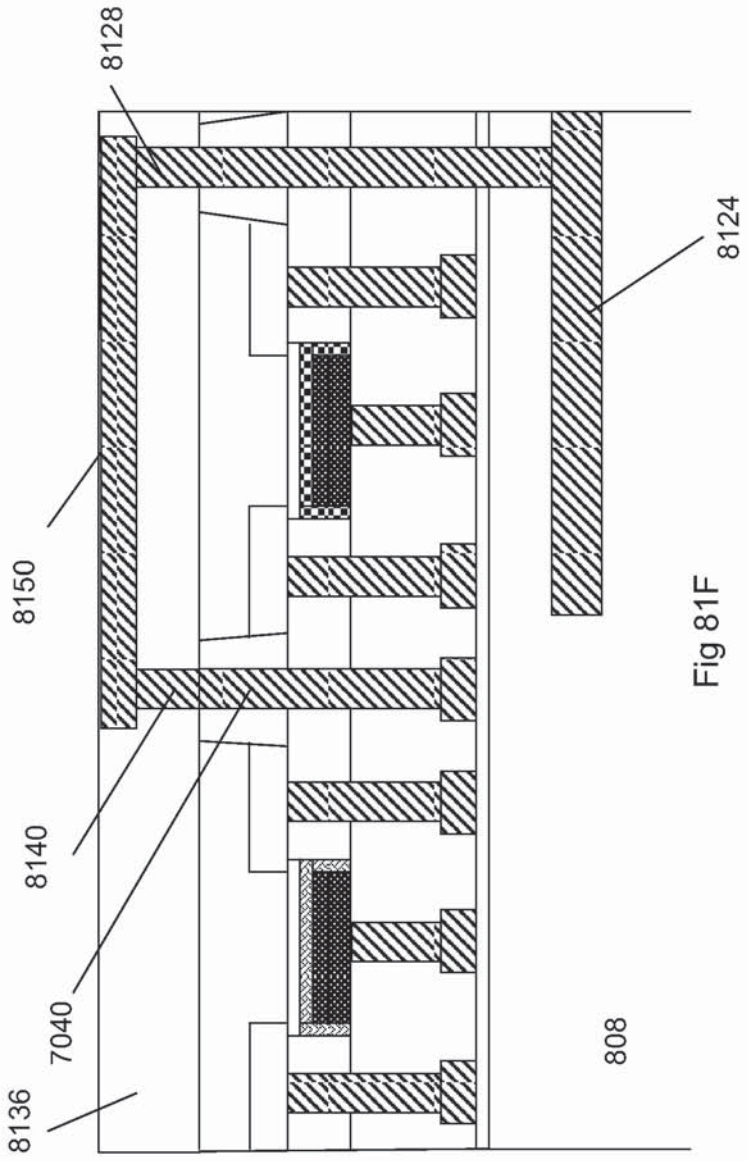


Fig 81F

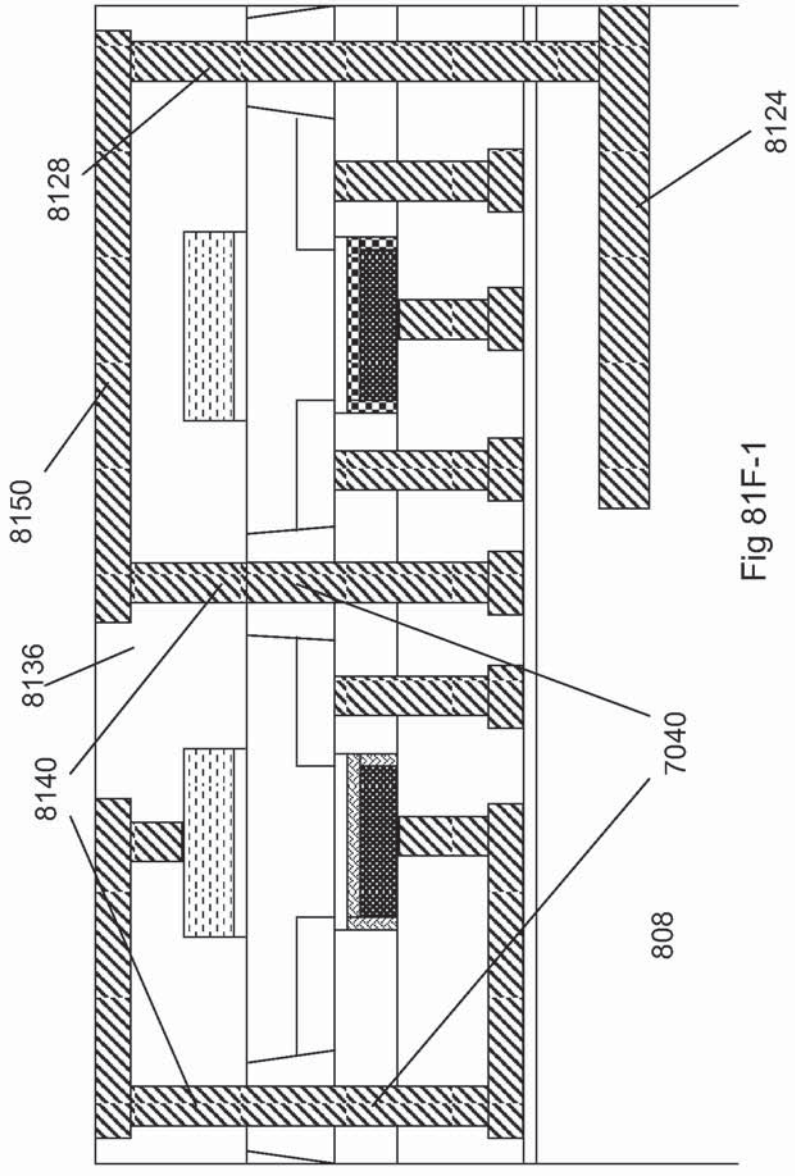


Fig 81F-1

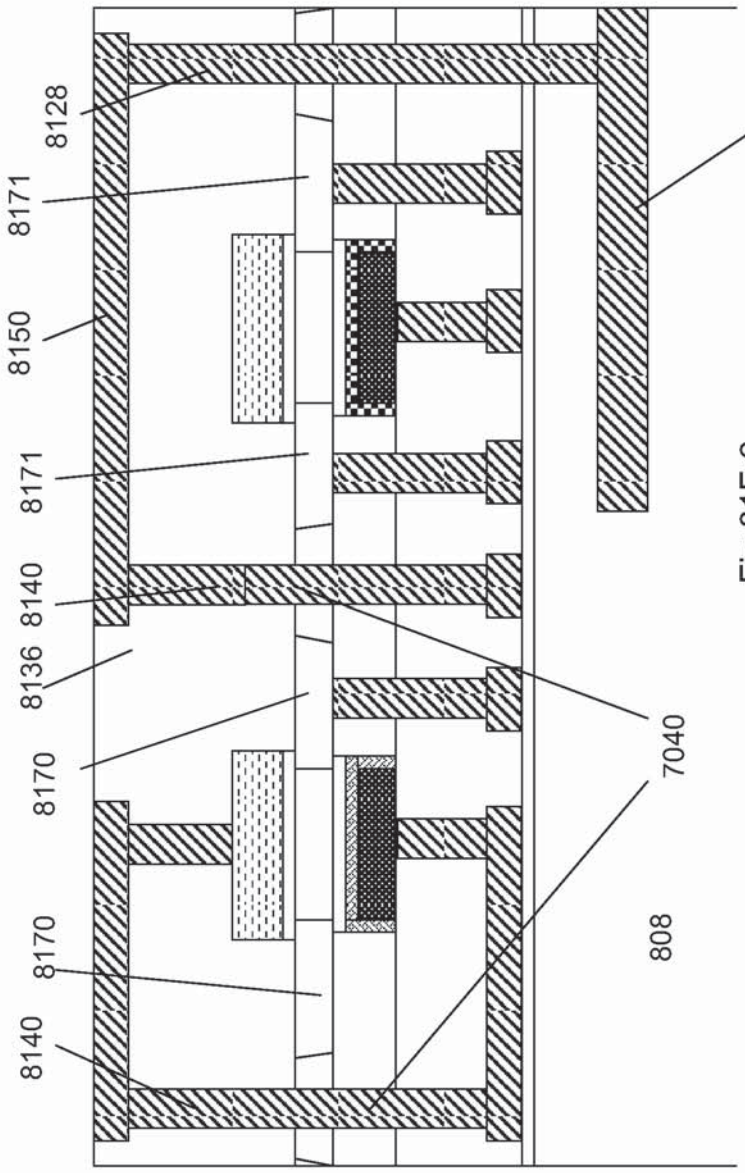


Fig 81F-2

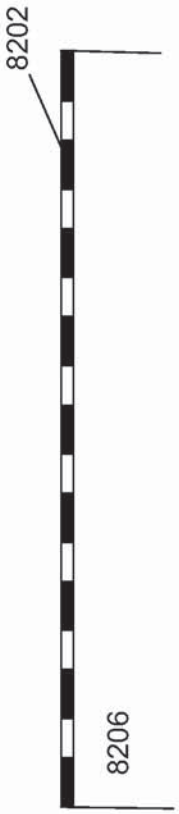


Fig 82A

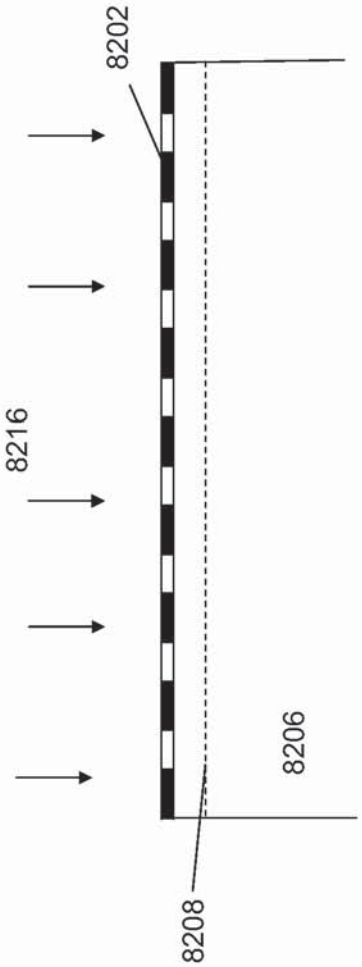


Fig 82B

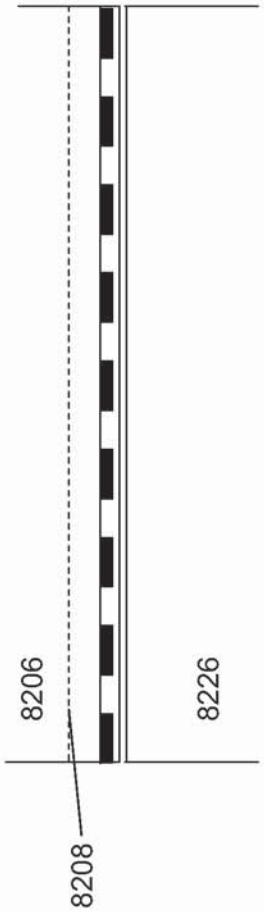


Fig 82C

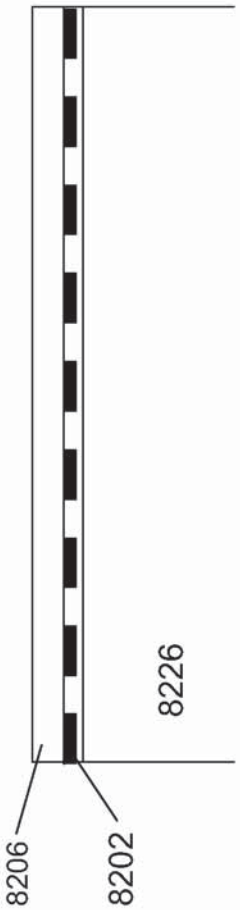


Fig 82D

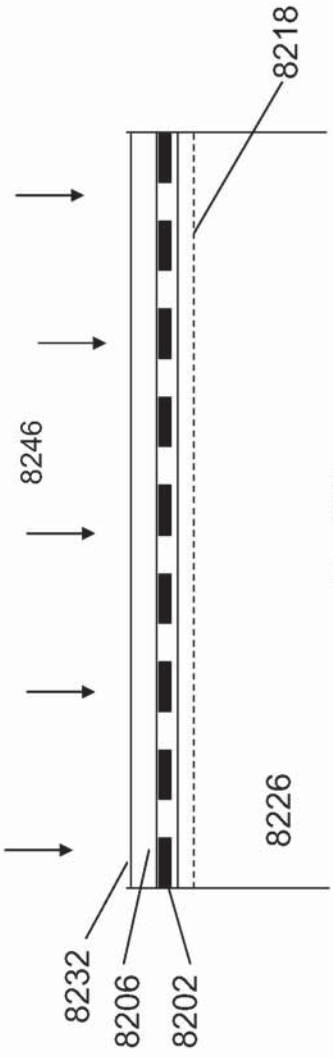


Fig 82E

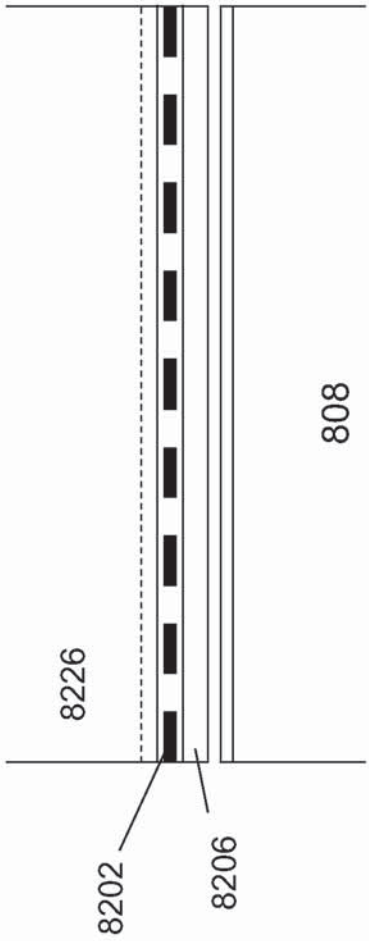


Fig 82F

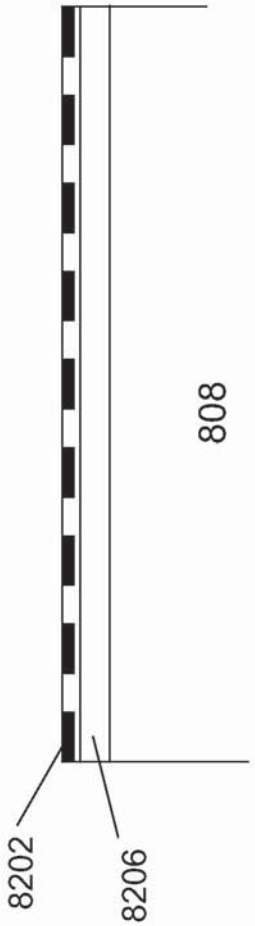
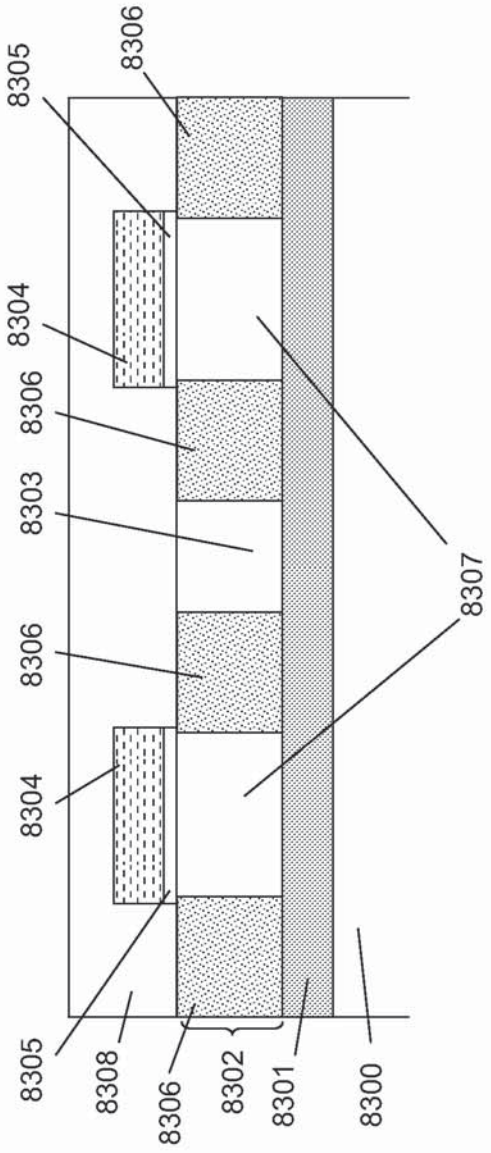


Fig 82G

Fig 83A


8305
8306
8304
8306
8303
8306
8304
8307
8305
8308
8306
8302
8301
8300

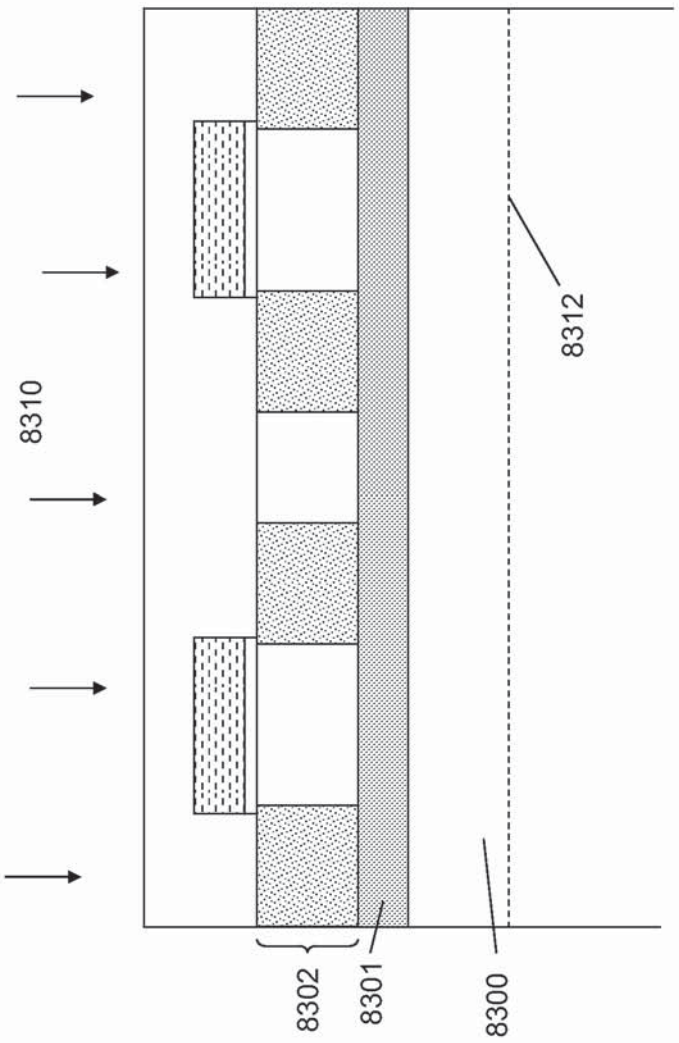


Fig 83B

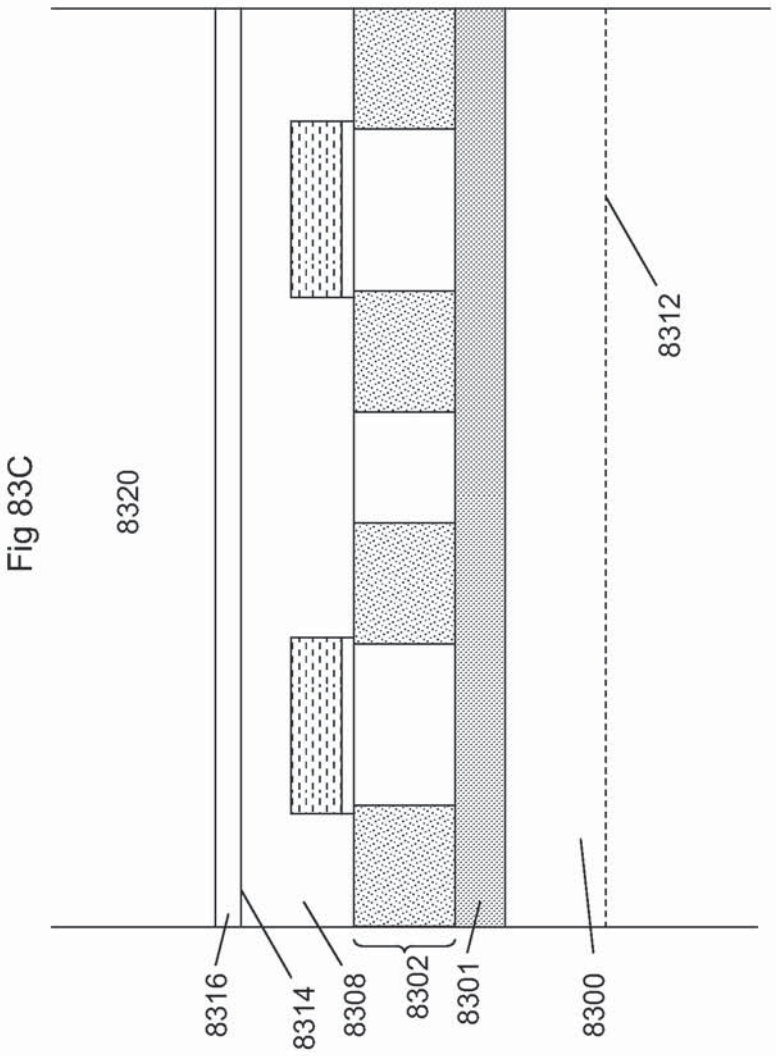


Fig 83C

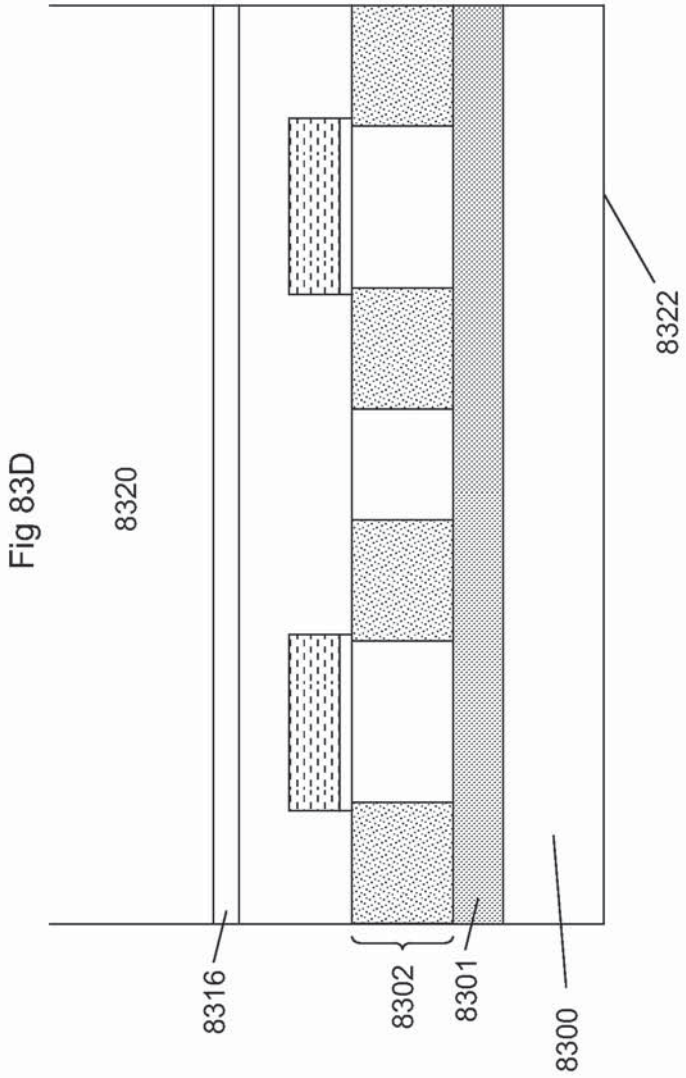


Fig 83D

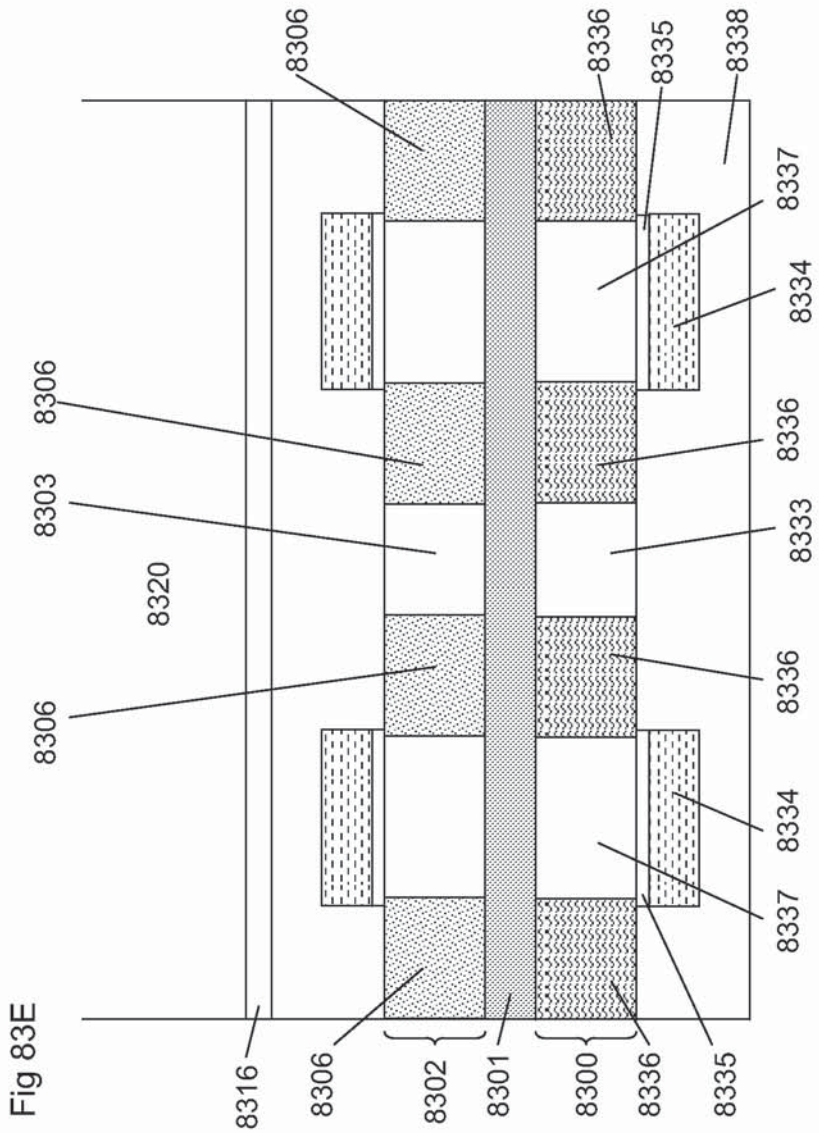

8306
8336
8335
8338
8337
8334
8306
8336
8303
8333
8320
8336
8306
8334
8337
8316
8306
8302
8301
8300
8336
8335

Fig 83E

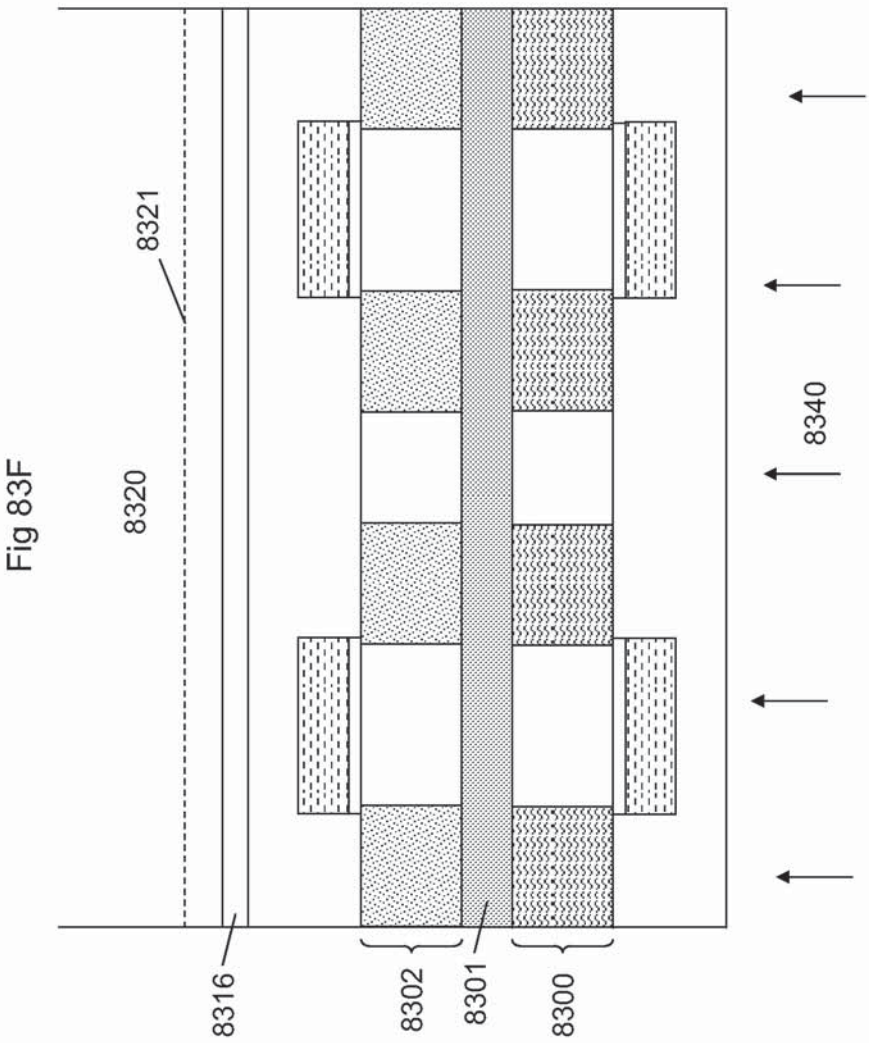


Fig 83F

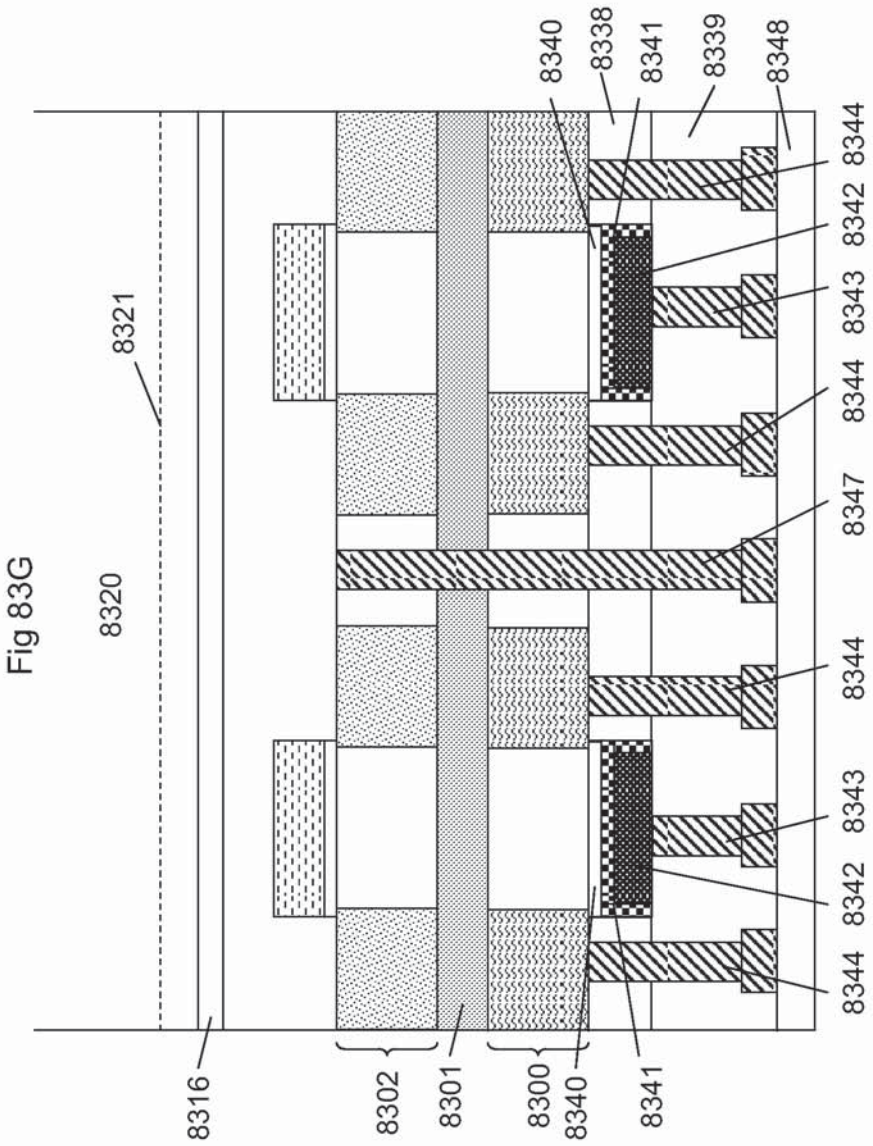

8340
8338
8341
8339
8348
8344
8342
8343
8344
8347
8344
8343
8342
8344
8321
8320
8316
8302
8301
8300
8340
8341

Fig 83G

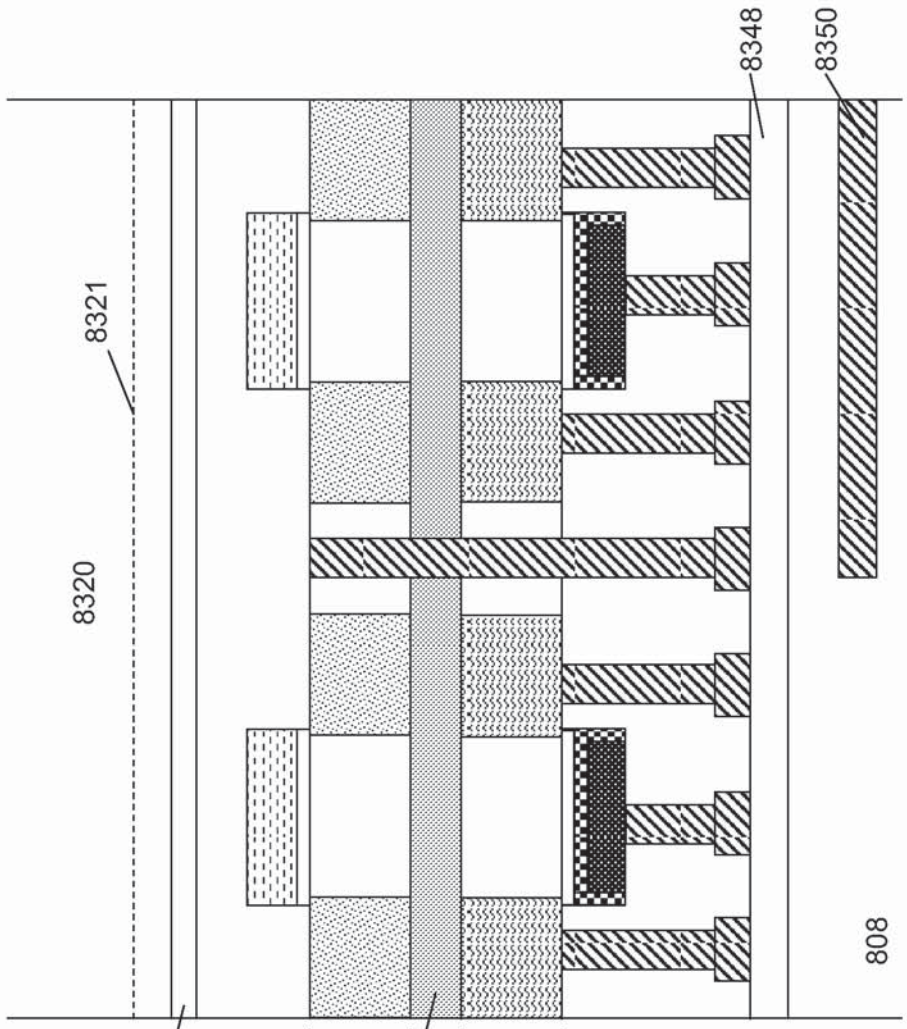


Fig 83H

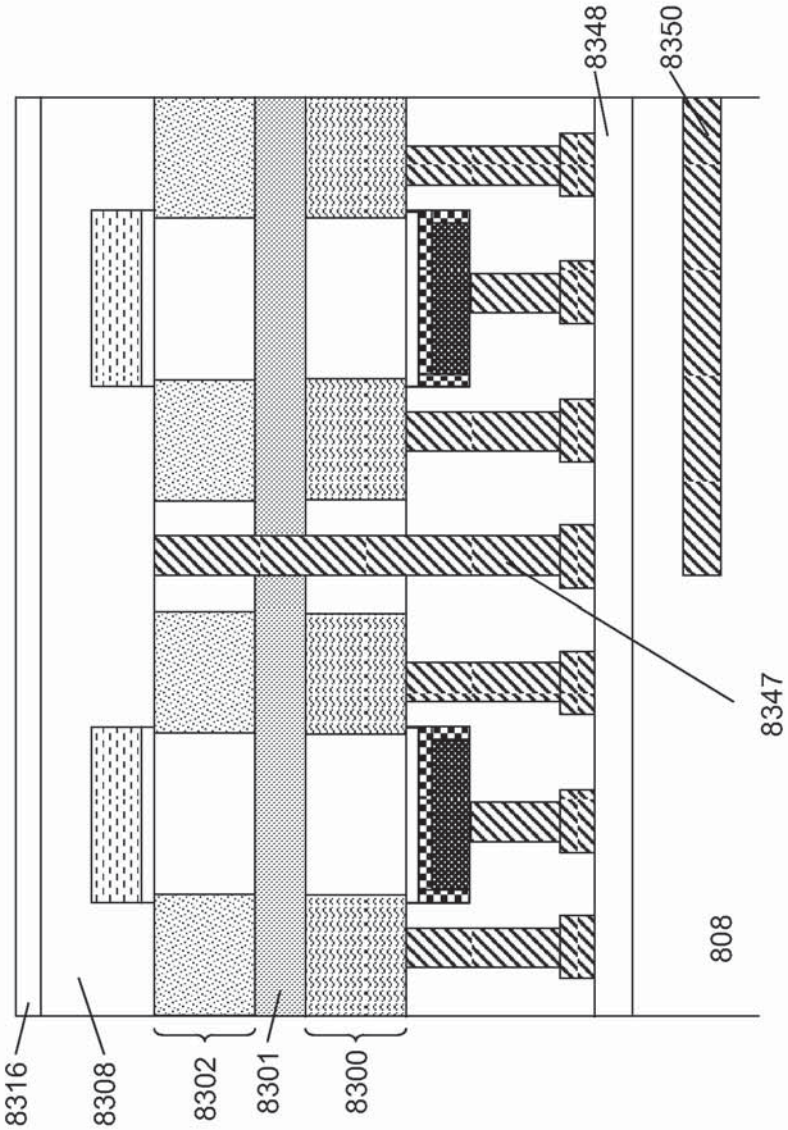


Fig 83I

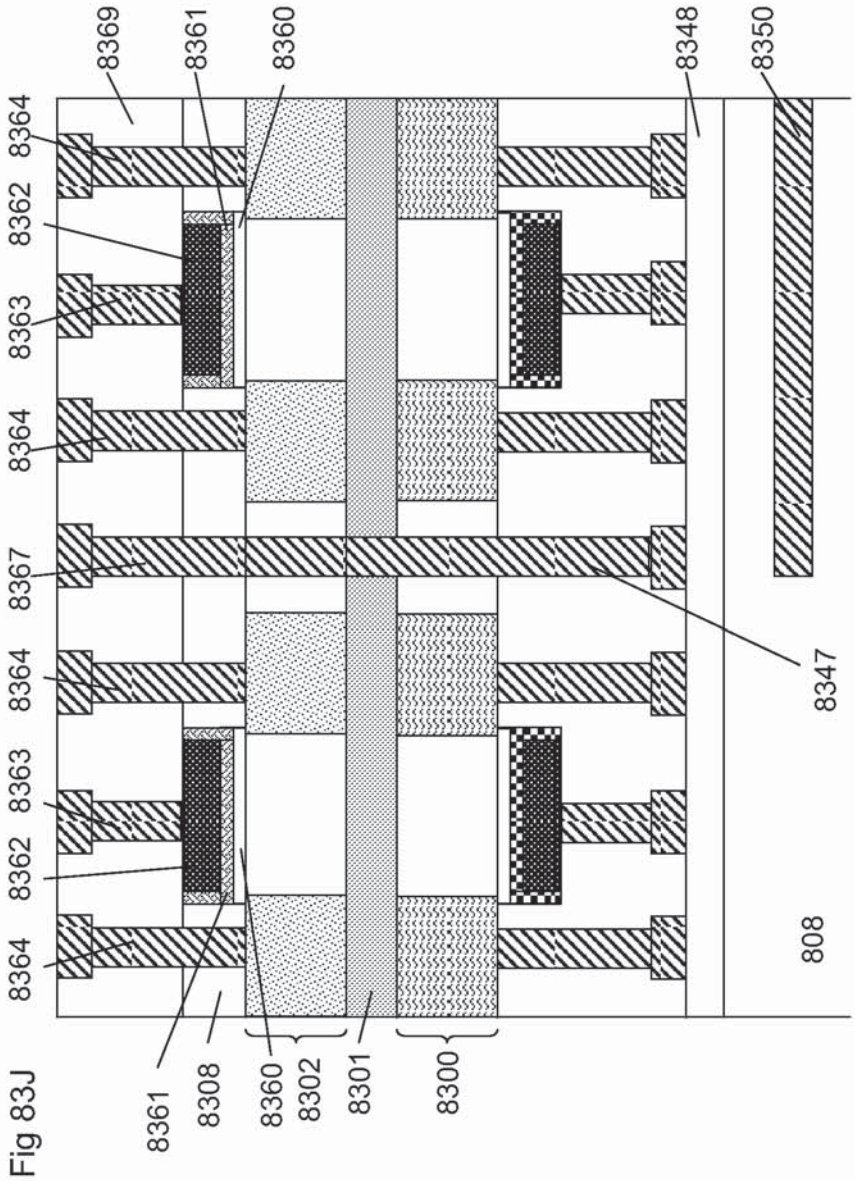

8369
8361
8360
8348
8350
8364
8362
8363
8364
8367
8364
8363
8362
8364
8347
808
8361
8308
8360
8302
8301
8300

Fig 83J

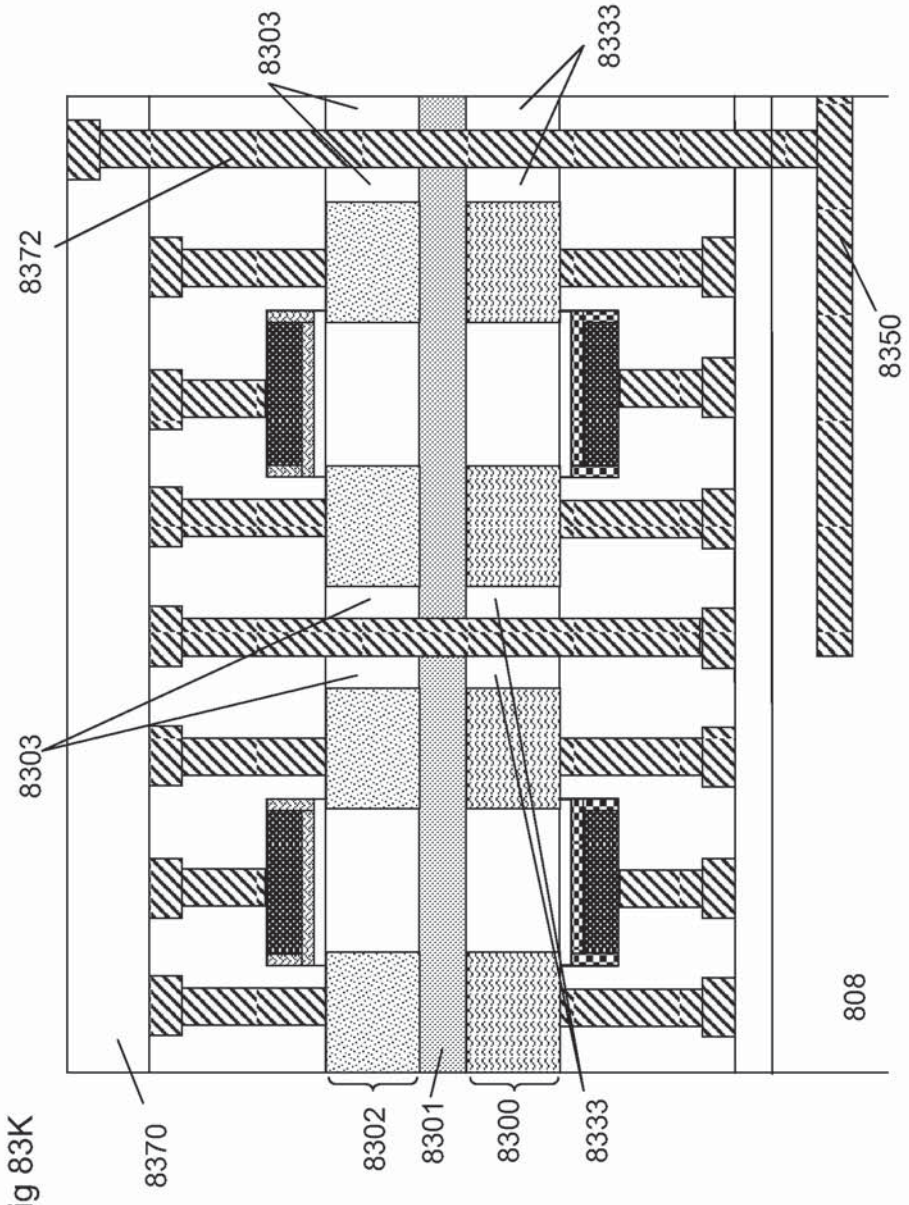


Fig 83K

Fig 83L

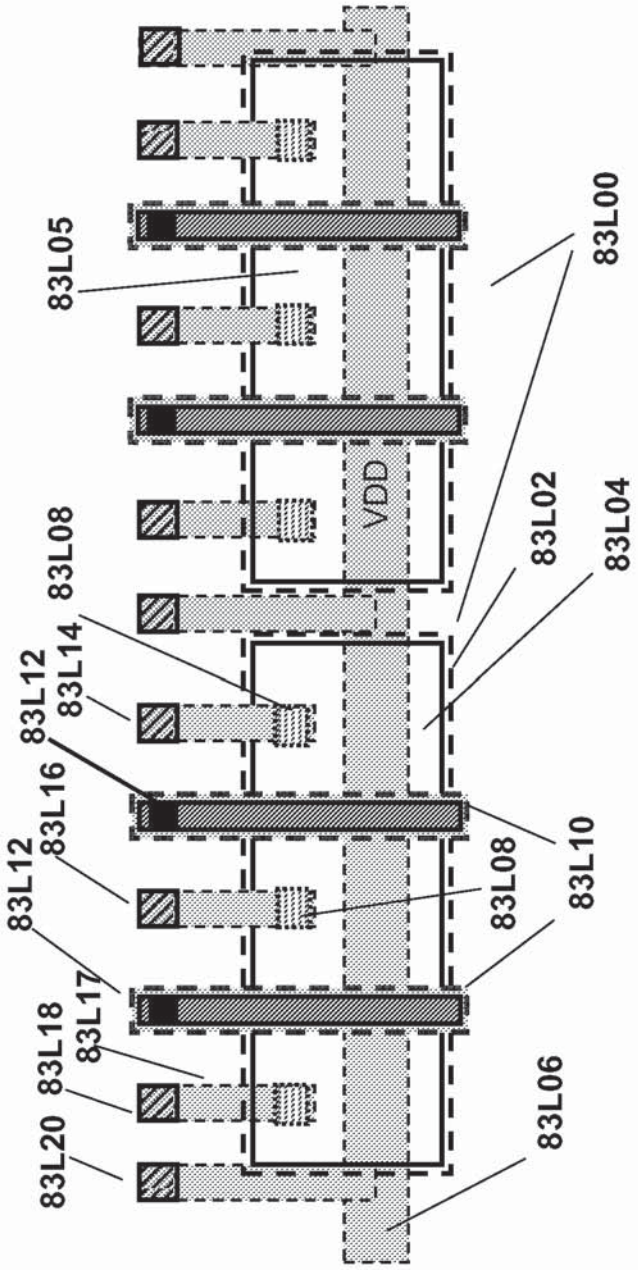
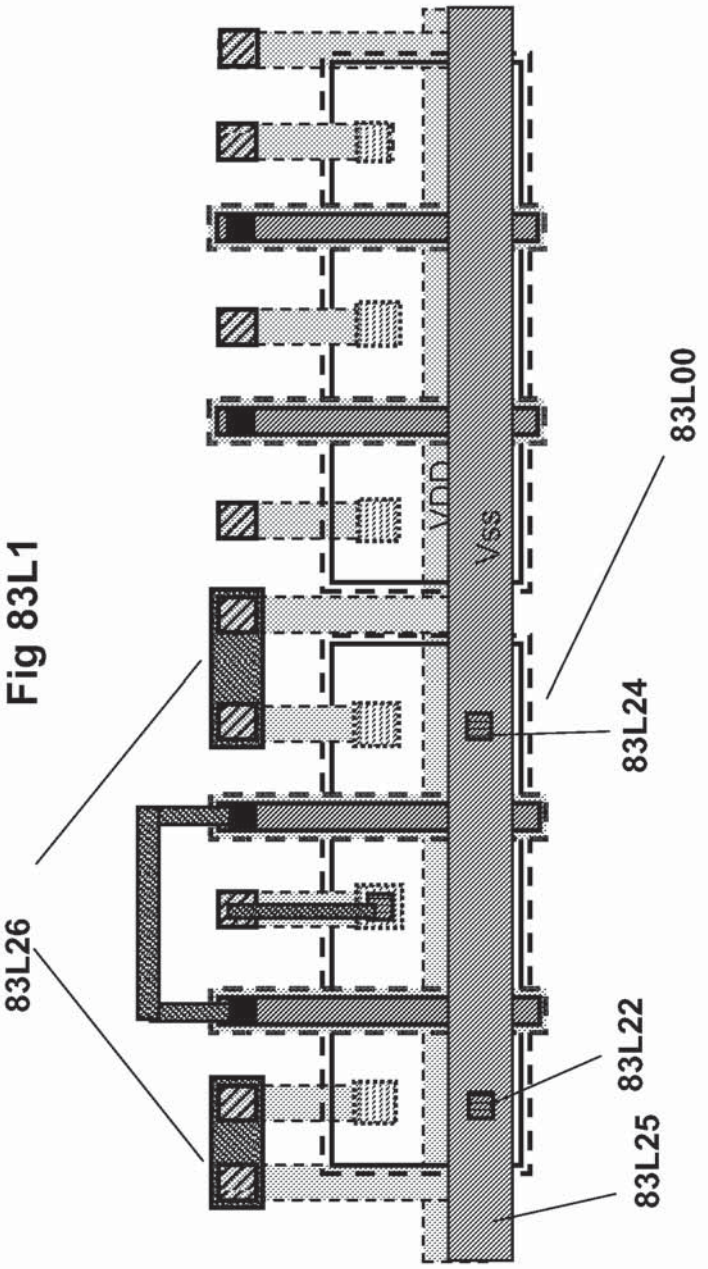

83L05
83L00
VDD
83L02
83L04
83L08
83L14
83L12
83L16
83L10
83L12
83L08
83L17
83L18
83L06
83L20

Fig 83L1



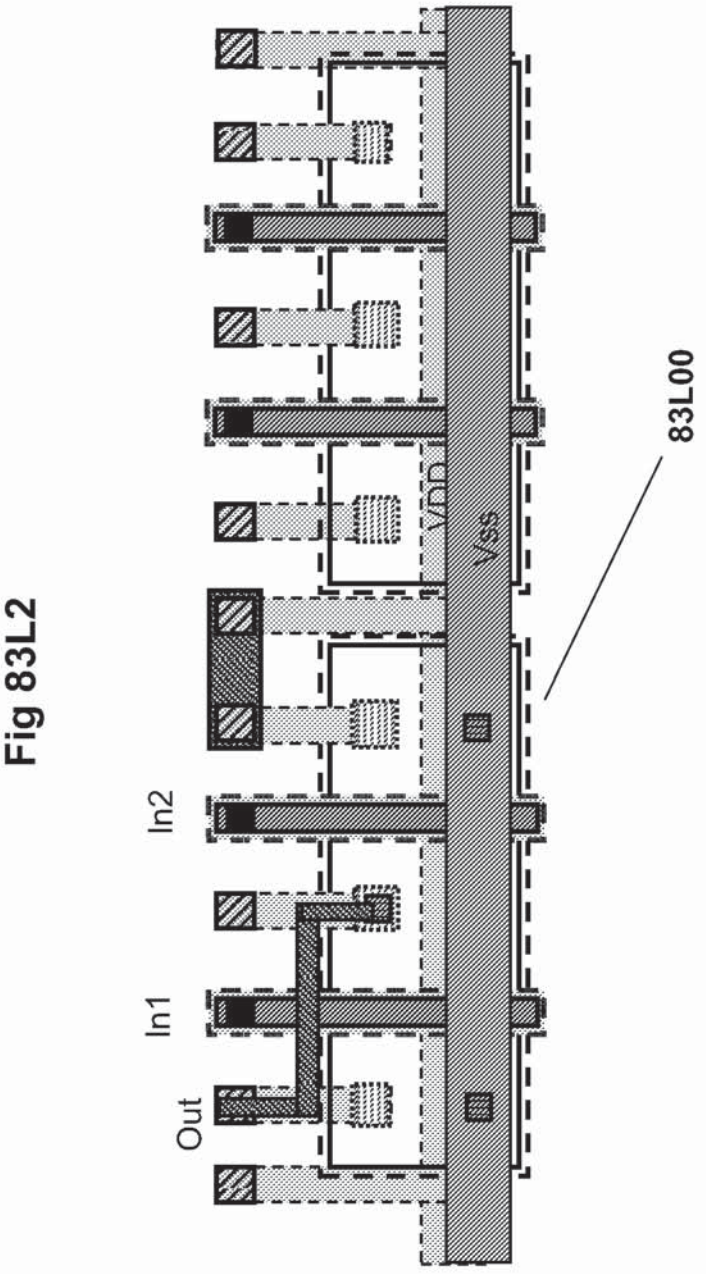


Fig 83L2

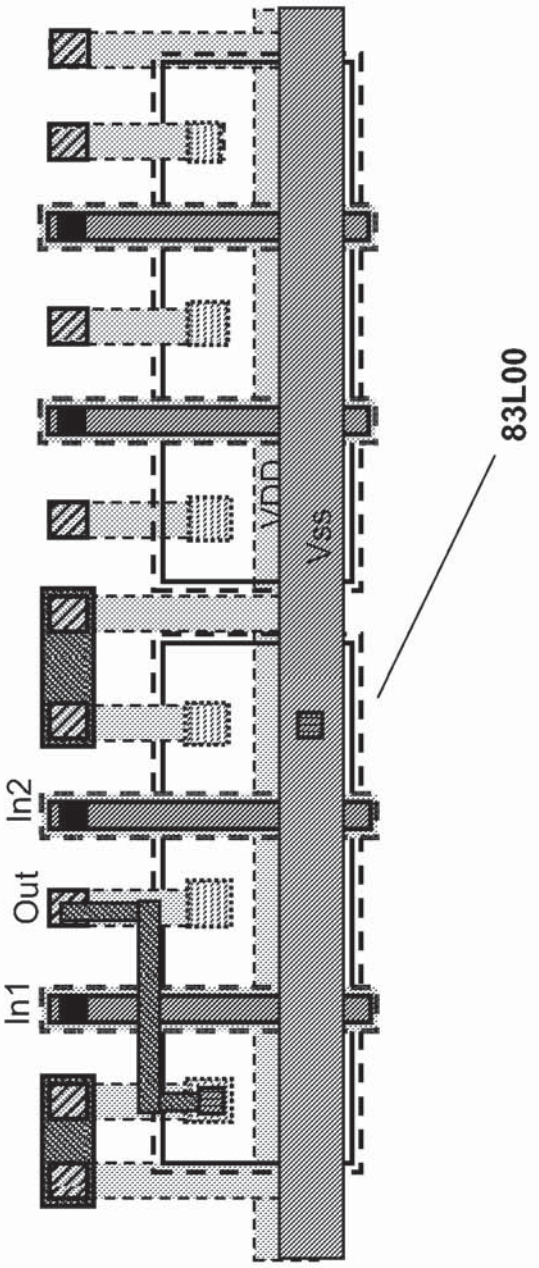
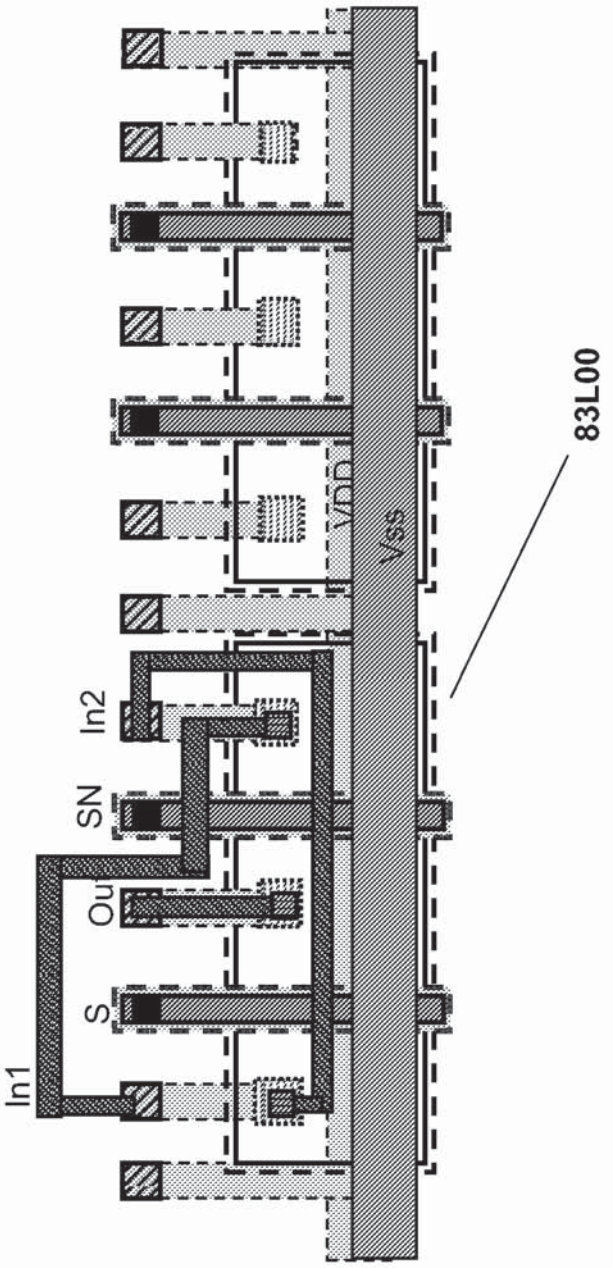
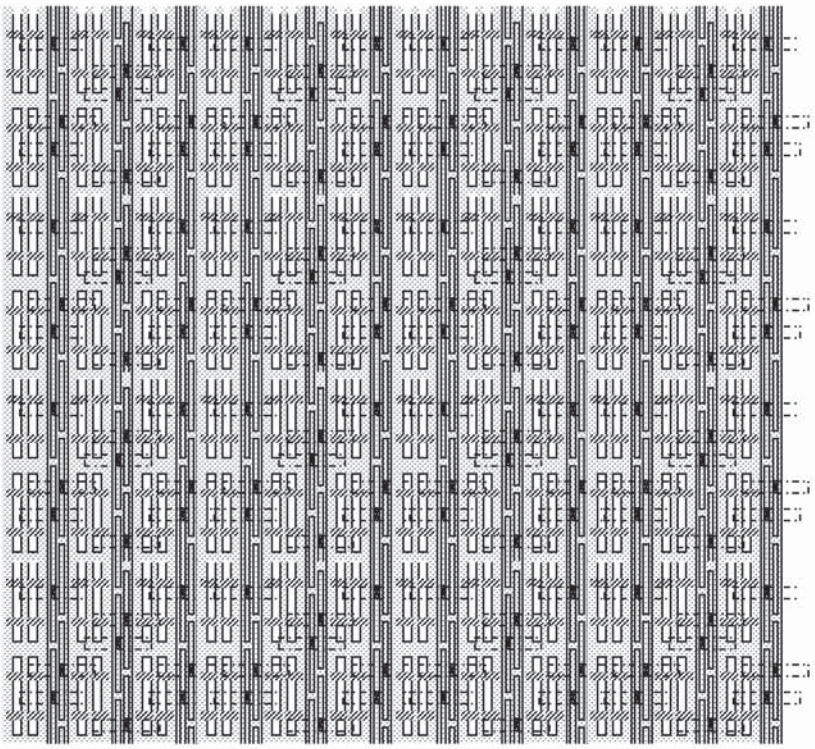


Fig 83L3

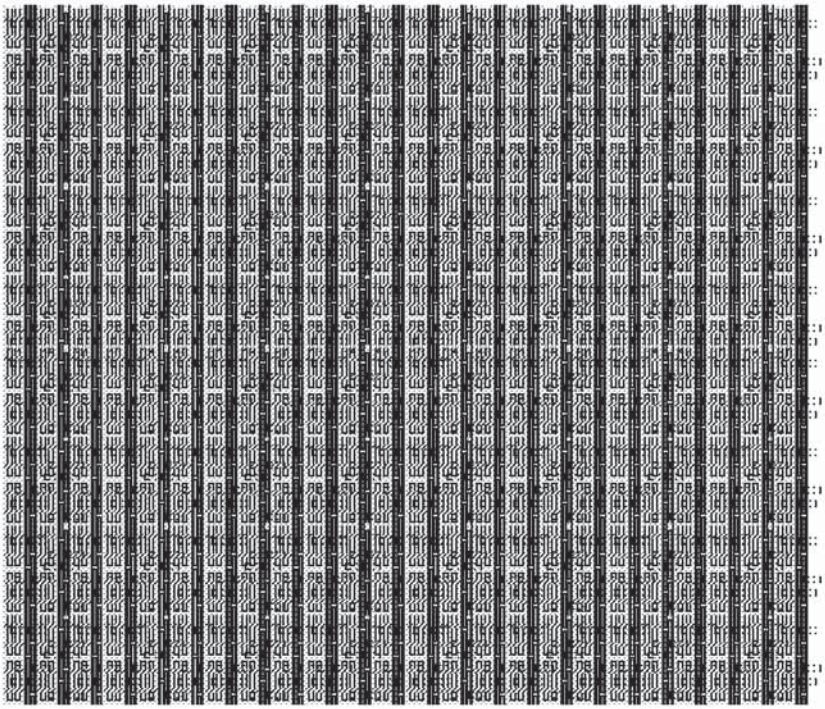
Fig 83L4





8402

Fig 84A



8402

Fig 84B

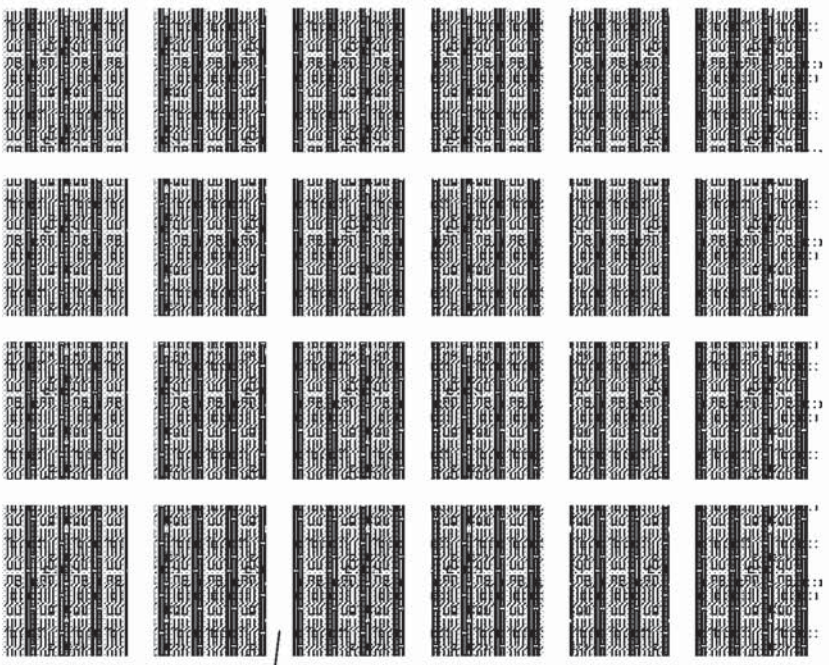


Fig 84C

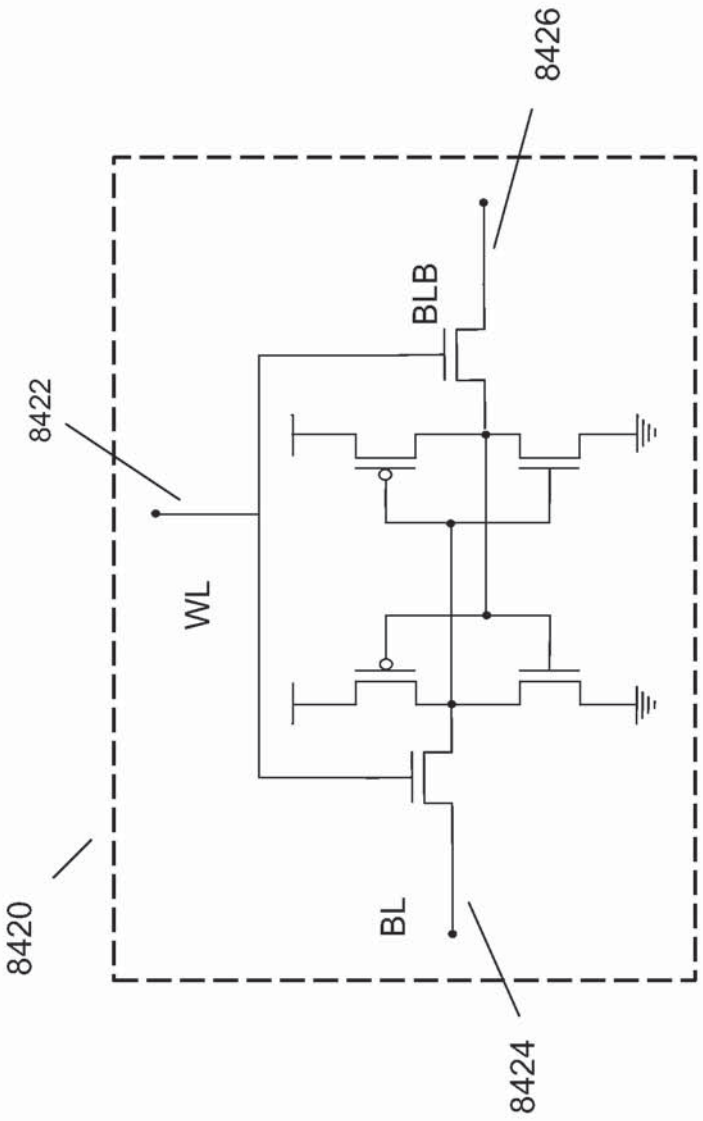


Fig 84D

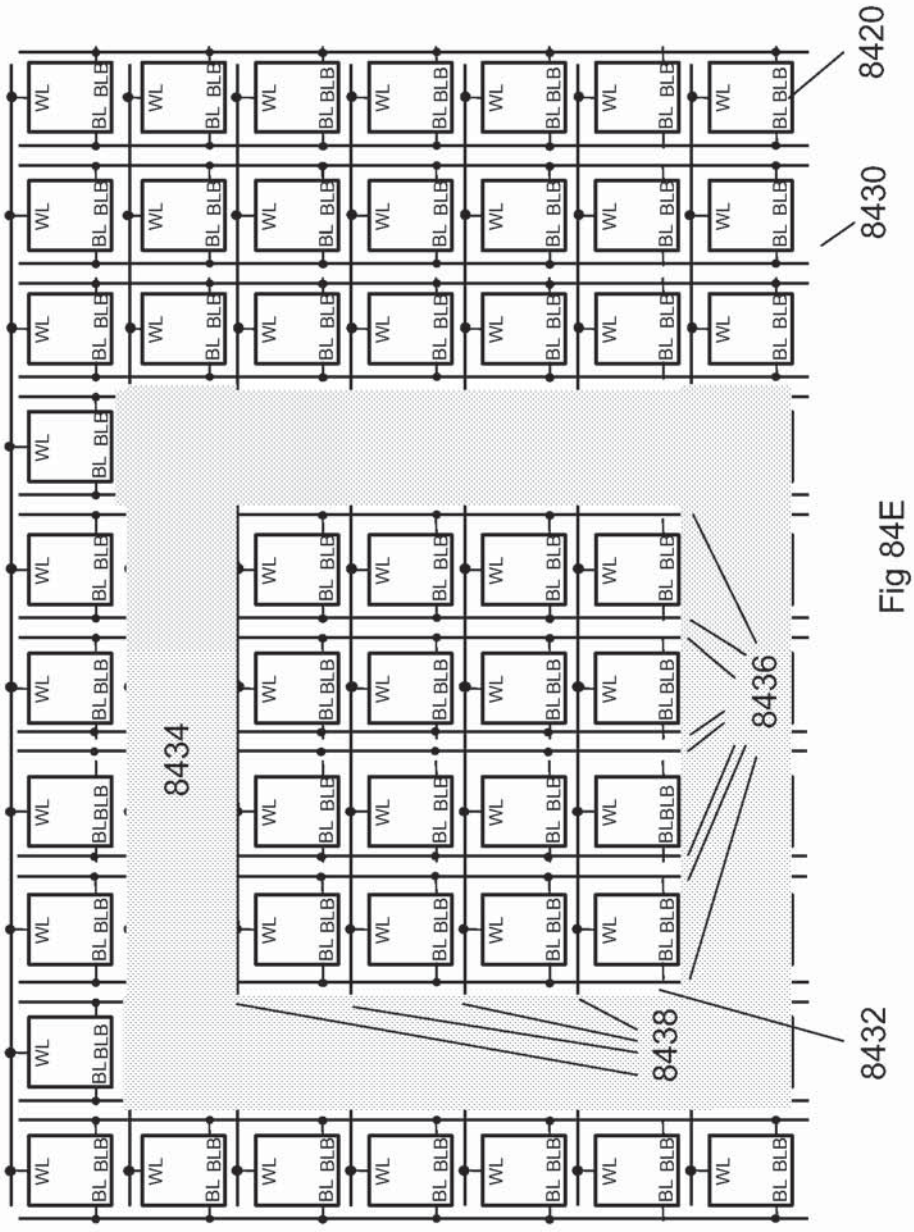


Fig 84E

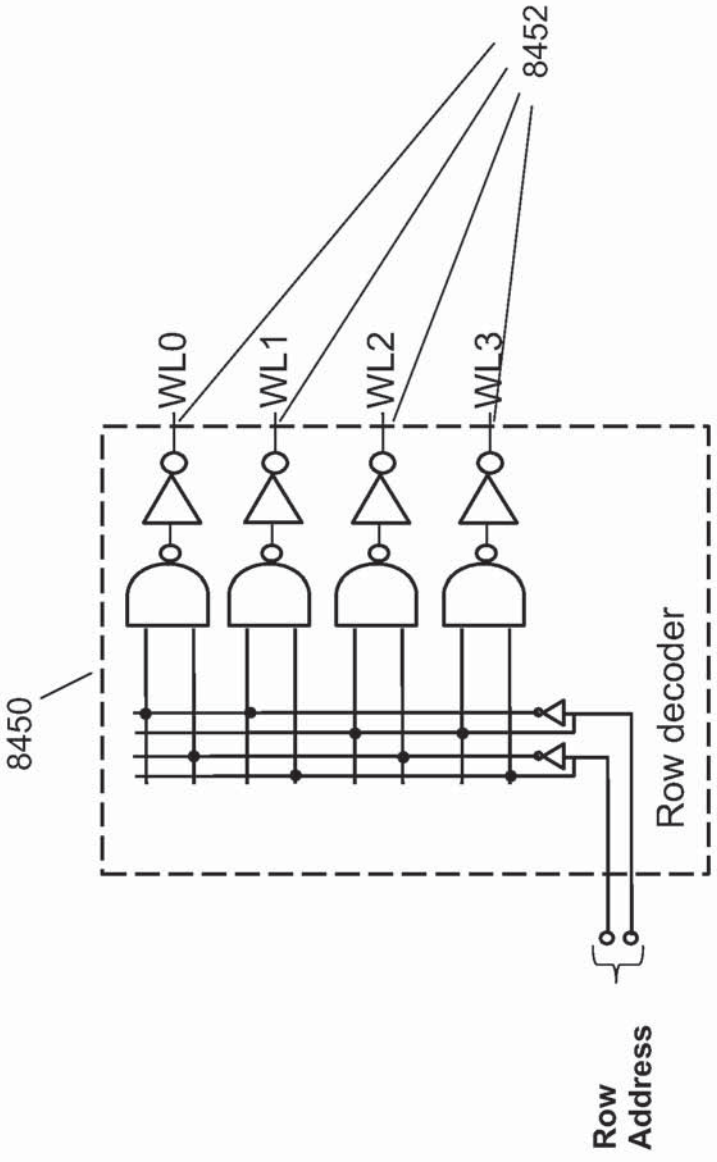


Fig 84F

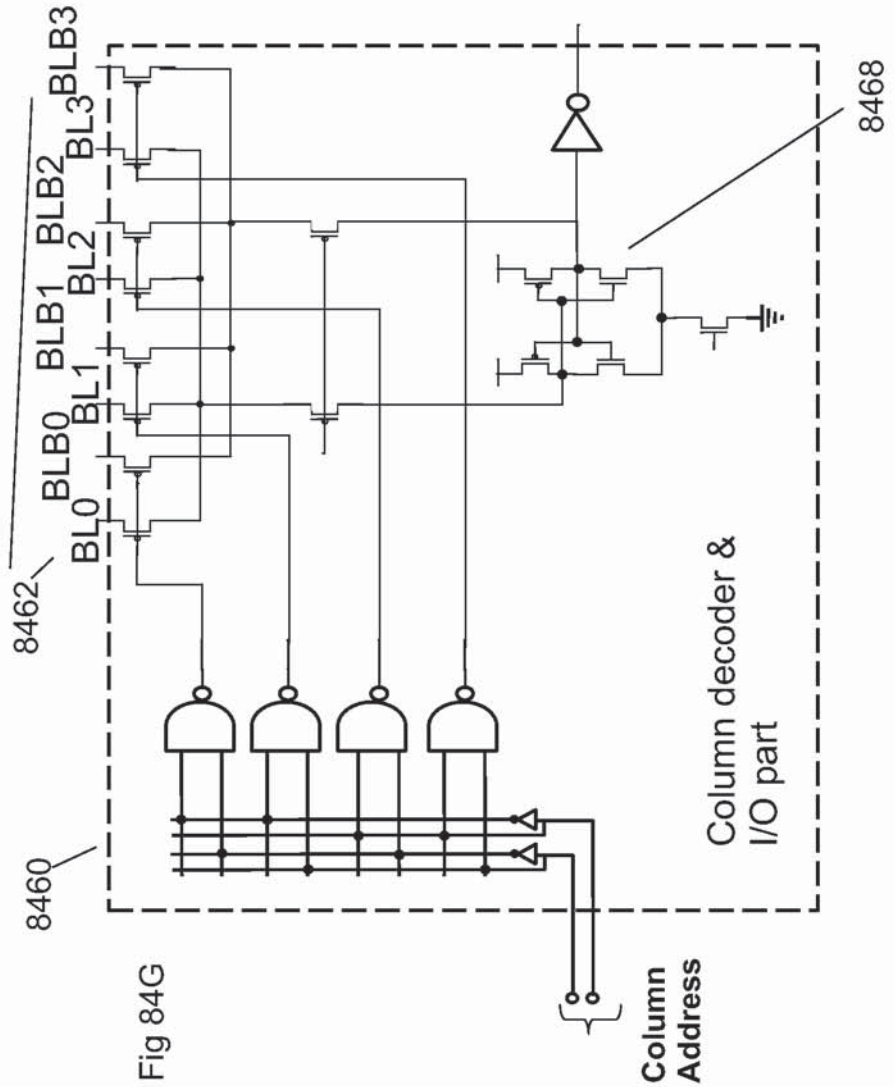

BLB3
BL3
BLB2
BL2
BLB1
BL1
BLB0
BL0
8462
8460
8468
Column decoder &
I/O part
Column
Address

Fig 84G

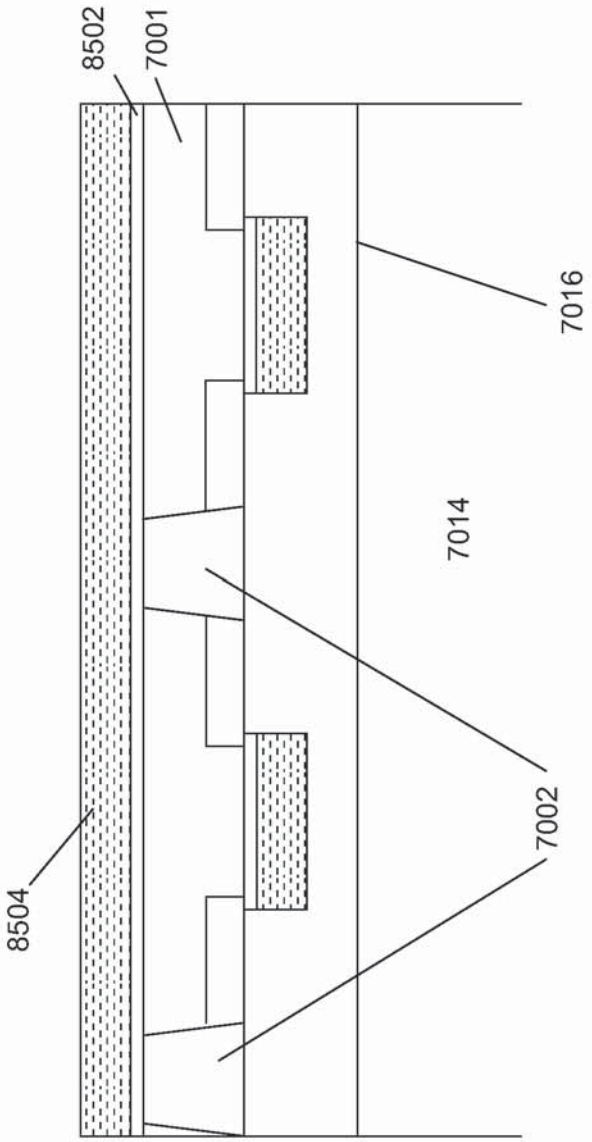


Fig 85A

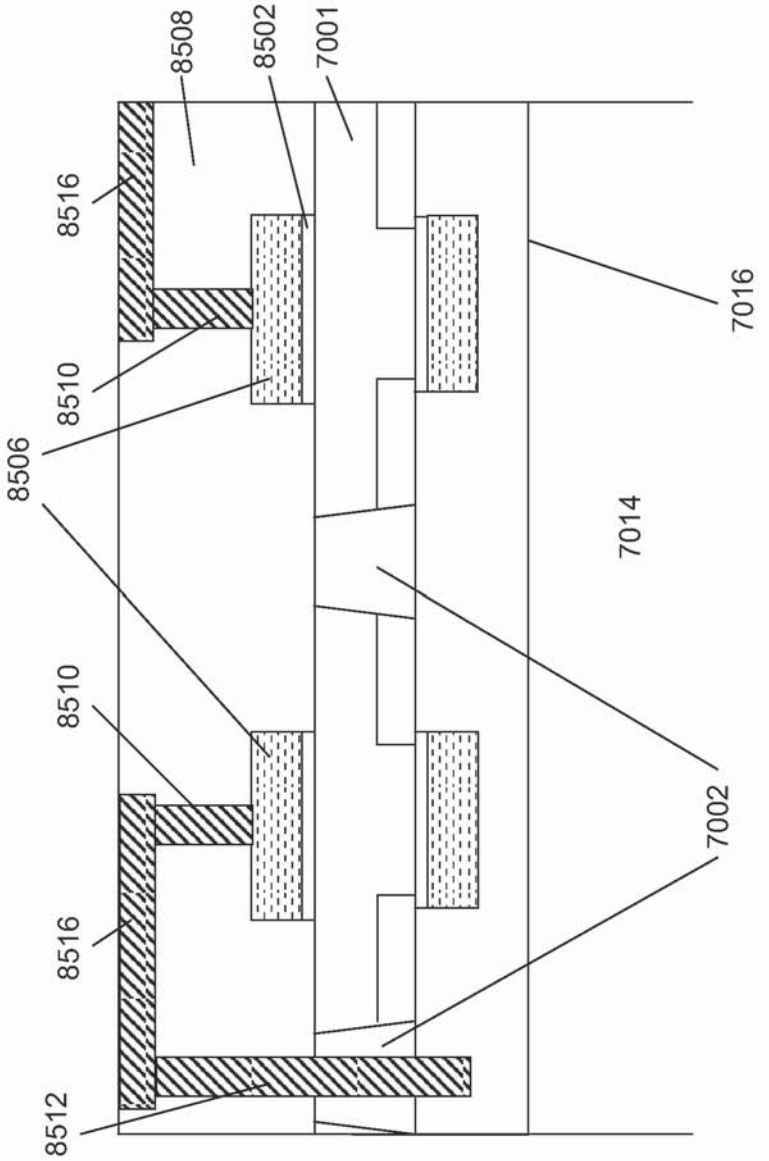


Fig 85B

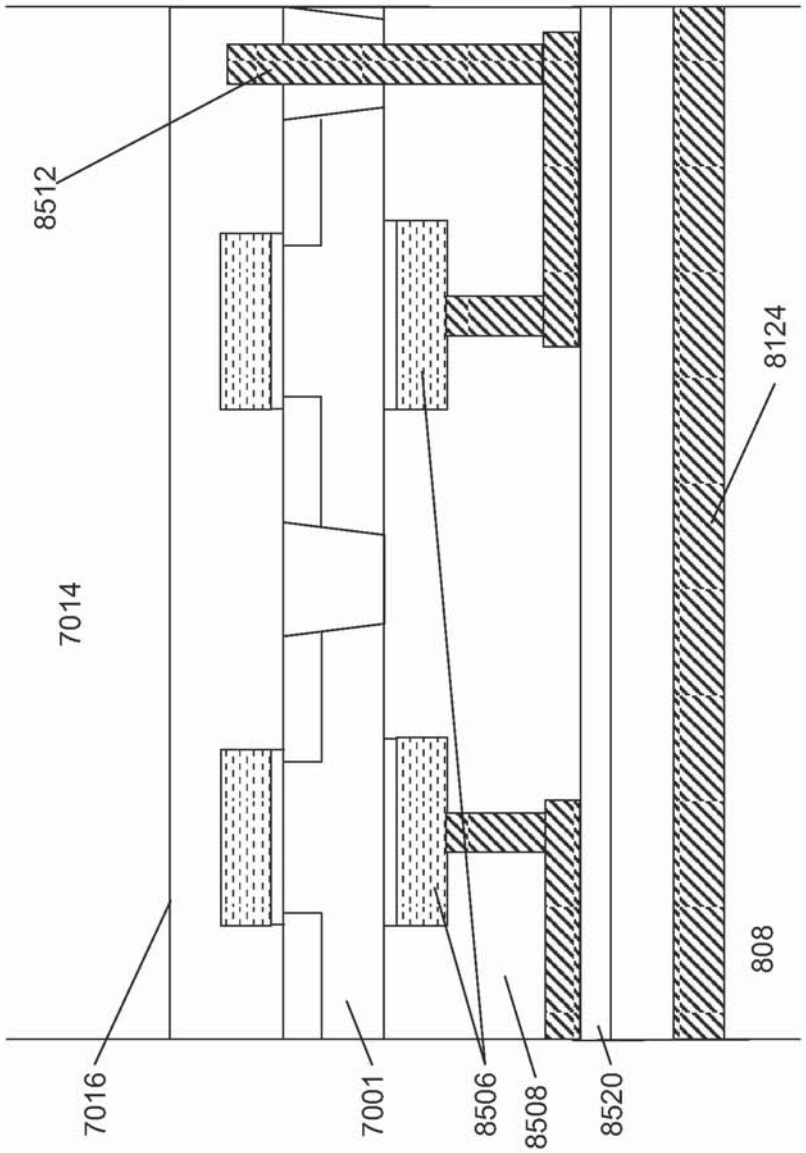


Fig 85C

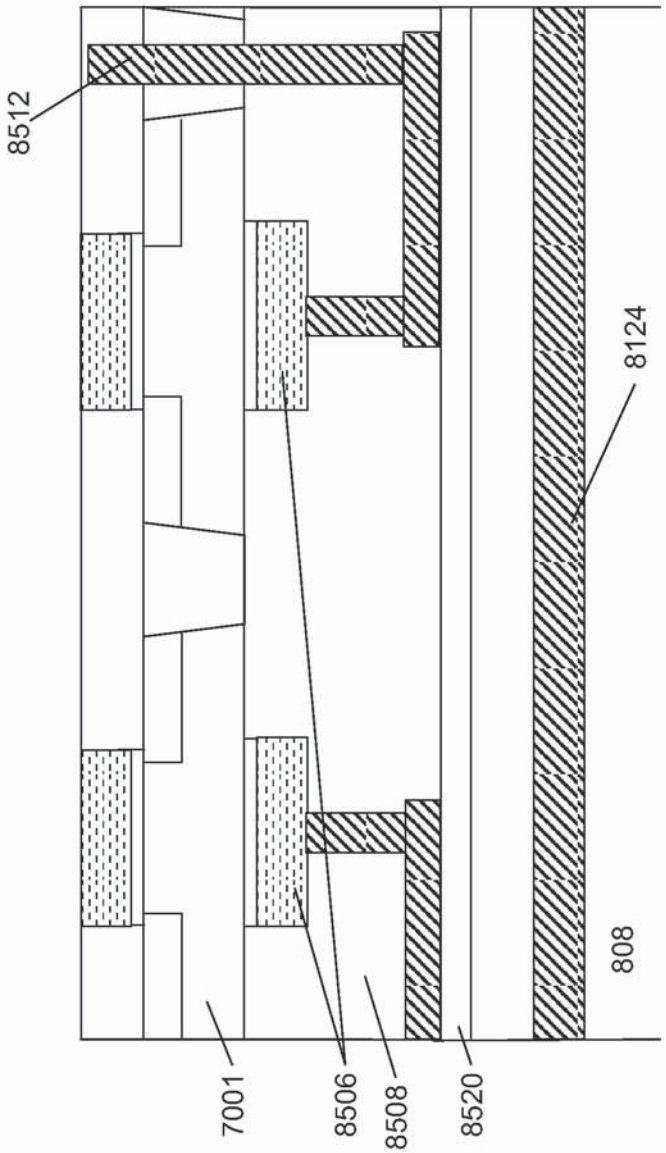


Fig 85D

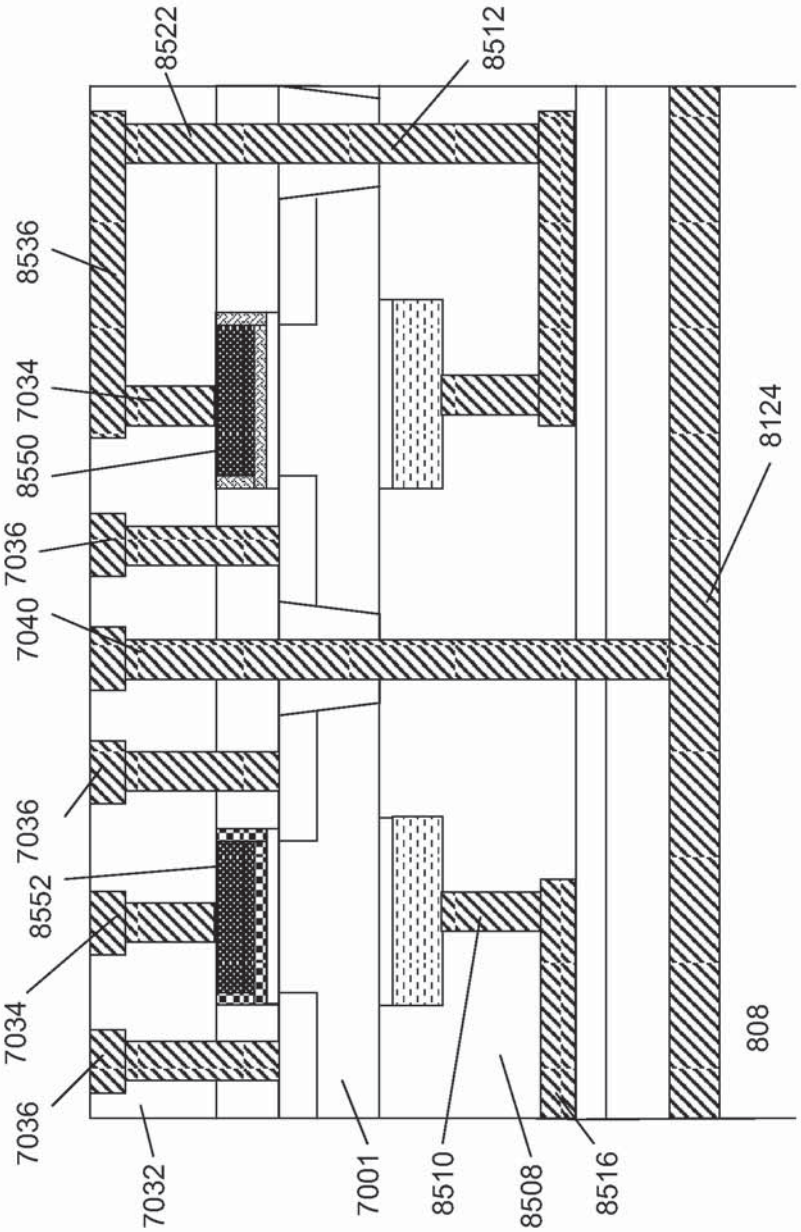

8522
8512
8536
7034
8550
7036
7040
8124
7036
8552
7034
7036
808
7032
7001
8510
8508
8516

Fig 85E

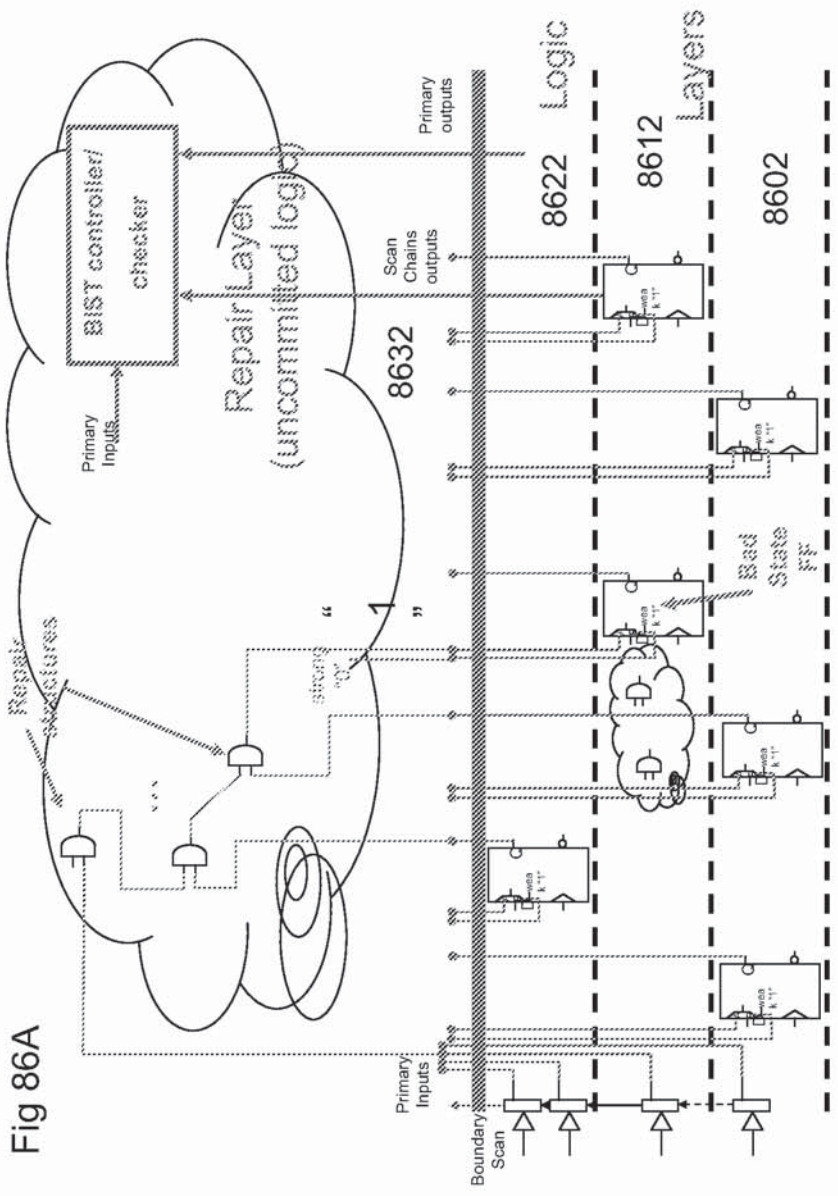

BIST controller/ checker
Repair Layer (uncommitted logic)
Primary Inputs
Scan Chains outputs
Primary outputs
8632
8622 Logic
8612
Layers
8602
Bad State FF
Repair Selectors
Primary Inputs
Boundary Scan

Fig 86A

Fig 86B

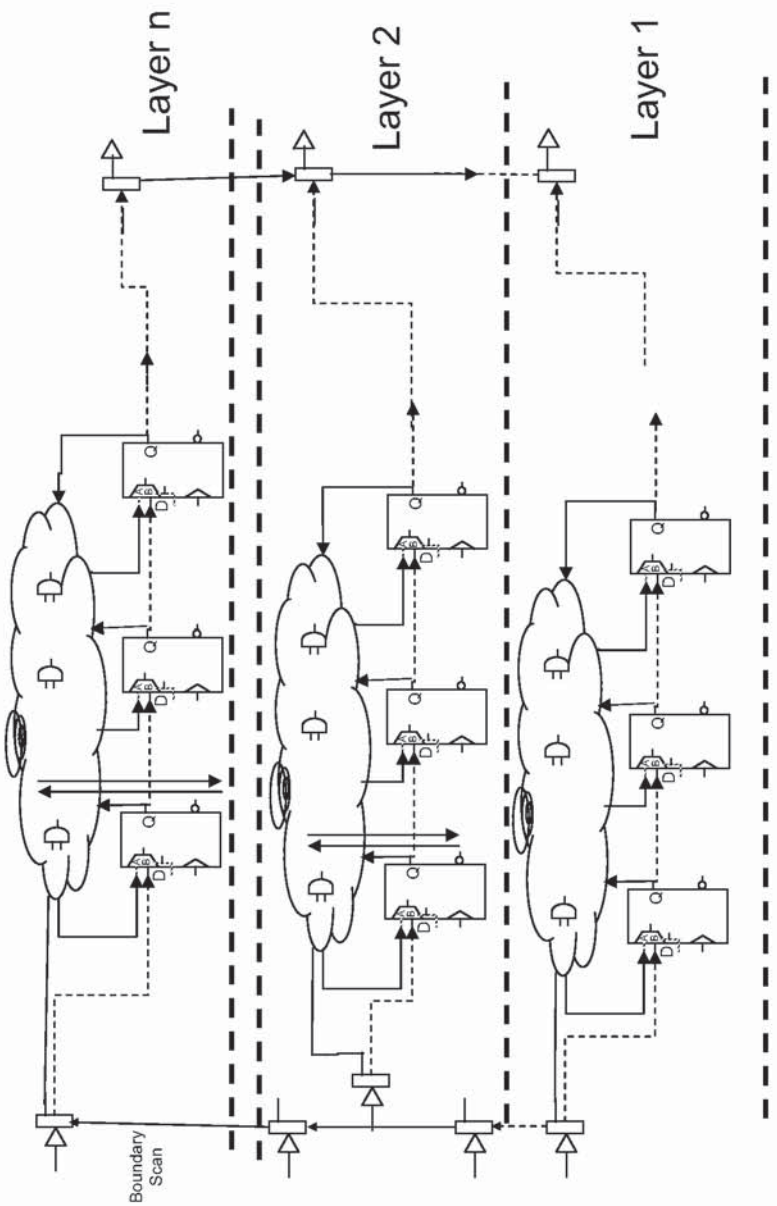
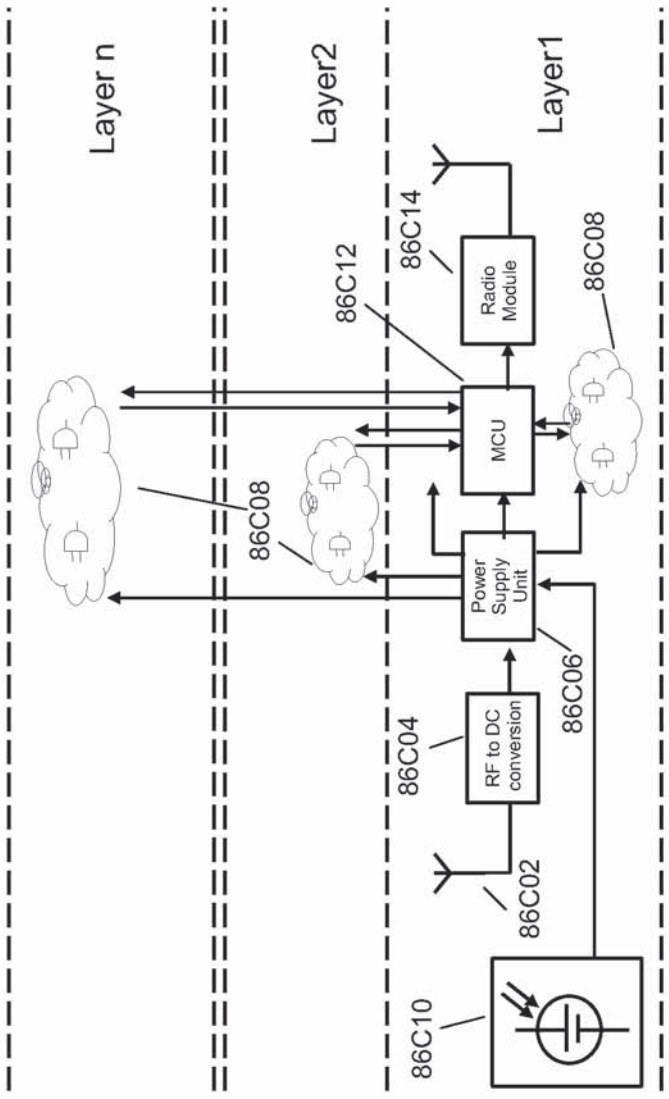


Fig 86C


Layer n
Layer2
Layer1
86C08
86C12
86C14
86C08
Radio Module
MCU
Power Supply Unit
86C04
RF to DC conversion
86C06
86C02
86C10

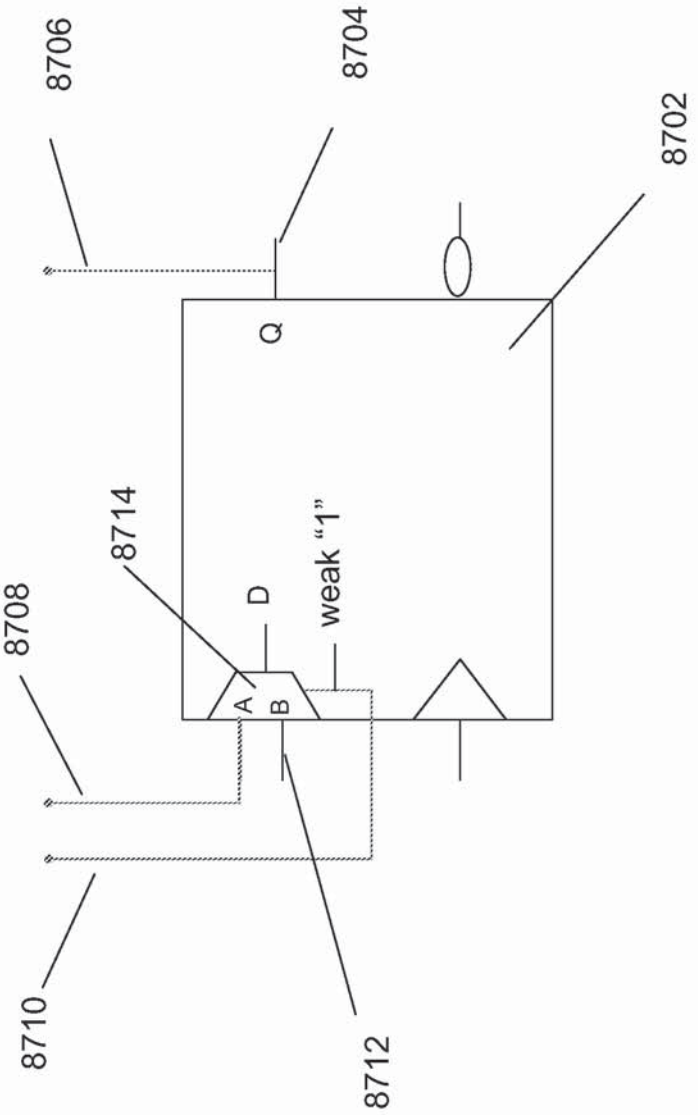
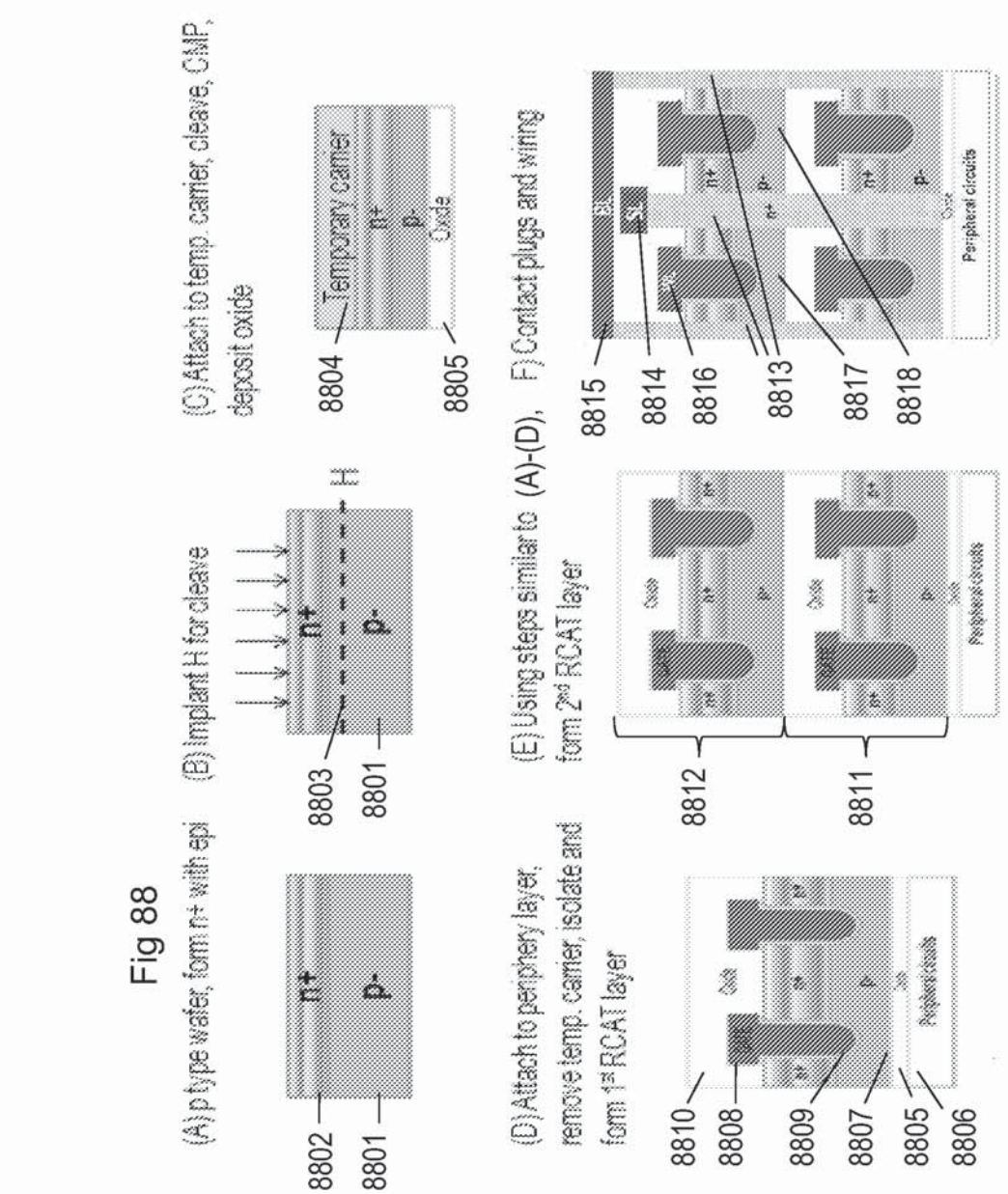


Fig 87

Fig 88


(A) p type wafer, form n+ with epi
(B) Implant H for cleave
(C) Attach to temp carrier, cleave, CMP, deposit oxide
n+
p-
H
Temporary carrier
Oxide
8801
8802
8803
8804
8805
(D) Attach to periphery layer, remove temp. carrier, isolate and form 1st RCAT layer
(E) Using steps similar to (A)-(D), form 2nd RCAT layer
(F) Contact plugs and wiring
Gate
Peripheral circuits
8806
8807
8808
8809
8810
8811
8812
8813
8814
8815
8816
8817
8818

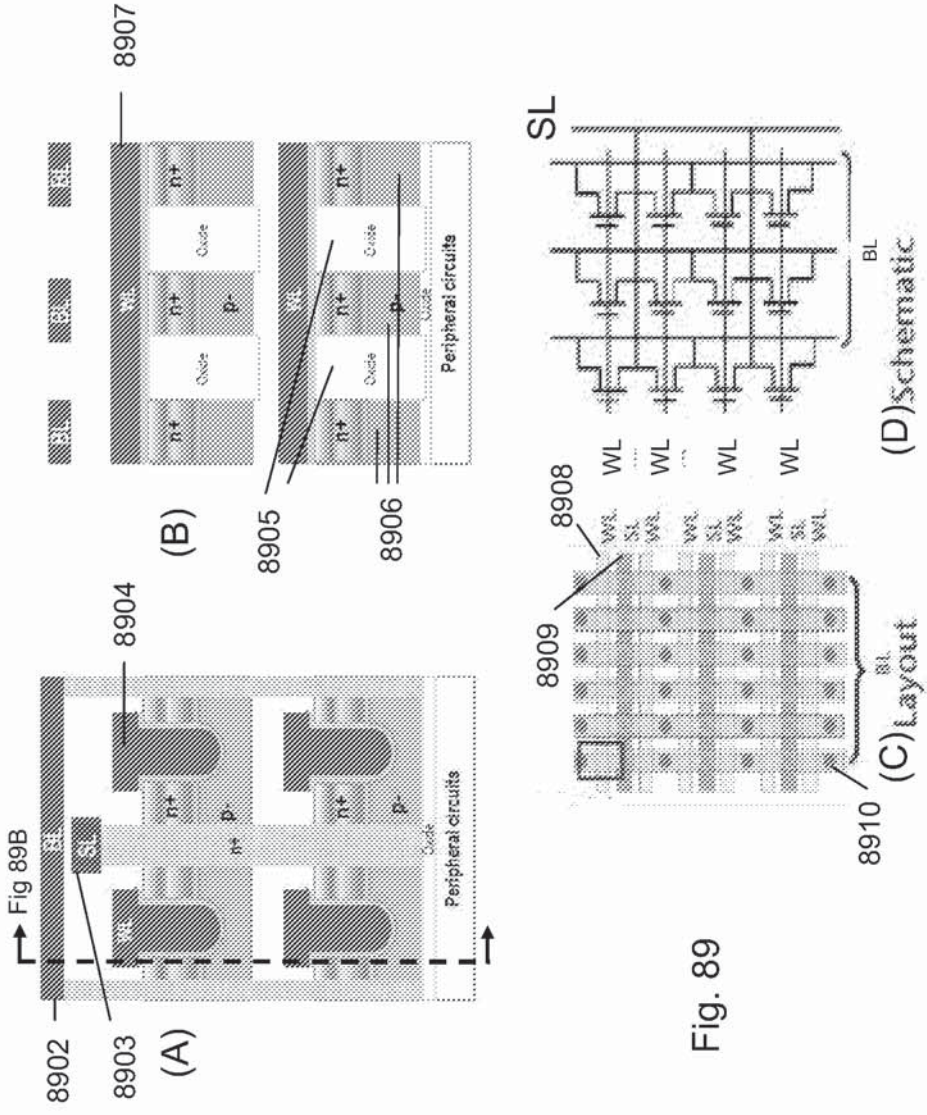

Fig 89B
8902
8903
8904
8905
8906
8907
8908
8909
8910
(A)
(B)
(C)Layout
(D)Schematic
Peripheral circuits
SL
BL
WL

Fig. 89

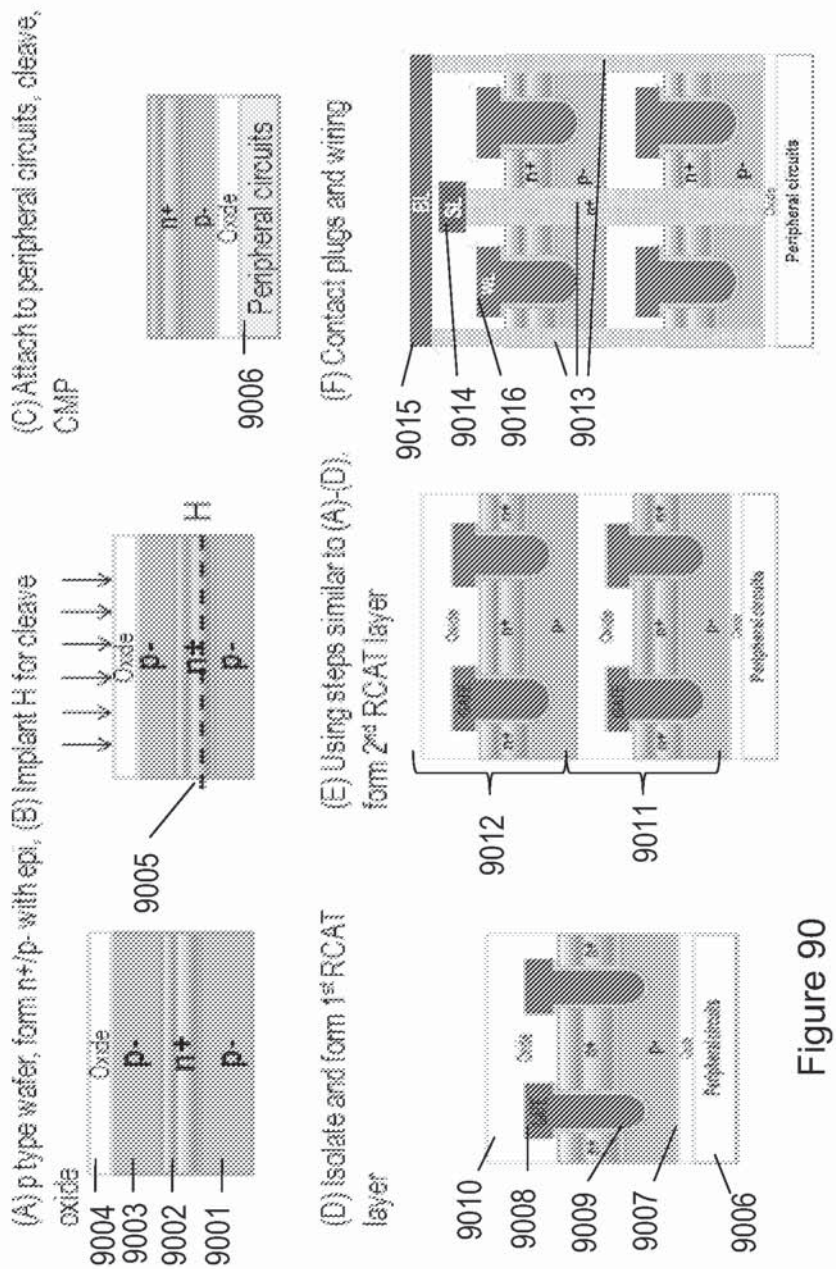

(A) p type wafer, form n+/p- with epi, (B) implant H for cleave
oxide
Oxide
p-
n+
p-
H
9004
9003
9002
9001
9005
(C) Attach to peripheral circuits, cleave, CMP
n+
p-
Oxide
Peripheral circuits
9006
(D) Isolate and form 1st RCAT layer
(E) Using steps similar to (A)-(D), form 2nd RCAT layer
(F) Contact plugs and wiring
9015
9014
9016
9013
9012
9011
9010
9008
9009
9007
9006

Figure 90

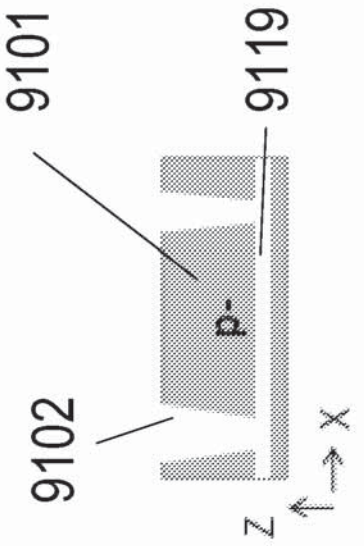


Figure 91A

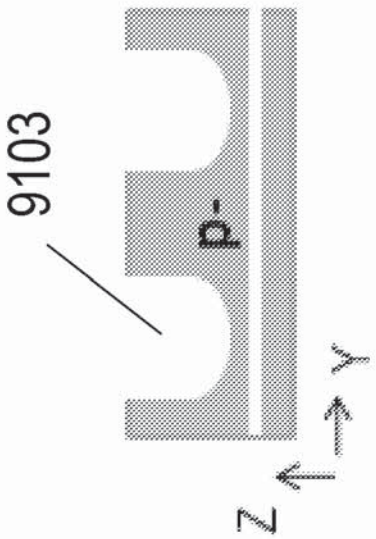


Figure 91B

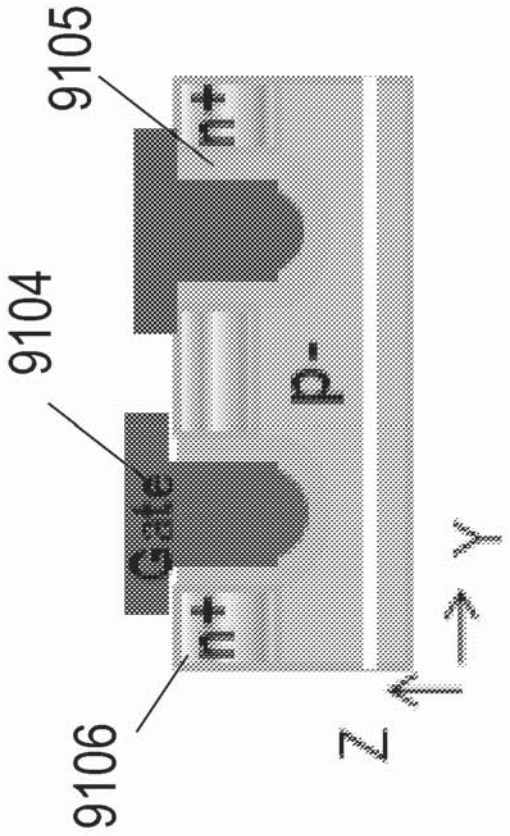


Figure 91C

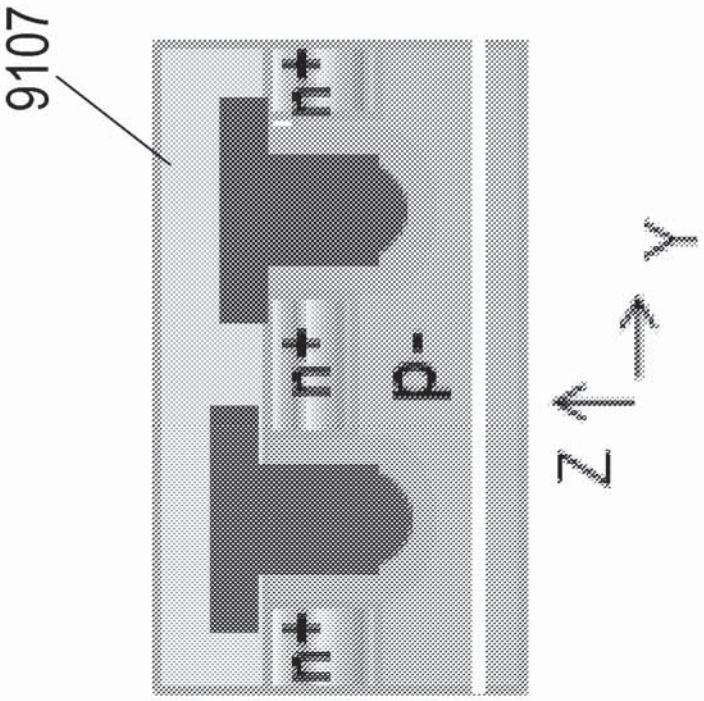


Figure 91D

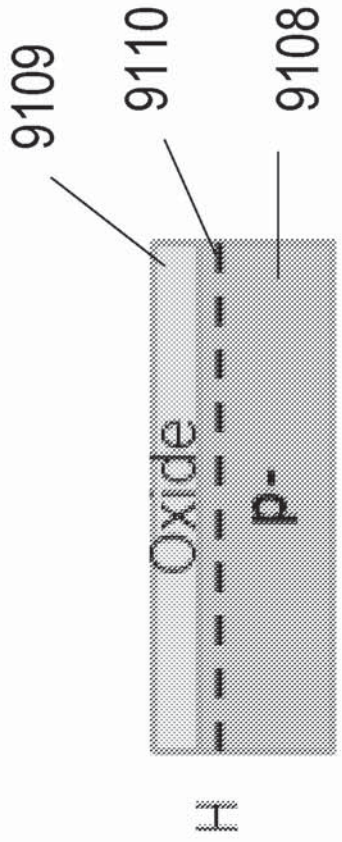


Figure 91E

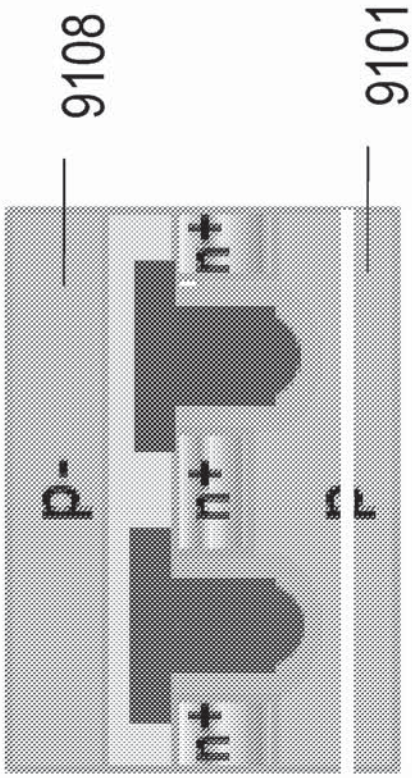


Figure 91F

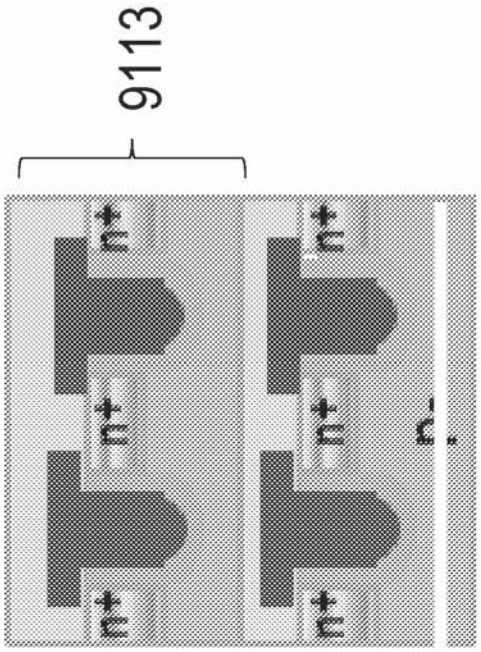


Figure 91G

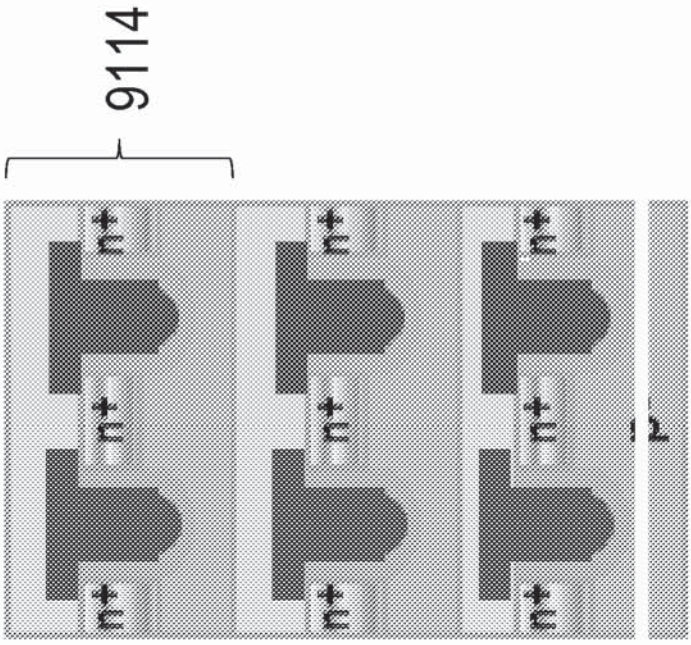


Figure 91H

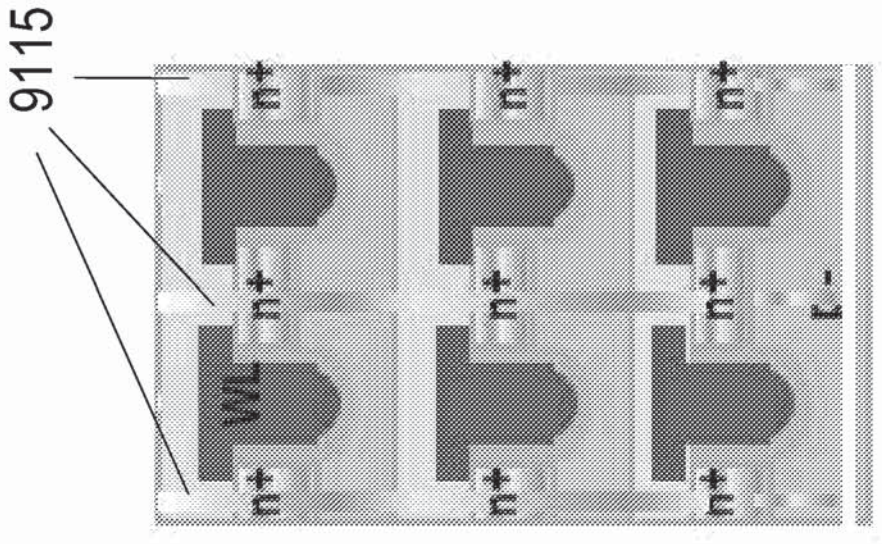


Figure 91I

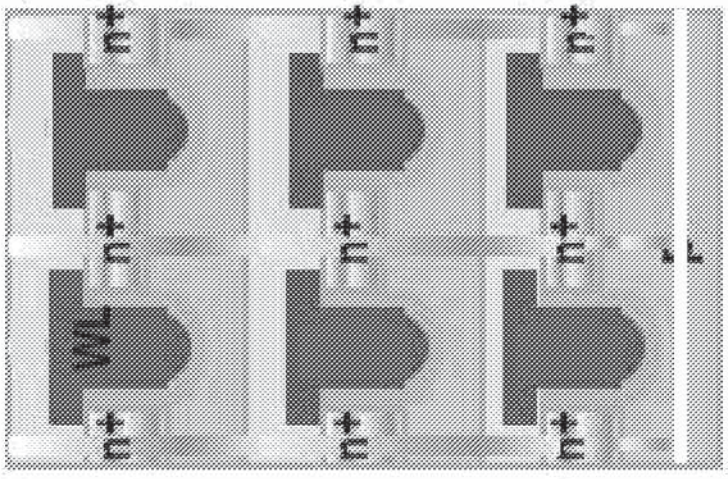


Figure 91J

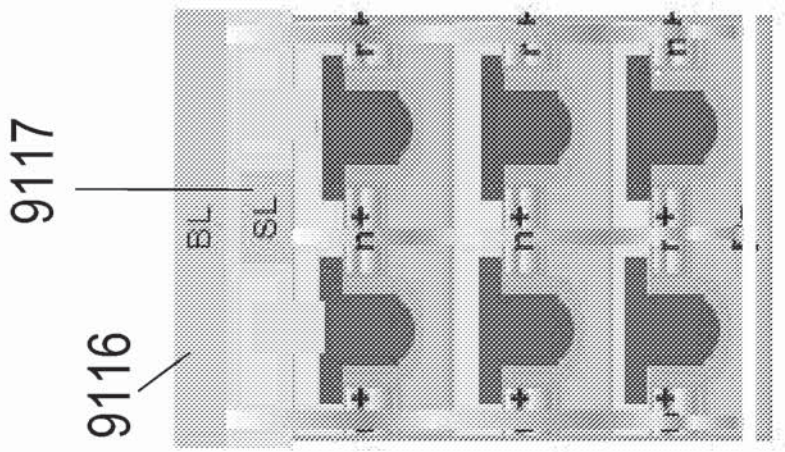


Figure 91K

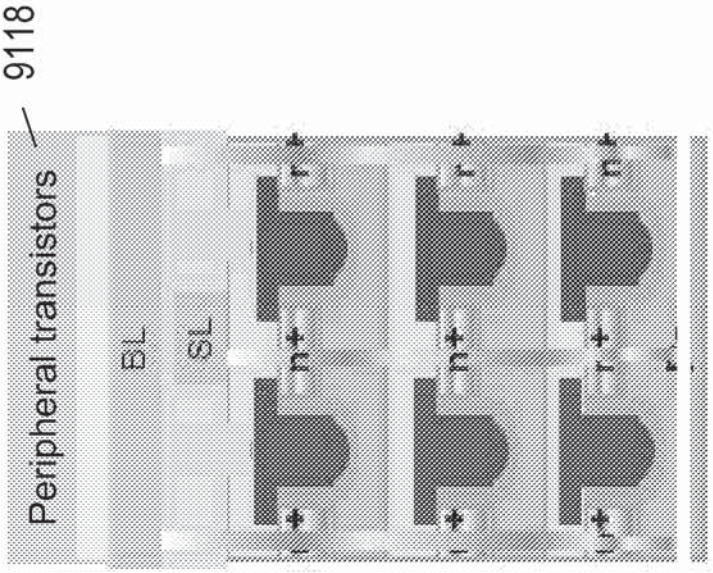


Figure 91L

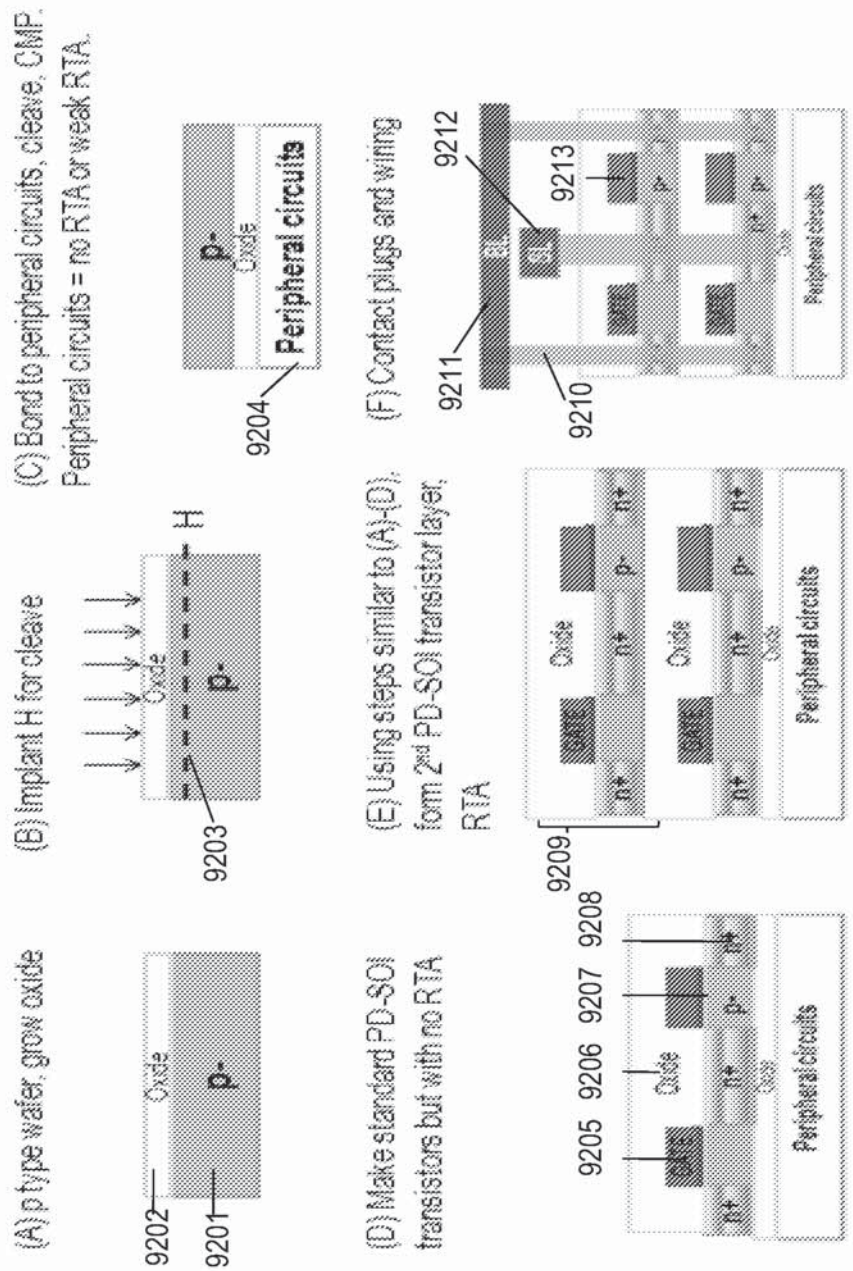

(A) p type wafer, grow oxide
(B) Implant H for cleave
(C) Bond to peripheral circuits, cleave, CMP. Peripheral circuits = no RTA or weak RTA.
(D) Make standard PD-SOI transistors but with no RTA
(E) Using steps similar to (A)-(D), form 2nd PD-SOI transistor layer, RTA
(F) Contact plugs and wiring
Oxide
p-
H
Peripheral circuits
9201
9202
9203
9204
9205
9206
9207
9208
9209
9210
9211
9212
9213
n+
p-
Gate
BL
SL

Figure 92

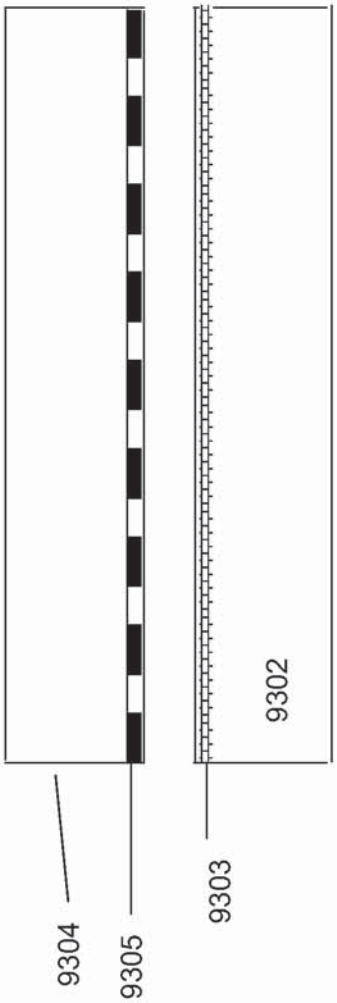


Fig 93A

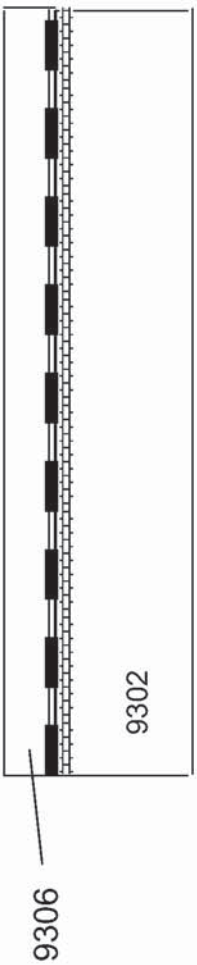


Fig 93B

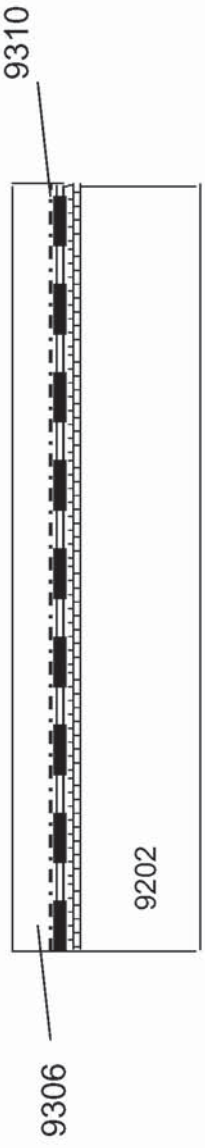


Fig 93C

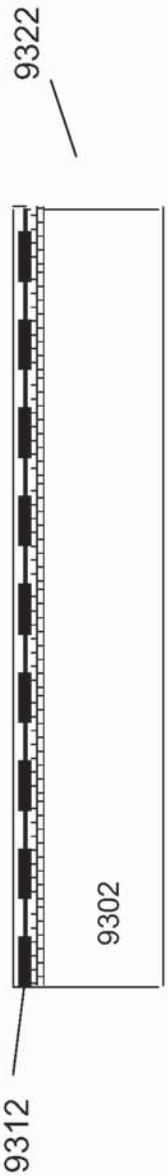
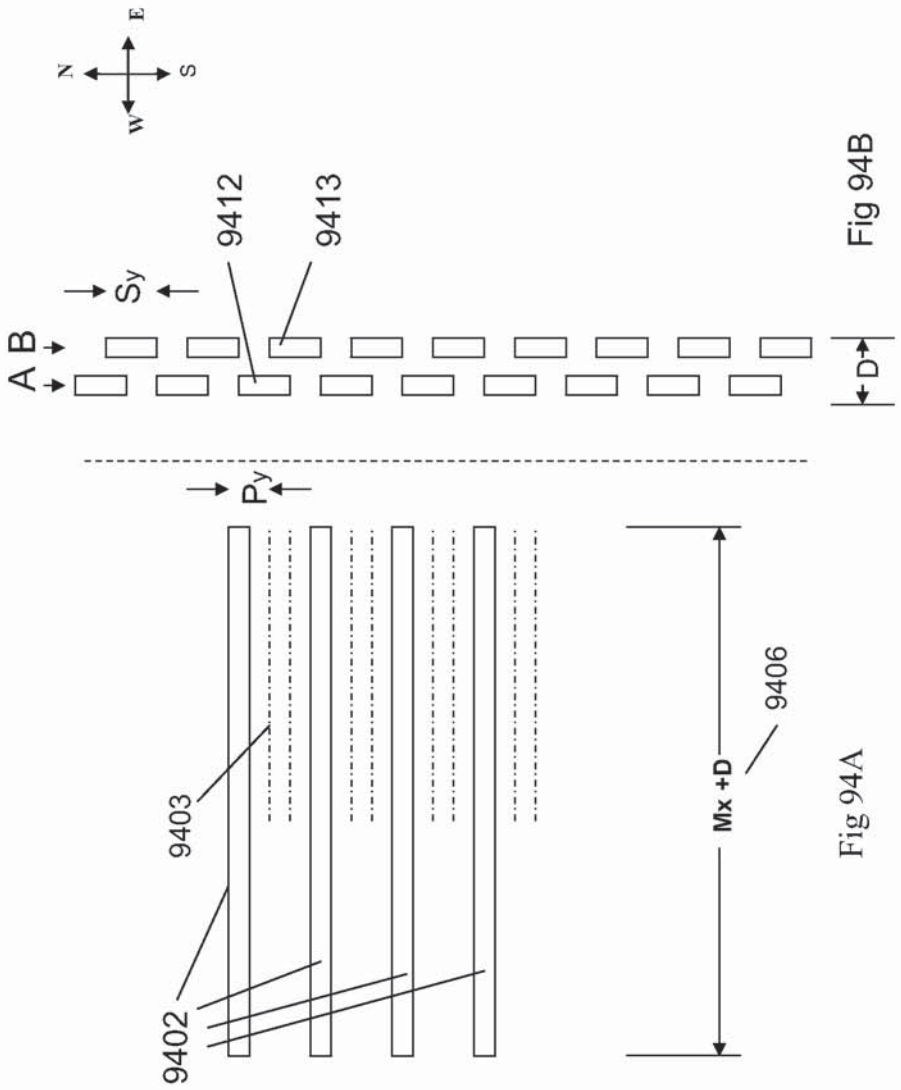


Fig 93D


N
E
S
W
A B
Sy
9412
9413
D
Fig 94B
Py
9403
9402
Mx +D
9406
Fig 94A

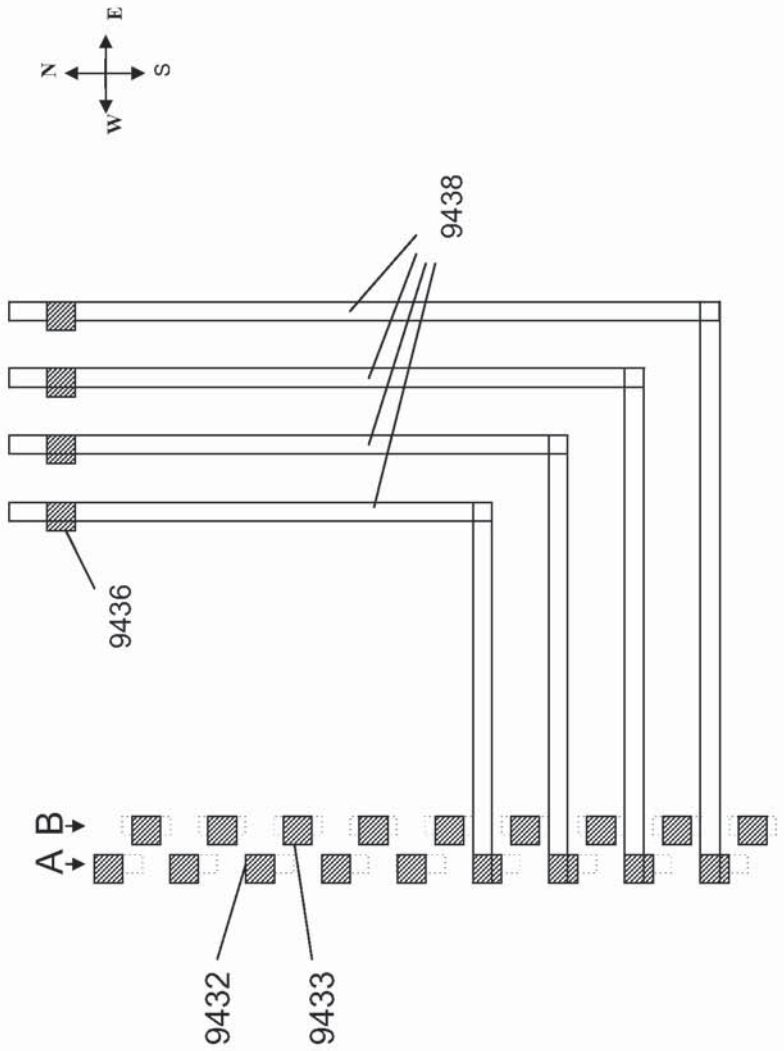


Fig 94C

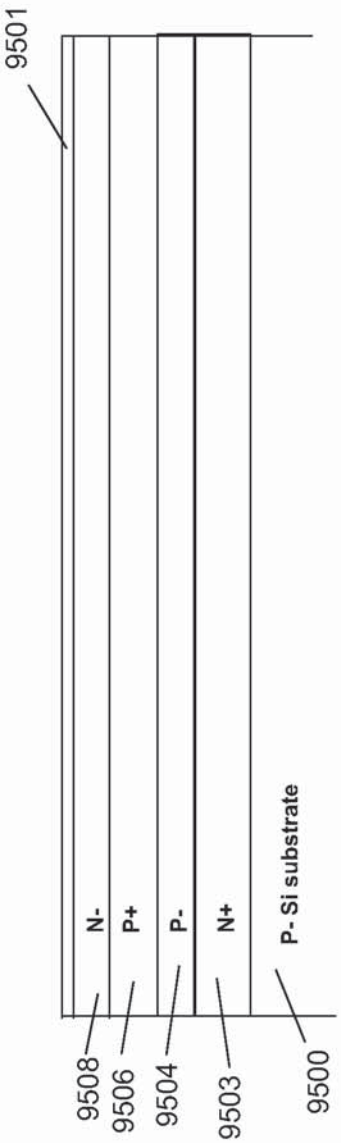


FIG. 95A

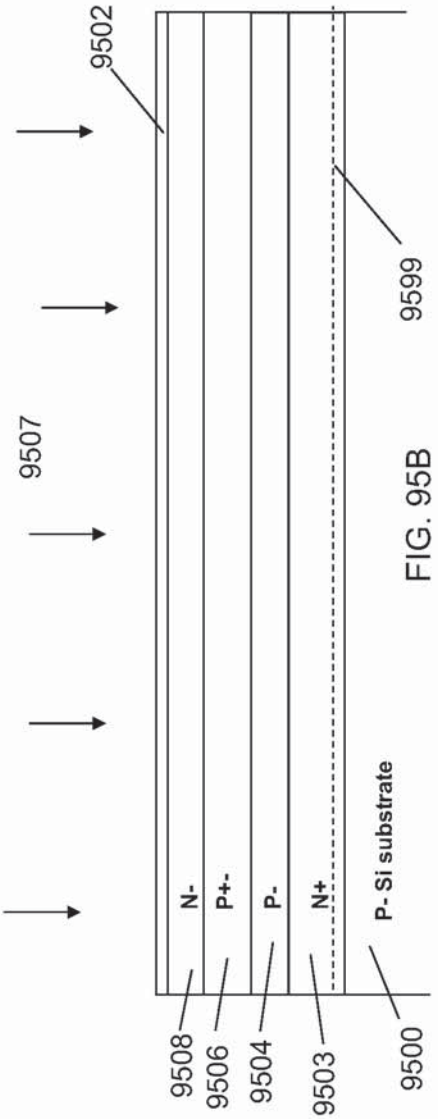


FIG. 95B

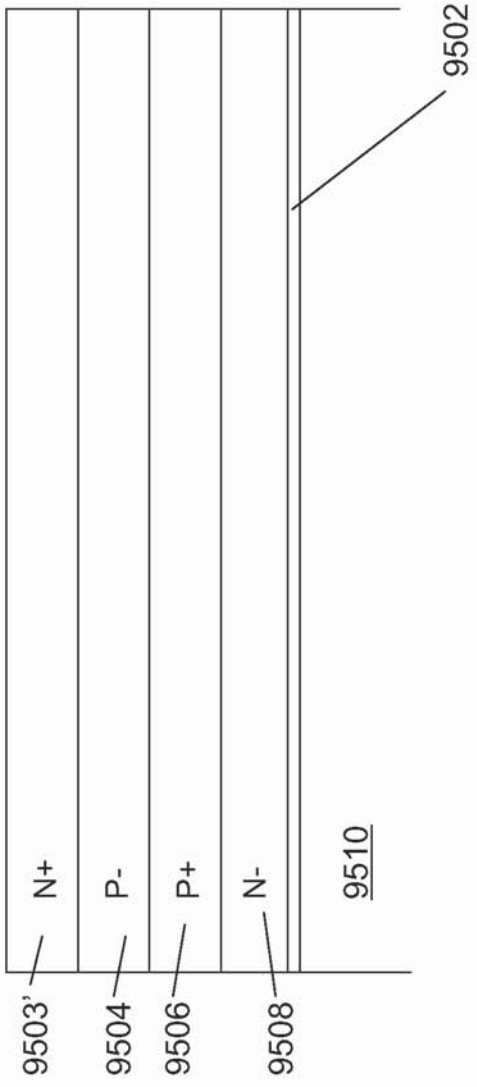


FIG. 95C

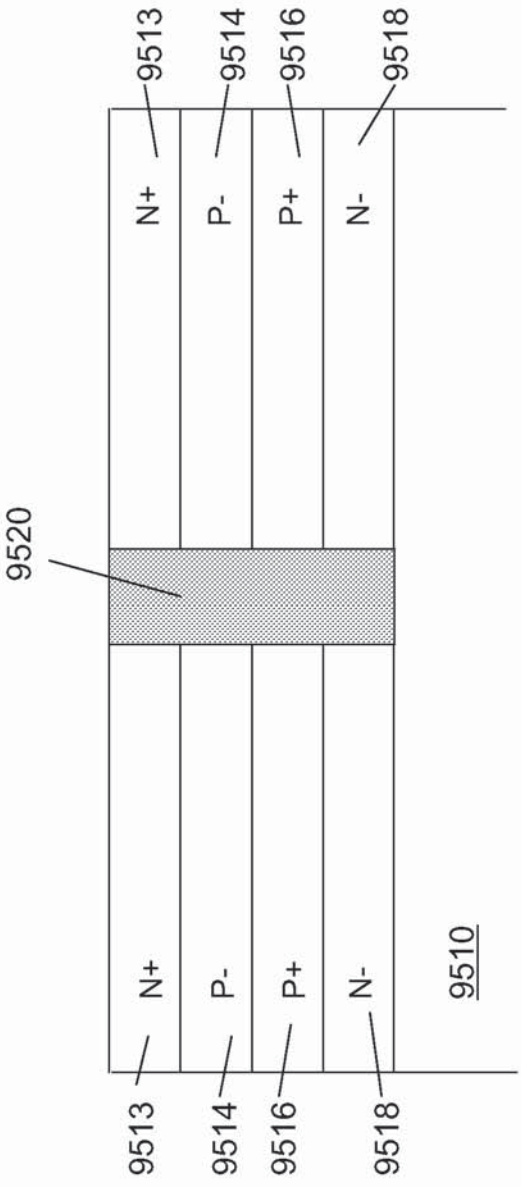

9513
9514
9516
9518
N+
P-
P+
N-
9520
9510
9513
9514
9516
9518
N+
P-
P+
N-
p-RCAT
n-RCAT

FIG. 95D

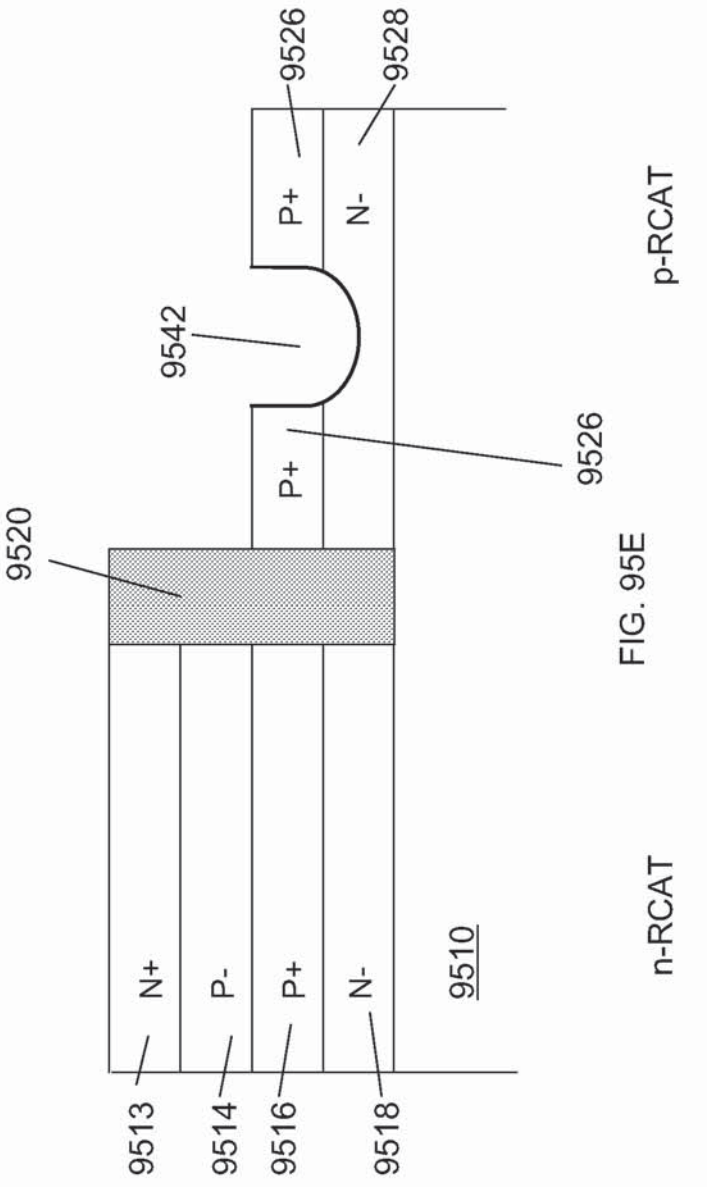

9526
9528
P+
N-
p-RCAT
9542
9526
P+
9520
N+
P-
P+
N-
9510
n-RCAT
9513
9514
9516
9518

FIG. 95E

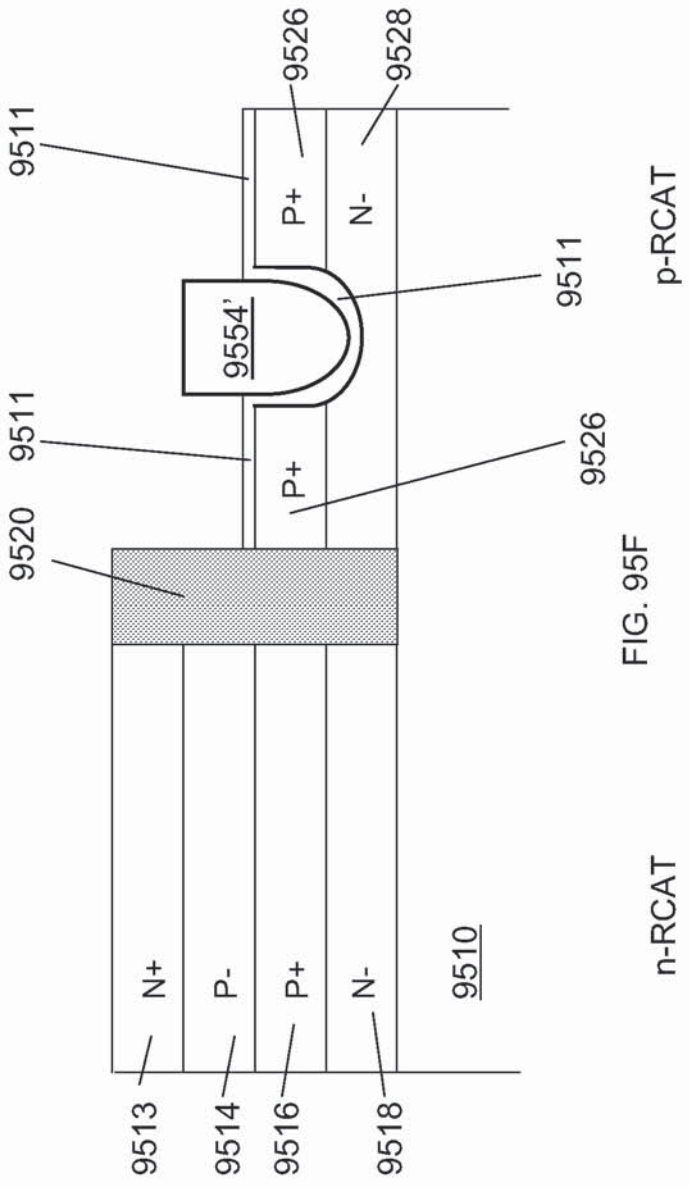

9526
9528
9511
P+
N-
9511
9554'
9511
P+
9526
9520
N+
P-
P+
N-
9510
9513
9514
9516
9518
p-RCAT
n-RCAT

FIG. 95F

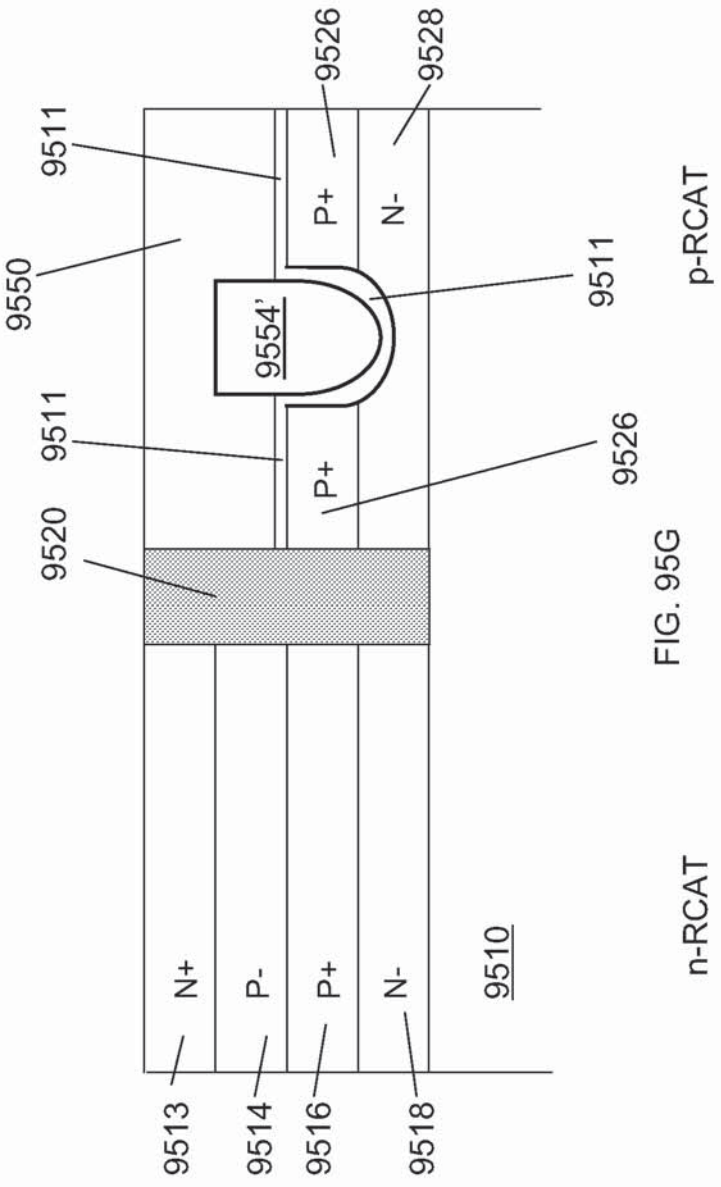

9526
9528
9511
P+
N-
9550
9554'
9511
9511
P+
9526
9520
N+
P-
P+
N-
9510
9513
9514
9516
9518
p-RCAT
n-RCAT

FIG. 95G

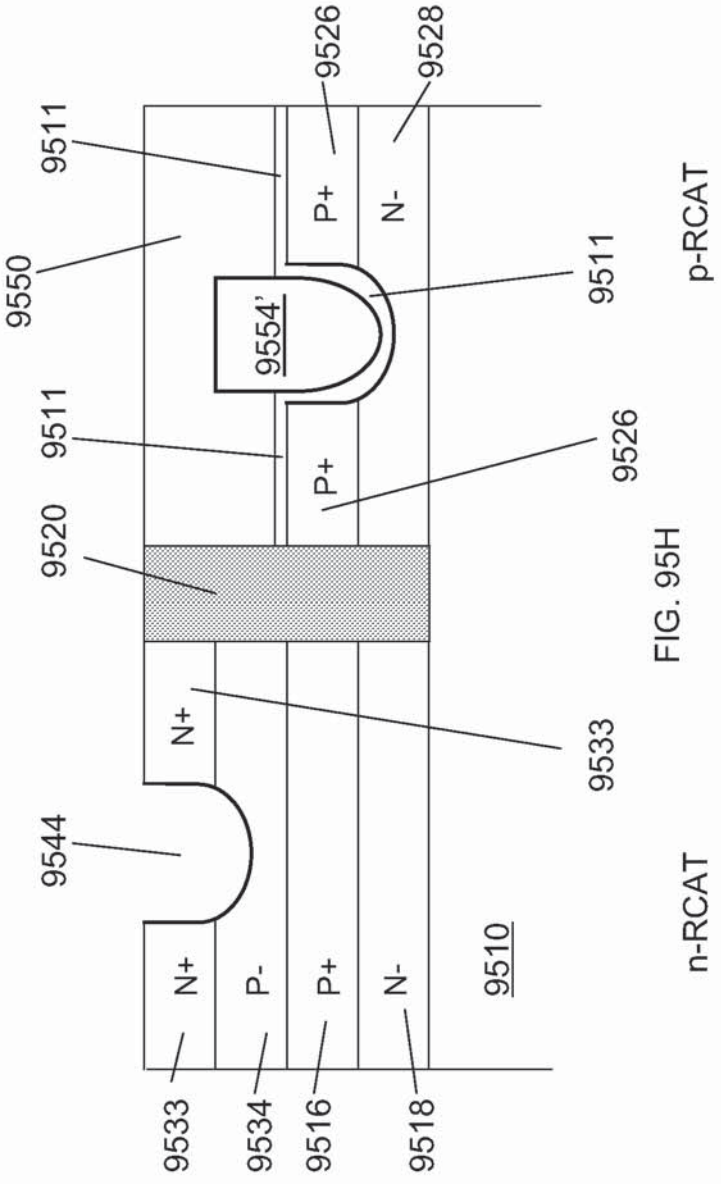

9526
9528
9511
P+
N-
9550
9554'
9511
p-RCAT
9511
9526
P+
9520
N+
9533
9544
9510
N+
P-
P+
N-
n-RCAT
9533
9534
9516
9518

FIG. 95H

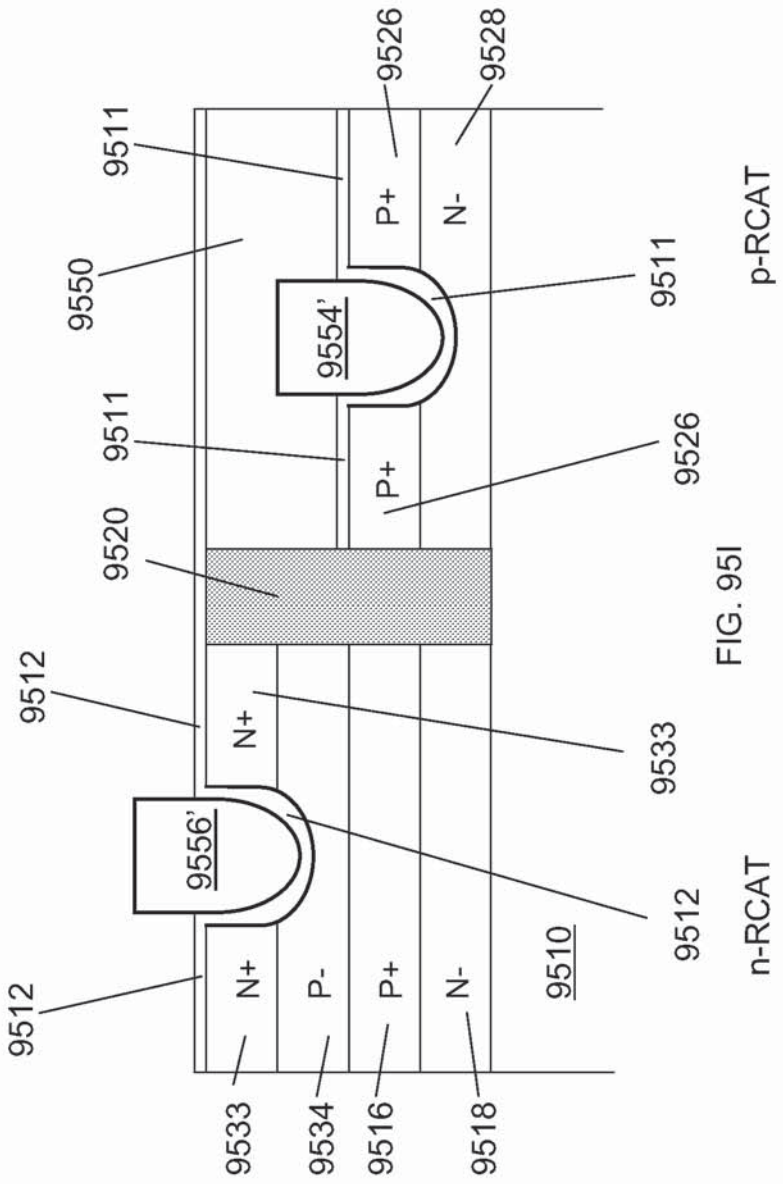

9526
9528
9511
P+
N-
9550
9554'
9511
p-RCAT
9511
9526
P+
9520
9512
N+
9533
9556'
9512
n-RCAT
9512
N+
P-
P+
N-
9510
9533
9534
9516
9518

FIG. 95I

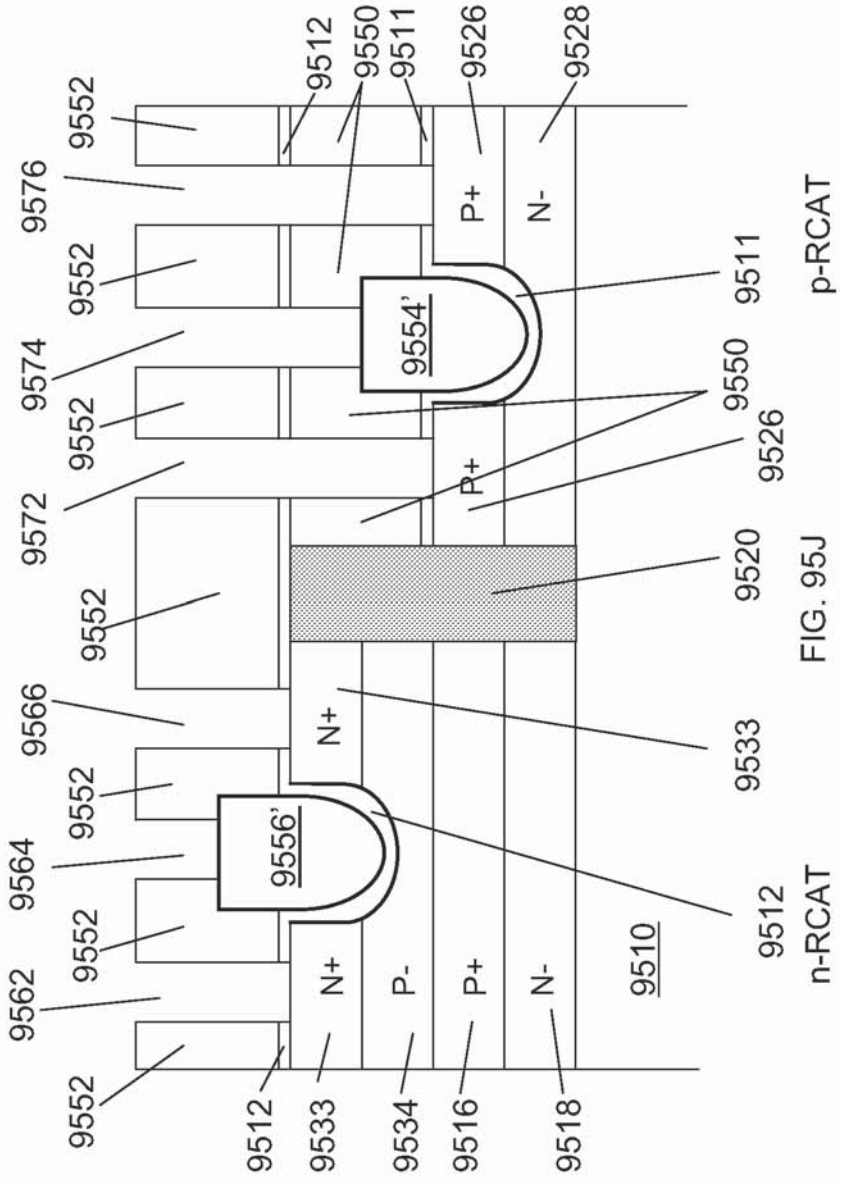

9552
9576
9552
9574
9552
9572
9552
9566
9552
9564
9552
9562
9552
9512
9533
9534
9516
9518
9512
9550
9511
9526
9528
P+
N-
9554'
9511
9550
9526
P+
9520
9533
N+
9556'
9512
n-RCAT
9510
N+
P-
P+
N-
p-RCAT

FIG. 95J

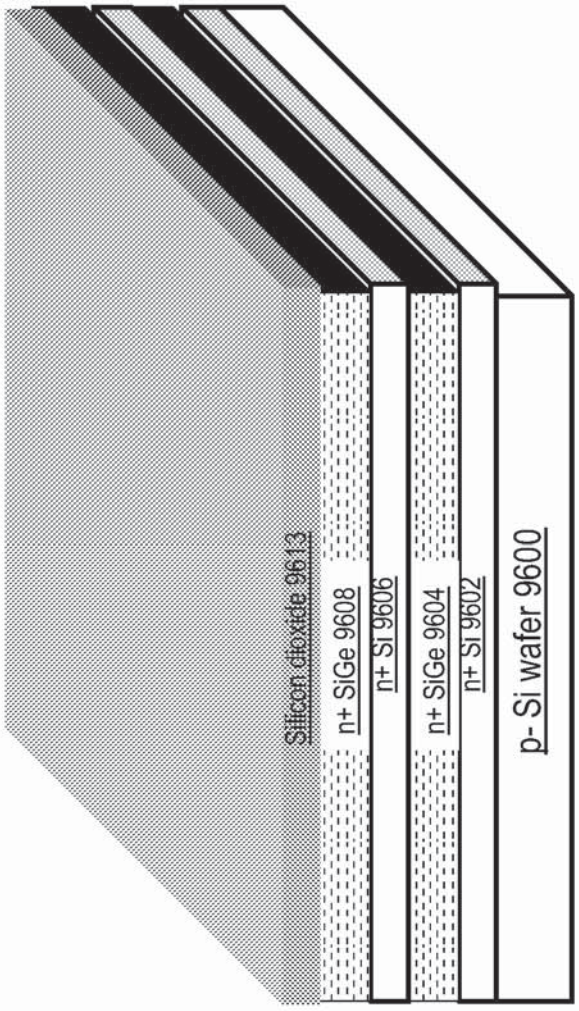

Silicon dioxide 9613
n+ SiGe 9608
n+ Si 9606
n+ SiGe 9604
n+ Si 9602
p- Si wafer 9600

FIG. 96A

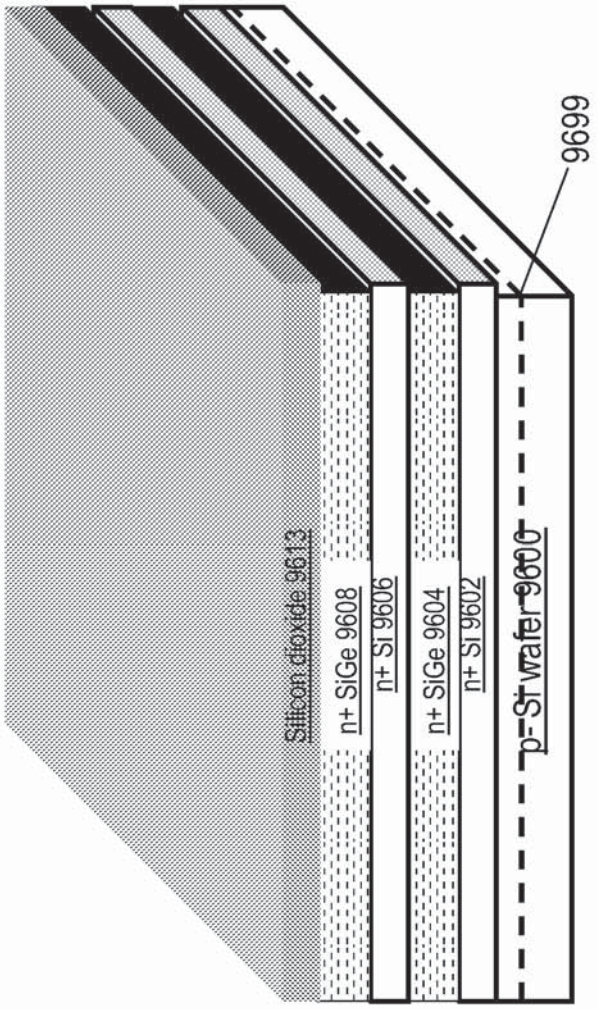

9699
Silicon dioxide 9613
n+ SiGe 9608
n+ Si 9606
n+ SiGe 9604
n+ Si 9602
p- Si wafer 9600

FIG. 96B

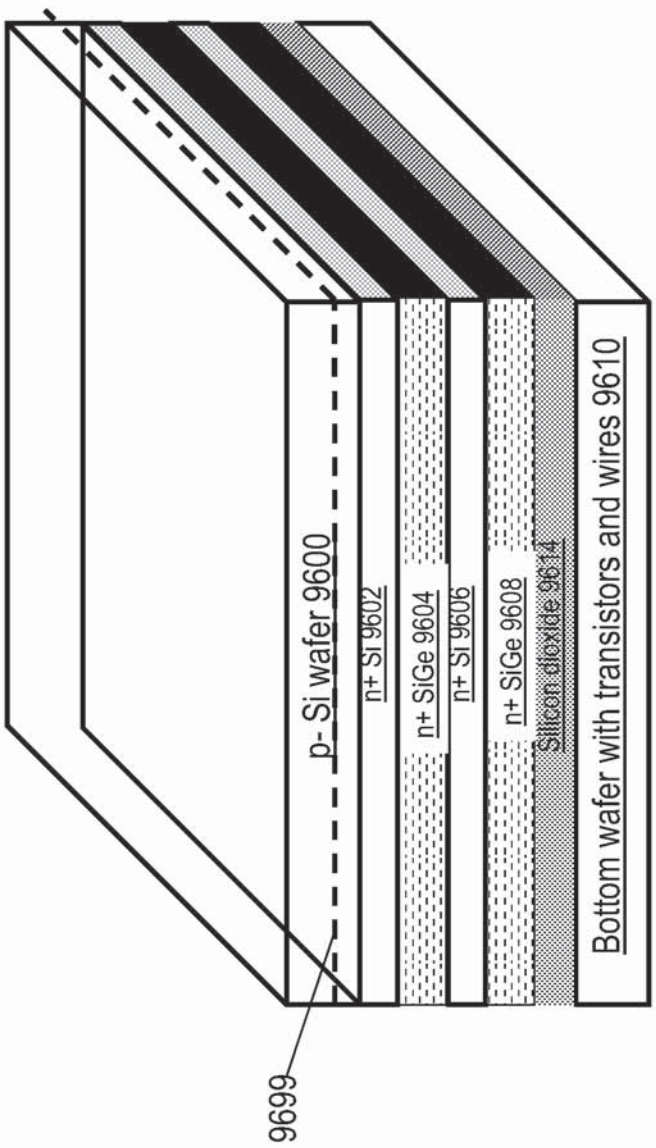

p- Si wafer 9600
n+ Si 9602
n+ SiGe 9604
n+ Si 9606
n+ SiGe 9608
Silicon dioxide 9614
Bottom wafer with transistors and wires 9610
9699

FIG. 96C

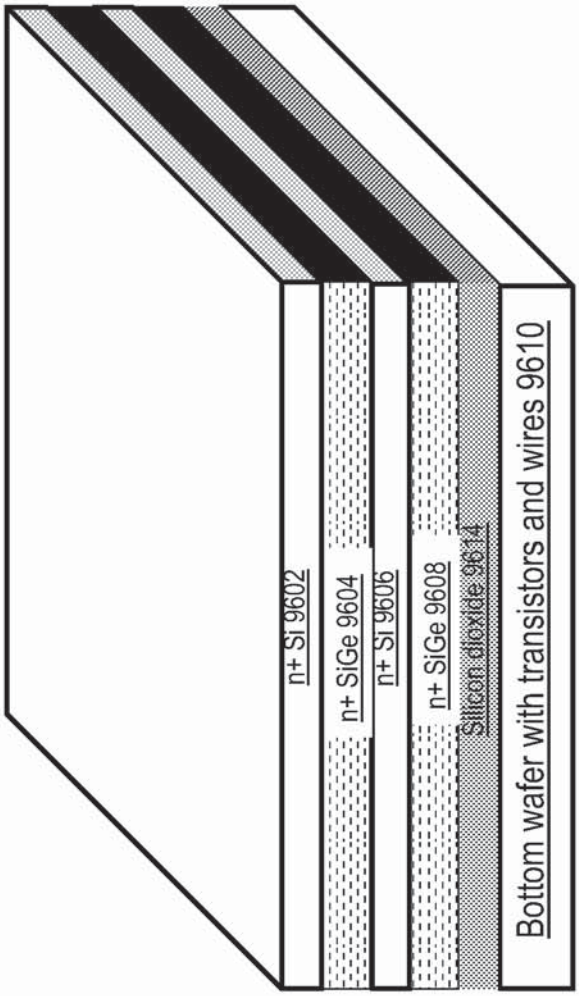

n+ Si 9602
n+ SiGe 9604
n+ Si 9606
n+ SiGe 9608
Silicon dioxide 9614
Bottom wafer with transistors and wires 9610

FIG. 96D

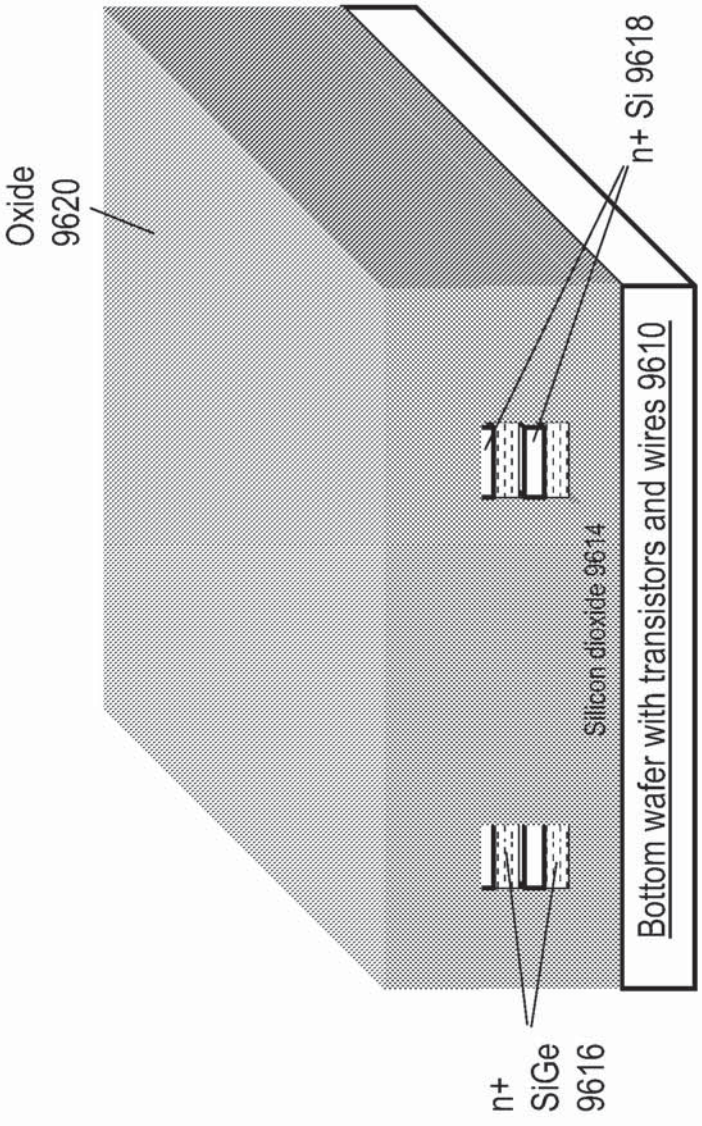

Oxide
9620
n+ Si 9618
Silicon dioxide 9614
Bottom wafer with transistors and wires 9610
n+
SiGe
9616

FIG. 96E

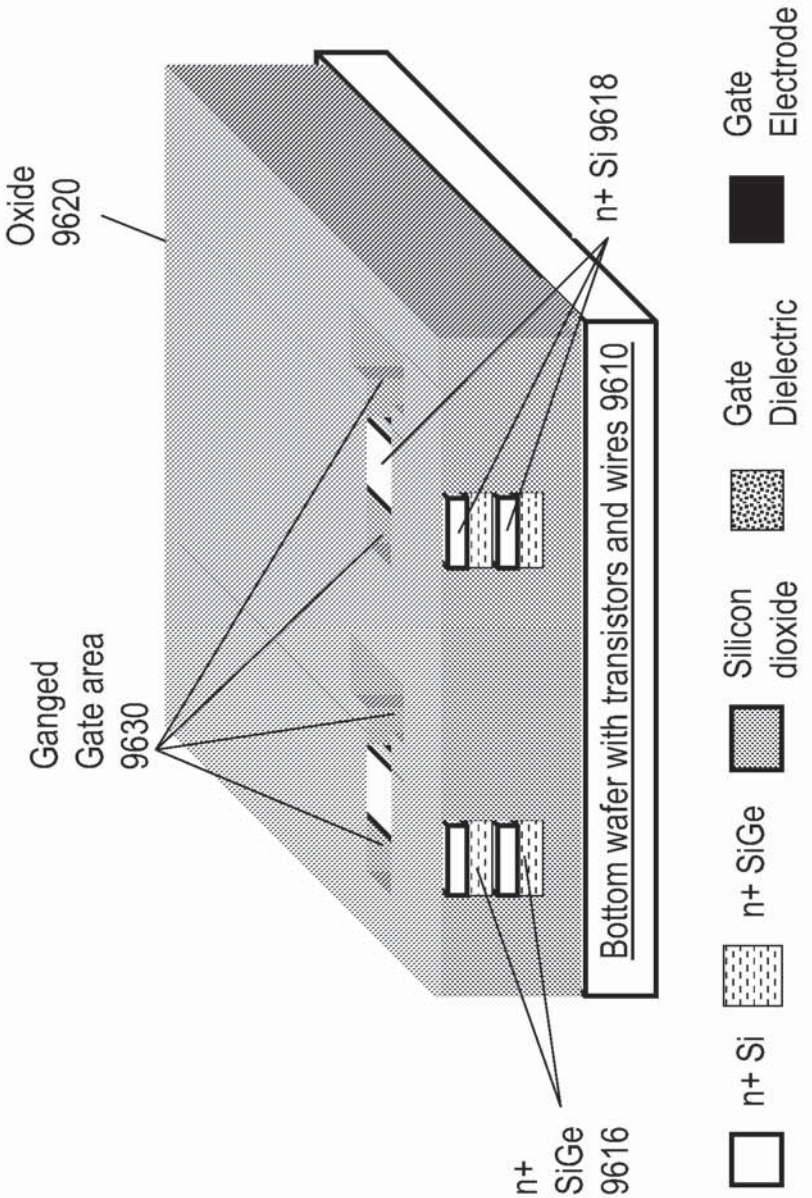

Oxide
9620
Ganged
Gate area
9630
n+ Si 9618
Bottom wafer with transistors and wires 9610
n+
SiGe
9616
n+ Si
n+ SiGe
Silicon
dioxide
Gate
Dielectric
Gate
Electrode

FIG. 96F

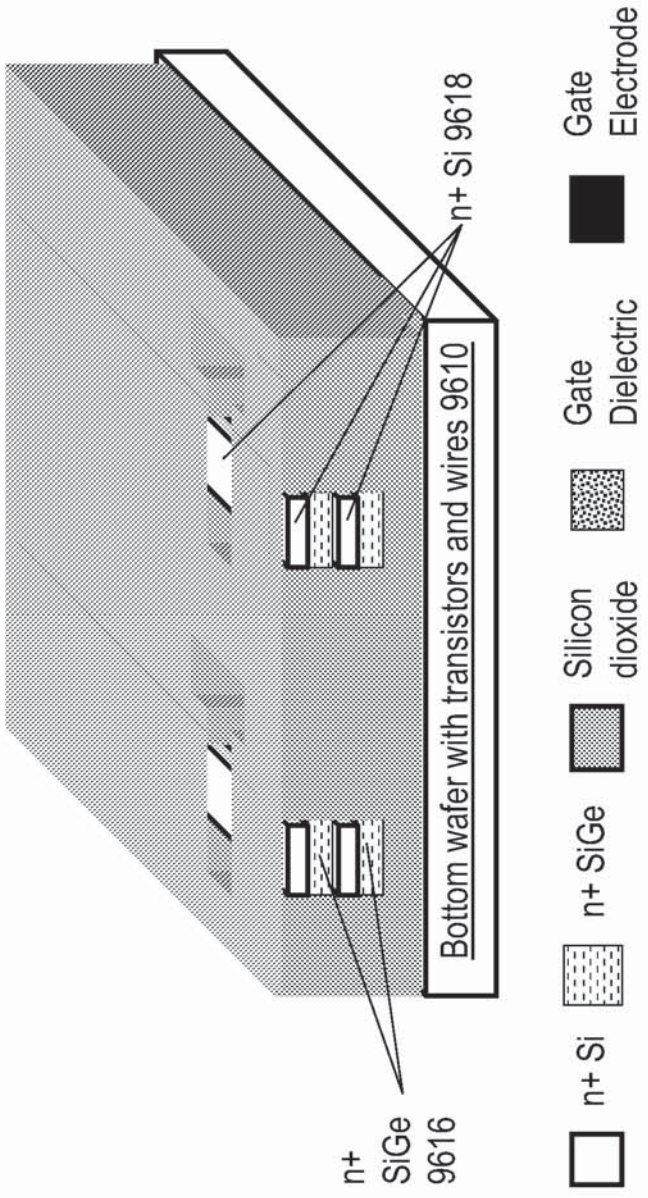

n+ Si 9618
Bottom wafer with transistors and wires 9610
n+ SiGe 9616
n+ Si
n+ SiGe
Silicon dioxide
Gate Dielectric
Gate Electrode

FIG. 96G

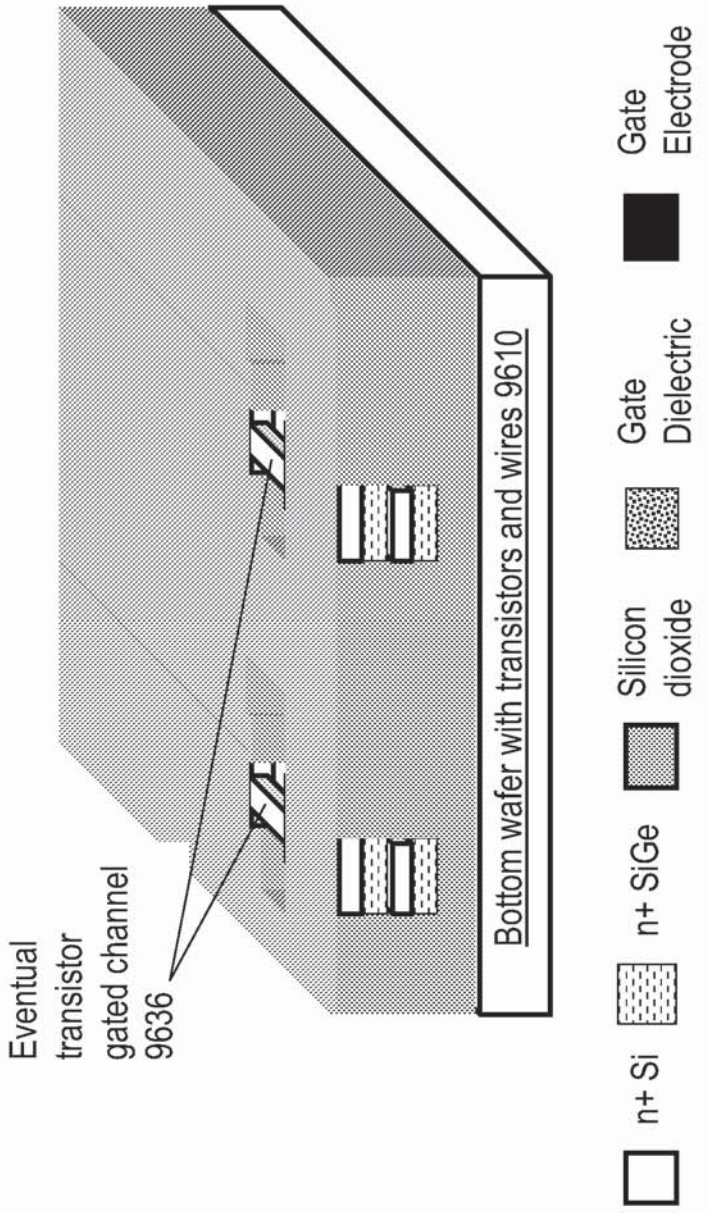

Eventual
transistor
gated channel
9636
Bottom wafer with transistors and wires 9610
n+ Si
n+ SiGe
Silicon
dioxide
Gate
Dielectric
Gate
Electrode

FIG. 96H

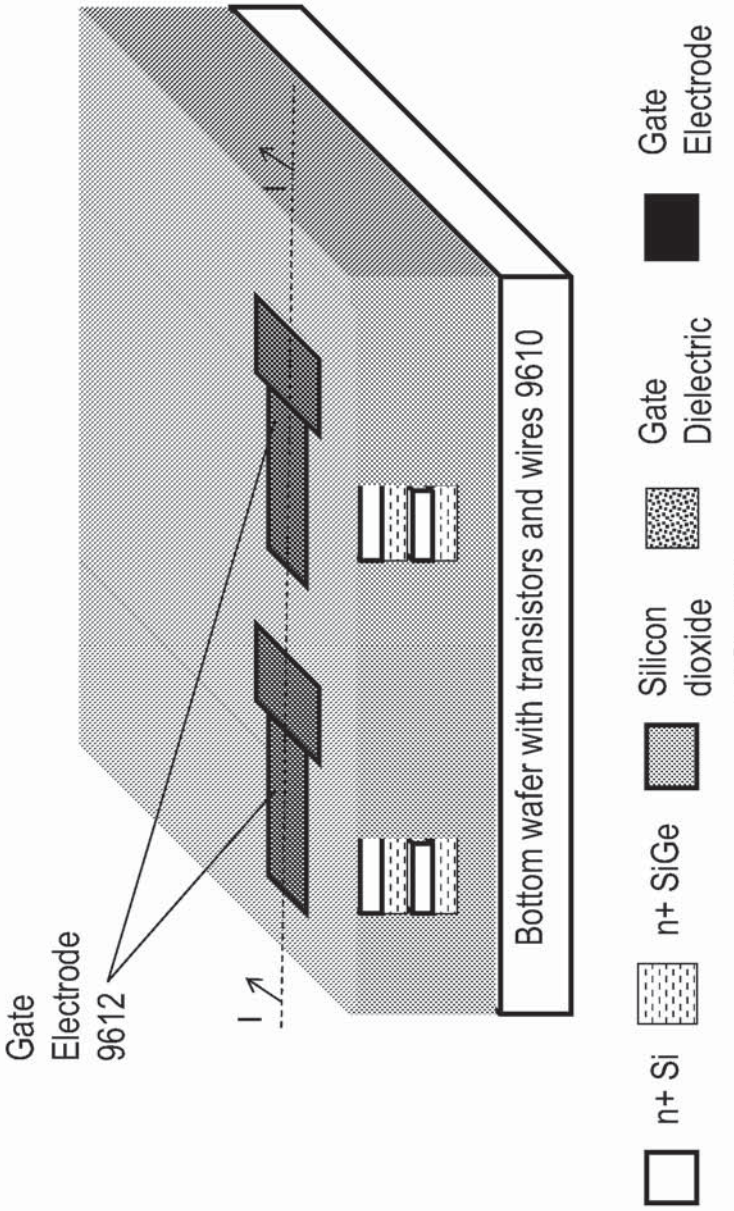

Gate
Electrode
9612
I
I
Bottom wafer with transistors and wires 9610
n+ Si
n+ SiGe
Silicon
dioxide
Gate
Dielectric
Gate
Electrode

FIG. 96I

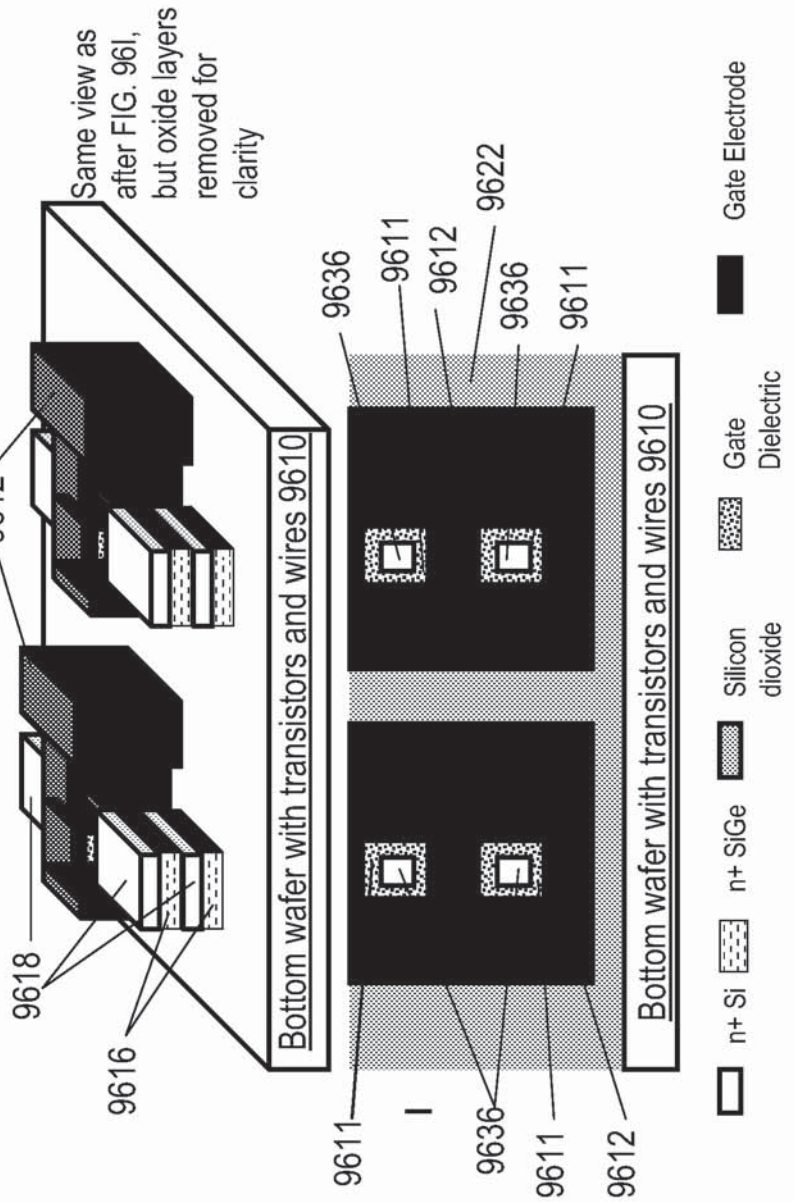
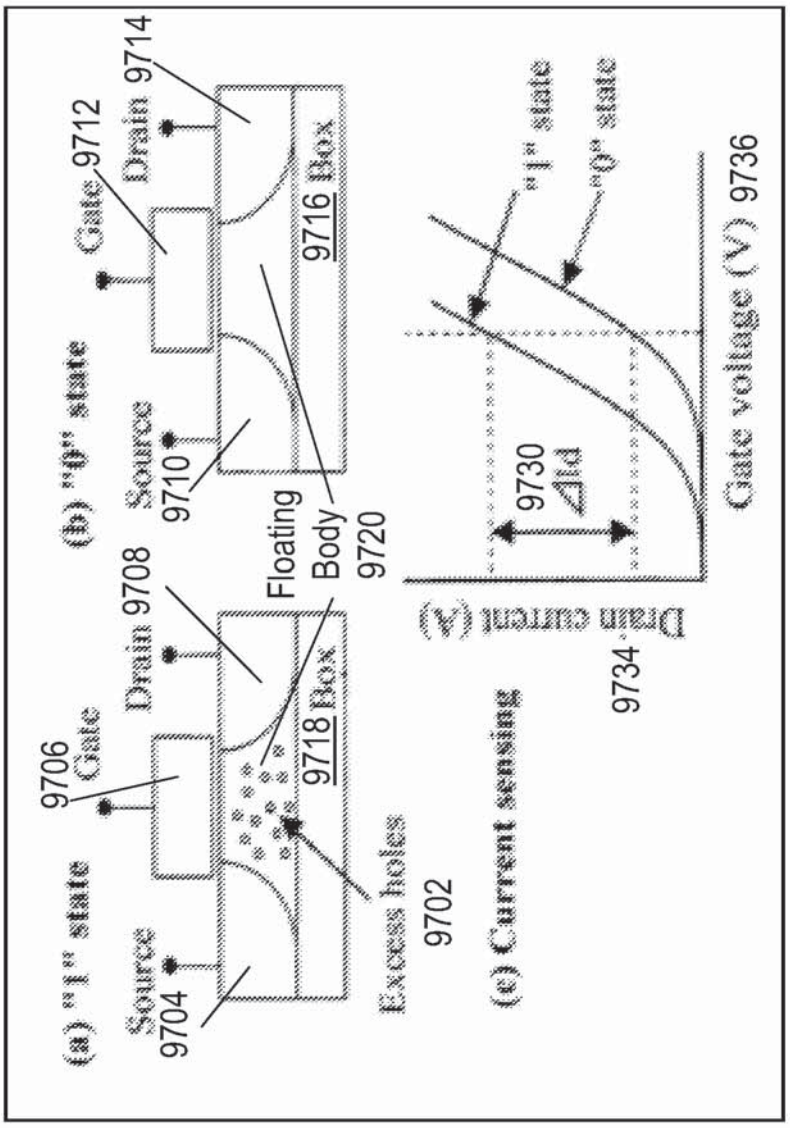

Same view as after FIG. 96l, but oxide layers removed for clarity
9612
9618
9616
Bottom wafer with transistors and wires 9610
9636
9611
9612
9622
9636
9611
I
9611
9636
9611
9612
Bottom wafer with transistors and wires 9610
n+ Si
n+ SiGe
Silicon dioxide
Gate Dielectric
Gate Electrode

FIG. 96J

FIG. 97 Prior Art



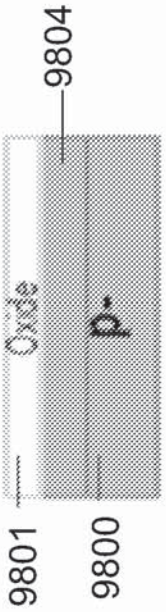


FIG. 98A

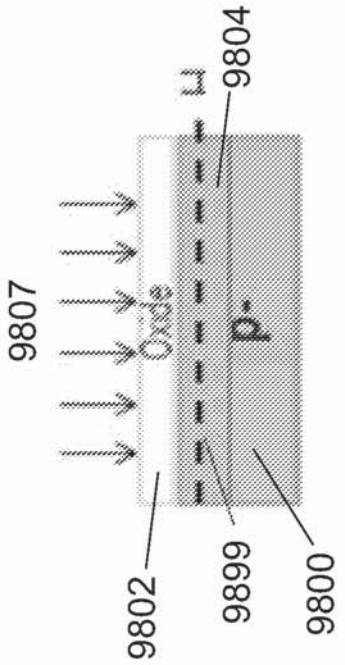


FIG. 98B

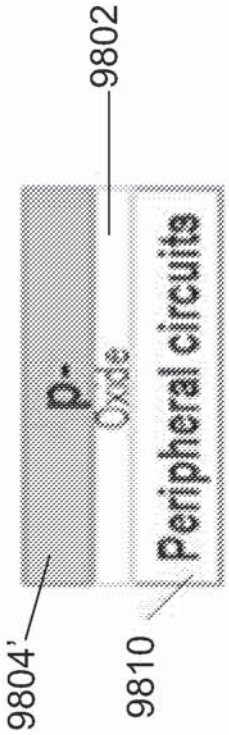


FIG. 98C

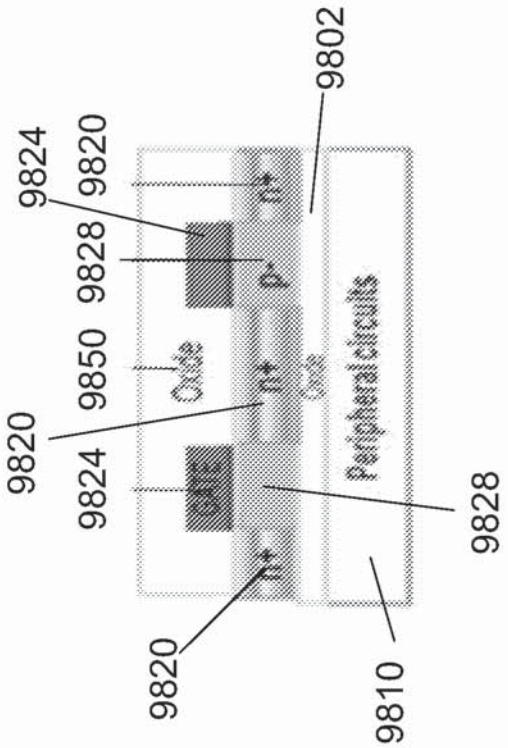

9802
9824
9820
9828
9850
9820
9824
9820
9828
9810
n+
p-
Oxide
n+
Oxide
GATE
n+
Peripheralcircuits

FIG. 98D

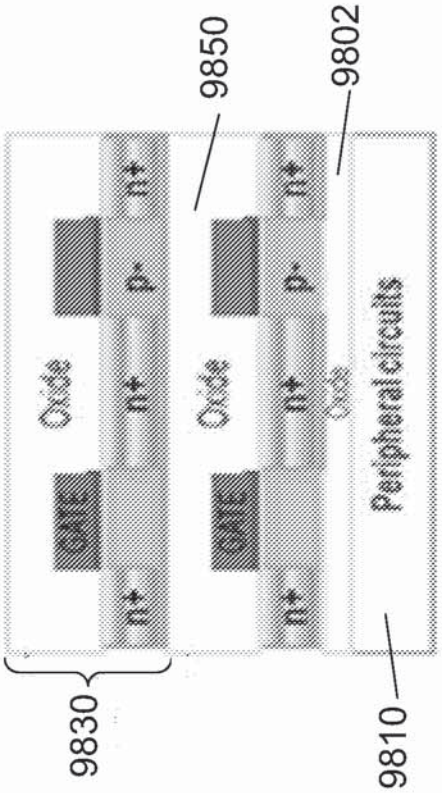

9850
9802
n+
p-
n+
Oxide
GATE
n+
n+
Oxide
GATE
n+
Sub
Peripheral circuits
9830
9810

FIG. 98E

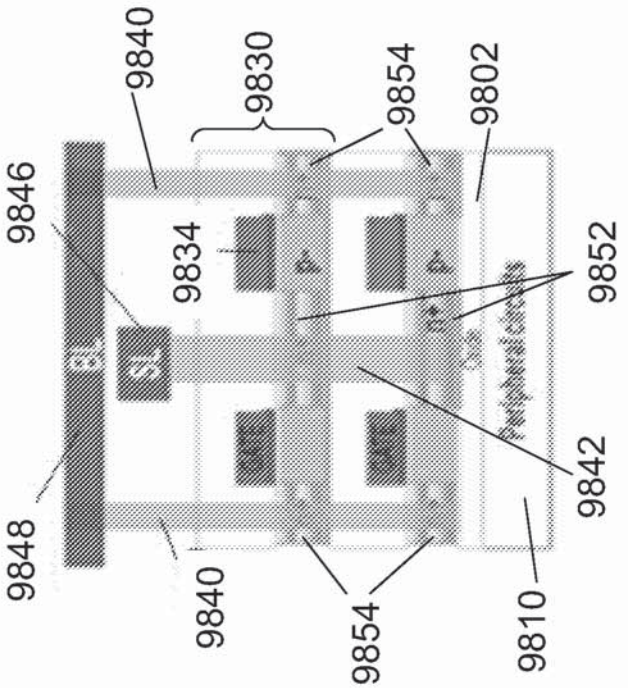


FIG. 98F

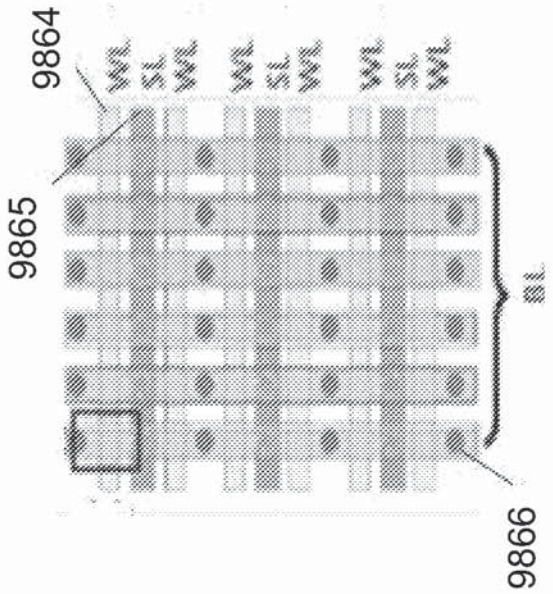


FIG. 98G

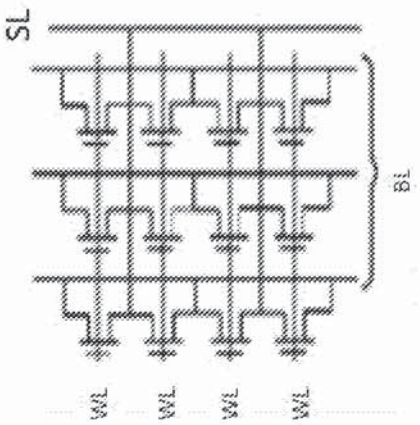


FIG. 98H

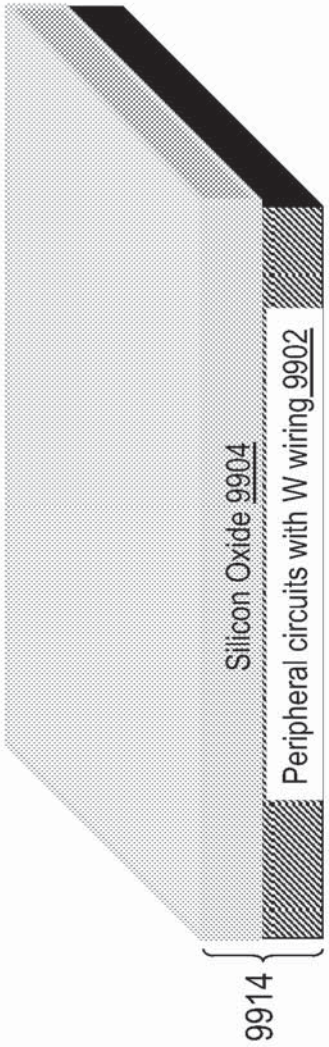

Silicon Oxide 9904
Peripheral circuits with W wiring 9902
9914

FIG. 99A

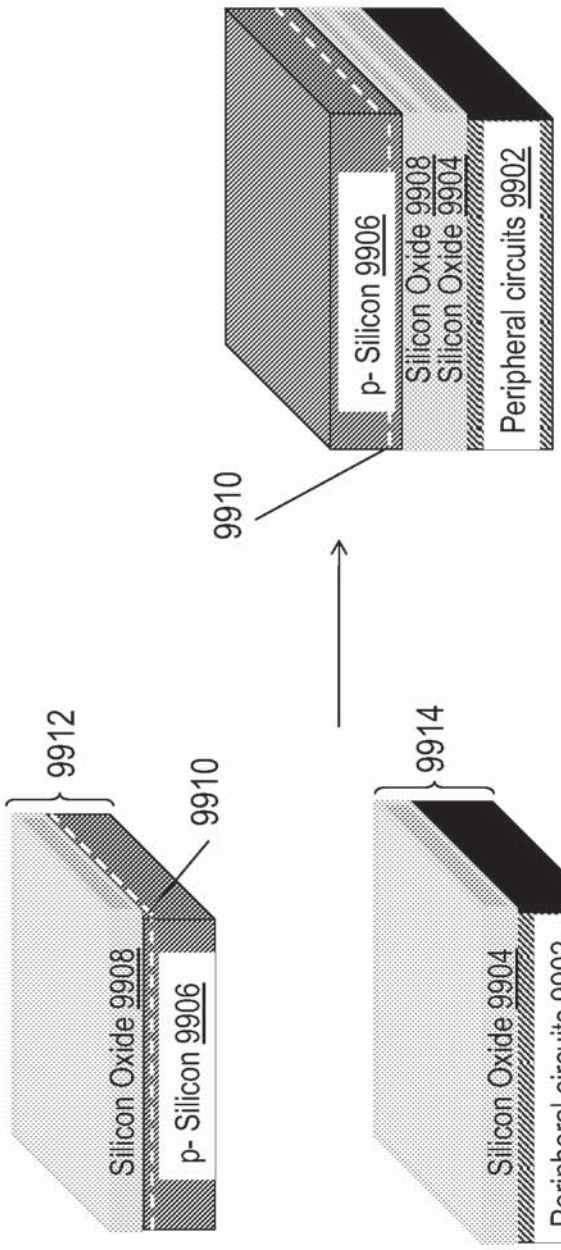

9912
9910
Silicon Oxide 9908
p- Silicon 9906
9914
Silicon Oxide 9904
Peripheral circuits 9902
9910
p- Silicon 9906
Silicon Oxide 9908
Silicon Oxide 9904
Peripheral circuits 9902

FIG. 99B

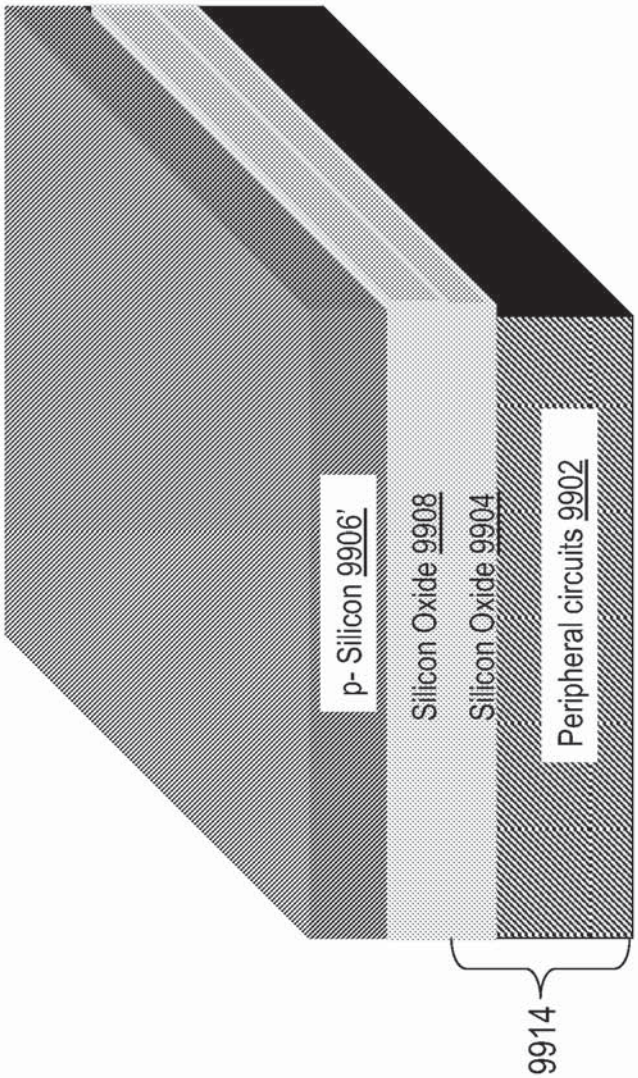

p- Silicon 9906'
Silicon Oxide 9908
Silicon Oxide 9904
Peripheral circuits 9902
9914

FIG. 99C

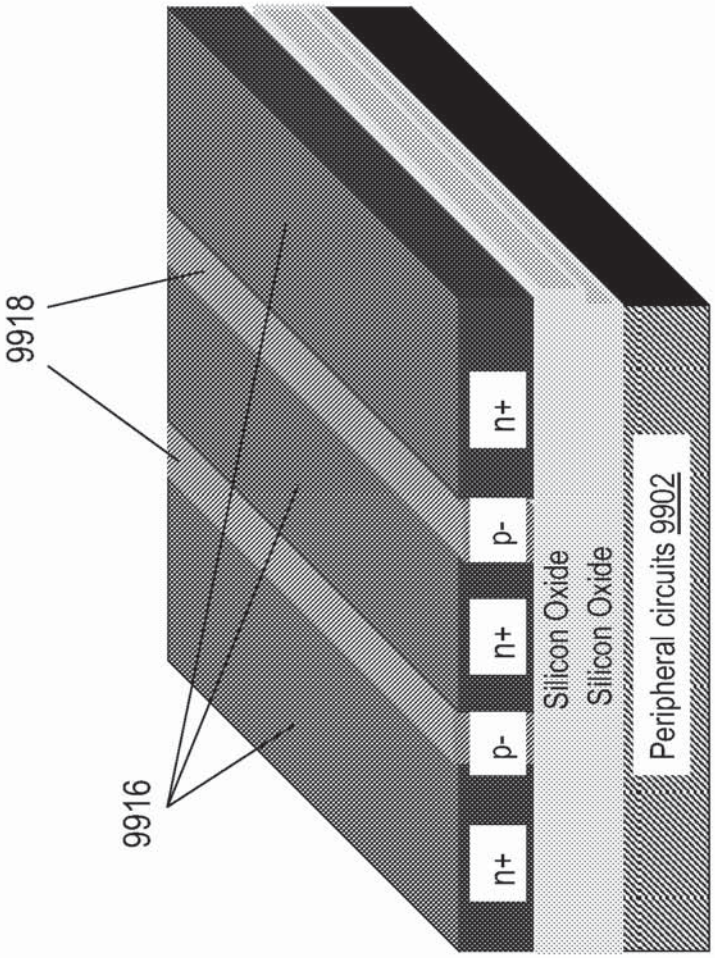

9918
9916
n+
p-
n+
p-
n+
Silicon Oxide
Silicon Oxide
Peripheral circuits 9902

FIG. 99D

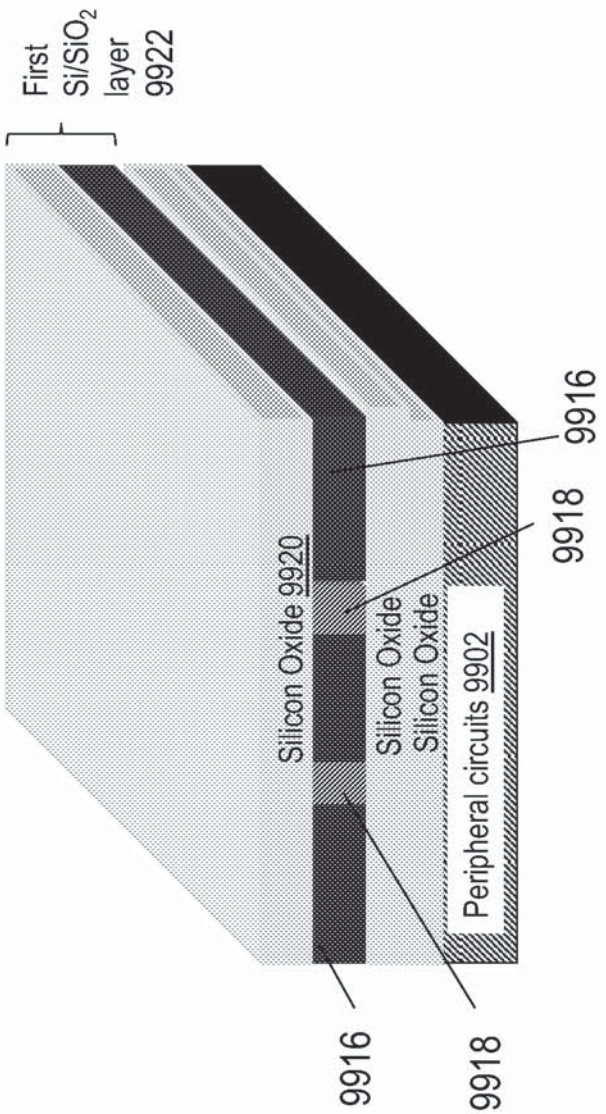

First
Si/SiO2
layer
9922
Silicon Oxide 9920
Silicon Oxide
Silicon Oxide
Peripheral circuits 9902
9916
9918
9916
9918

FIG. 99E

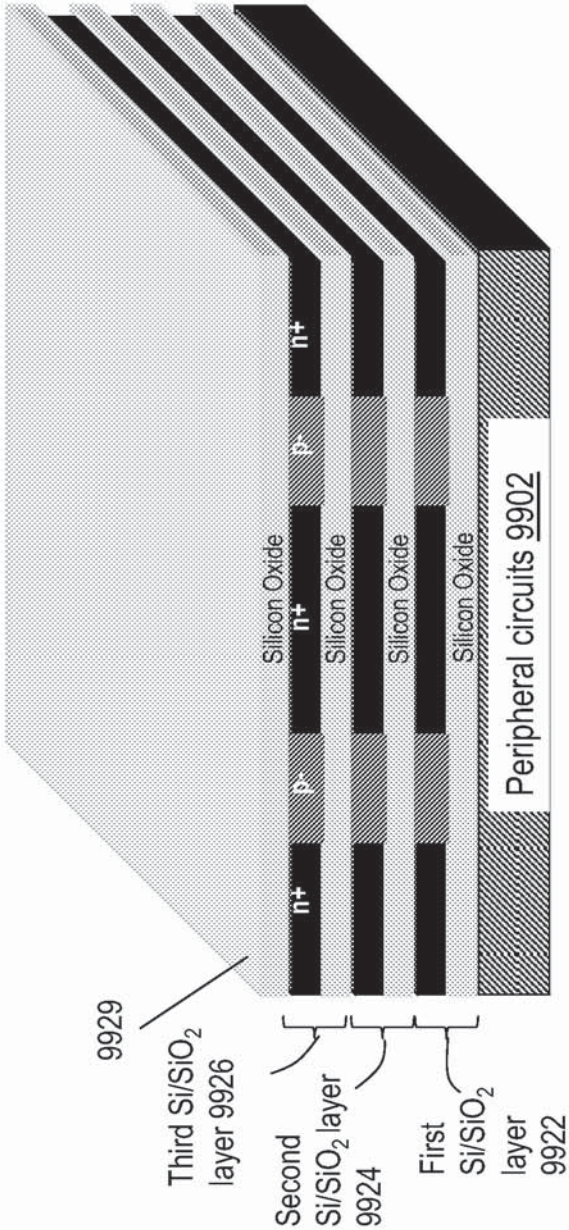

9929
Third Si/SiO2 layer 9926
Second Si/SiO2 layer 9924
First Si/SiO2 layer 9922
n+
p-
n+
p-
n+
Silicon Oxide
Silicon Oxide
Silicon Oxide
Silicon Oxide
Peripheral circuits 9902

FIG. 99F

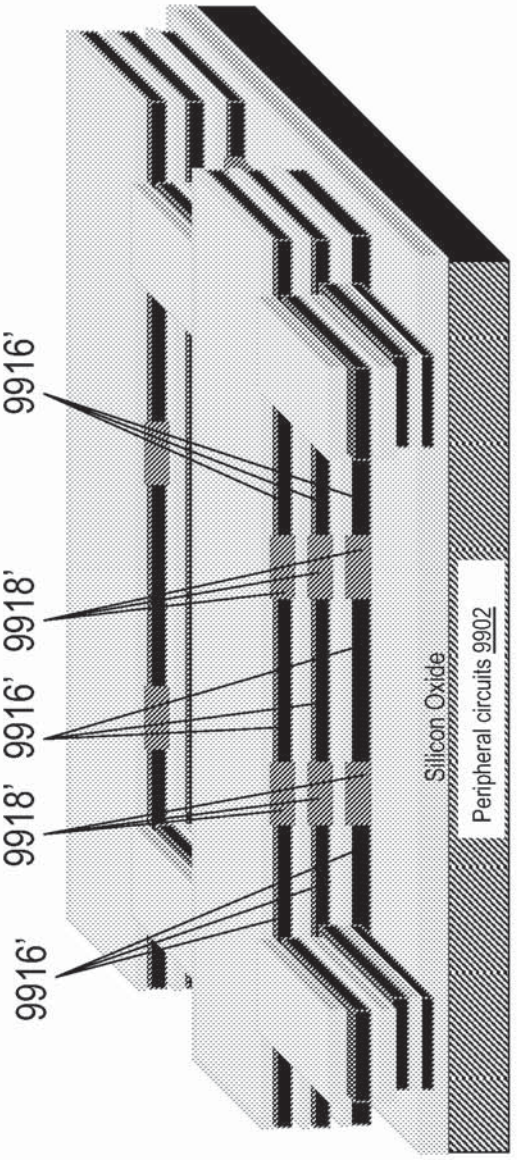

9916'
9918'
9916'
9918'
9916'
Silicon Oxide
Peripheral circuits 9902
Symbols
p- Silicon 9918'
Silicon oxide
n+ Silicon 9916'

FIG. 99G

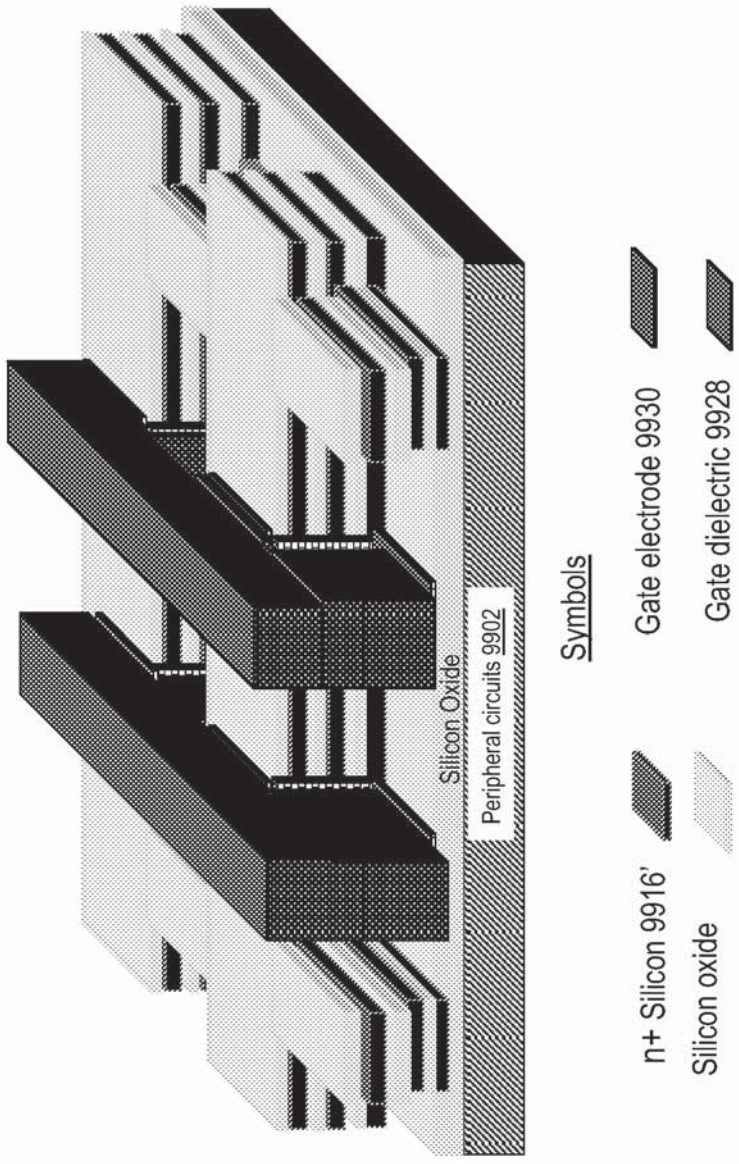

Silicon Oxide
Peripheral circuits 9902
Symbols
n+ Silicon 9916'
Silicon oxide
Gate electrode 9930
Gate dielectric 9928

FIG. 99H

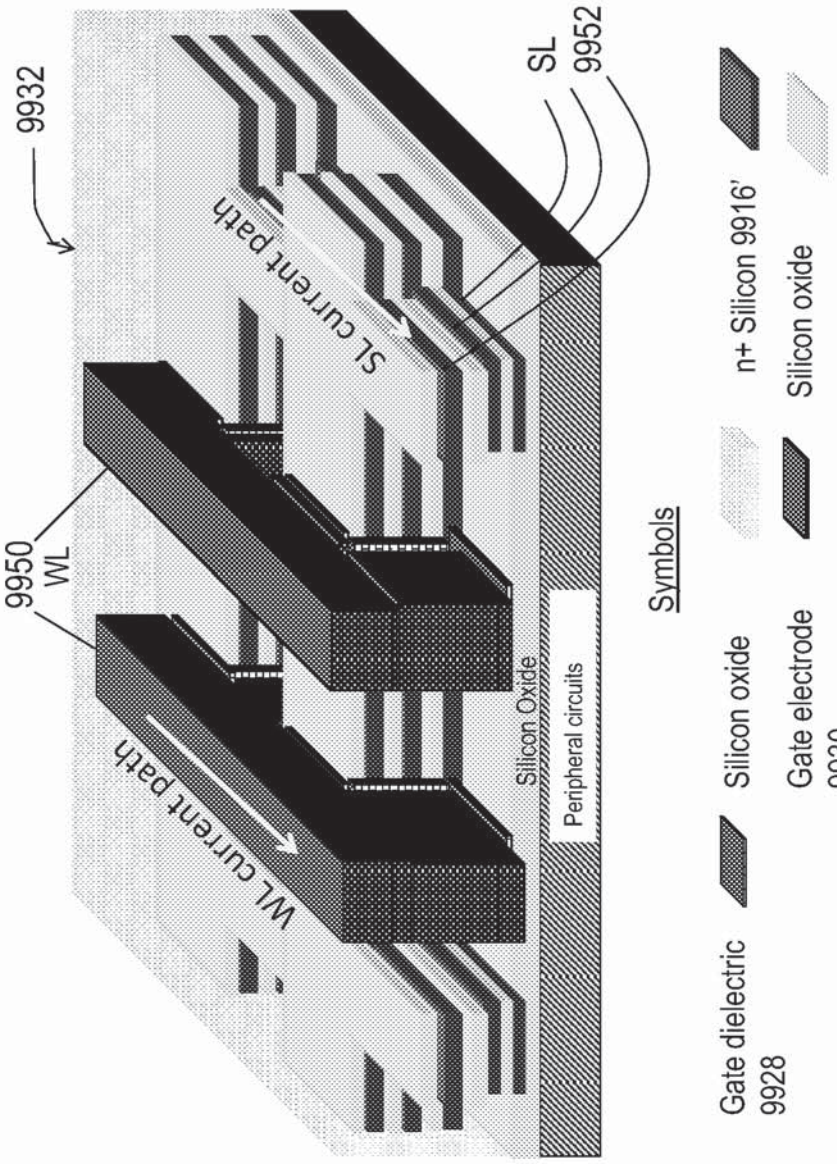

9932
SL
9952
SL current path
9950
WL
WL current path
Silicon Oxide
Peripheral circuits
Symbols
Gate dielectric
9928
Silicon oxide
Gate electrode
9930
n+ Silicon 9916'
Silicon oxide

FIG. 99I

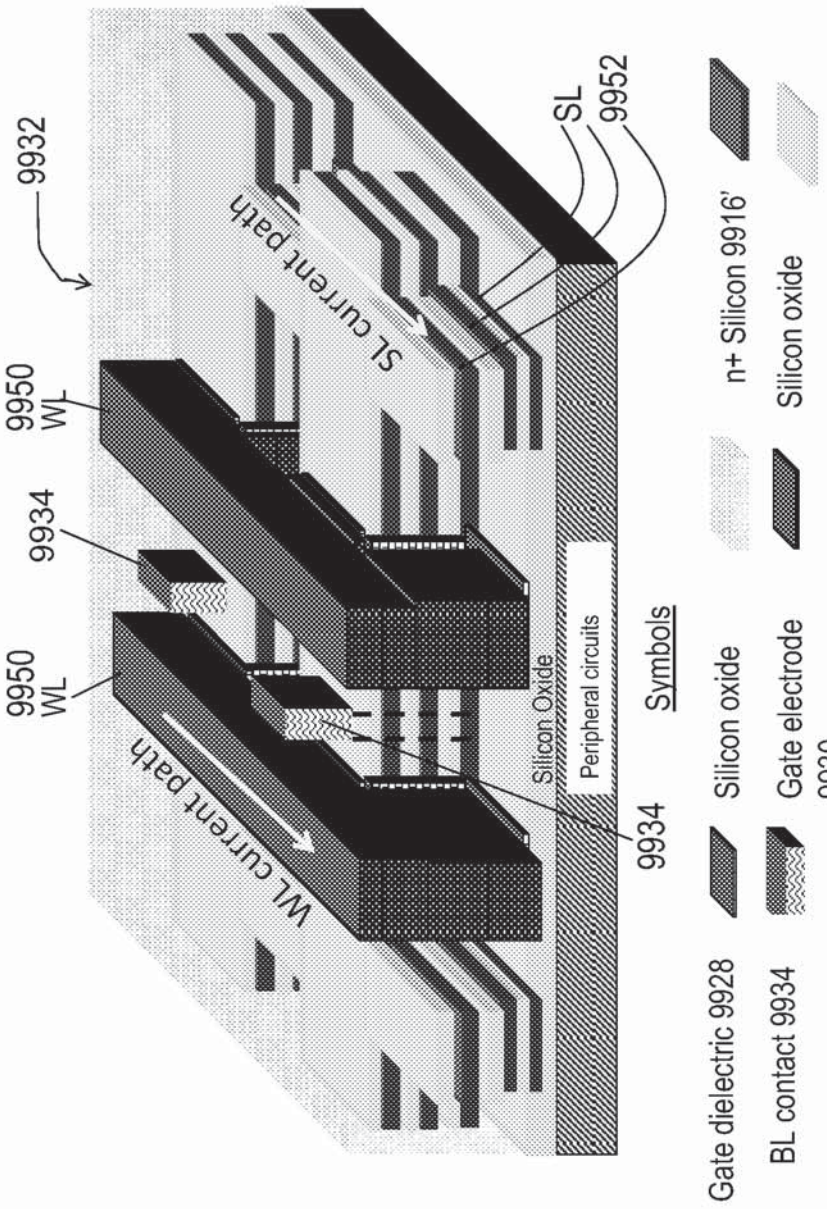

9932
9950
WL
9934
9950
WL
WL current path
SL current path
SL
9952
Silicon Oxide
Peripheral circuits
9934
Symbols
Silicon oxide
Gate electrode
9930
n+ Silicon 9916'
Silicon oxide
Gate dielectric 9928
BL contact 9934

FIG. 99J

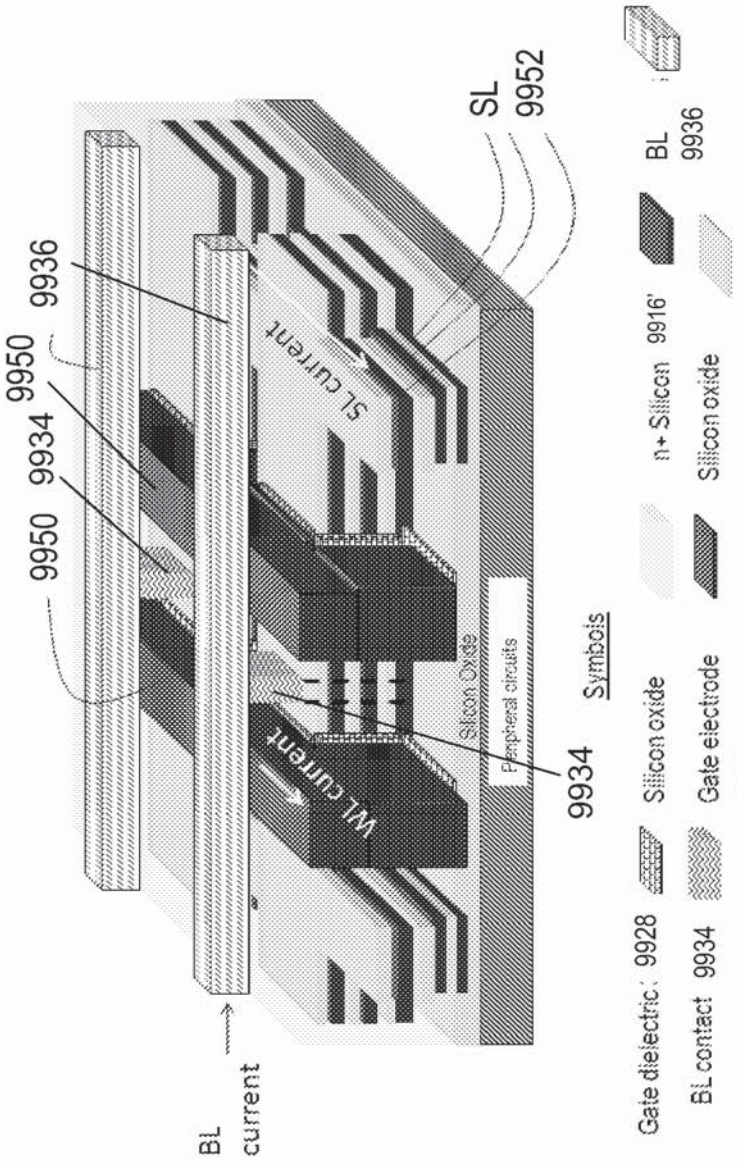

SL
9952
BL
9936
9936
9950
9934
9950
SL current
WL current
Silicon Oxide
Peripheral circuits
9934
Symbols
n+ Silicon 9916'
Silicon oxide
Gate electrode
9930
Silicon oxide
Gate dielectric 9928
BL contact 9934
BL
current

FIG. 99K

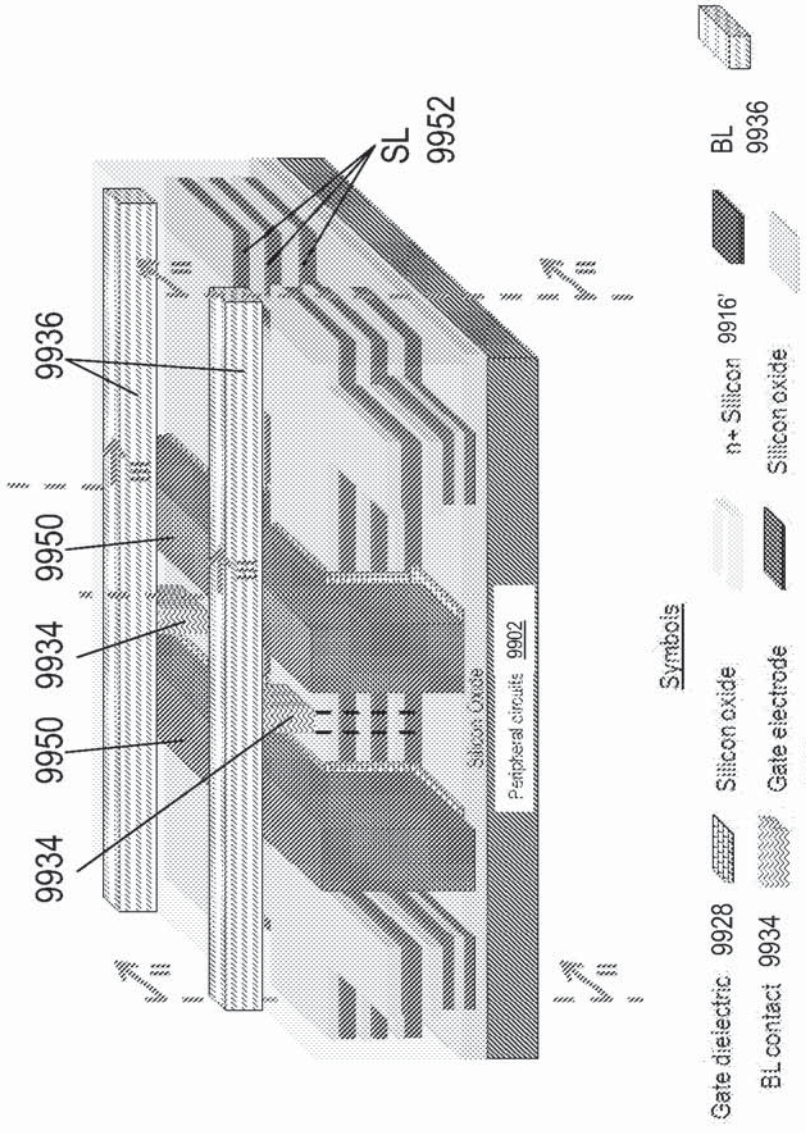

SL
9952
9936
9934
9950
9934
9950
9936
Peripheral circuits 9902
Silicon oxide
Symbols
Gate dielectric 9928
Bl contact 9934
Silicon oxide
Gate electrode
9930
n+ Silicon 9916'
Silicon oxide
BL
9936

FIG. 99L

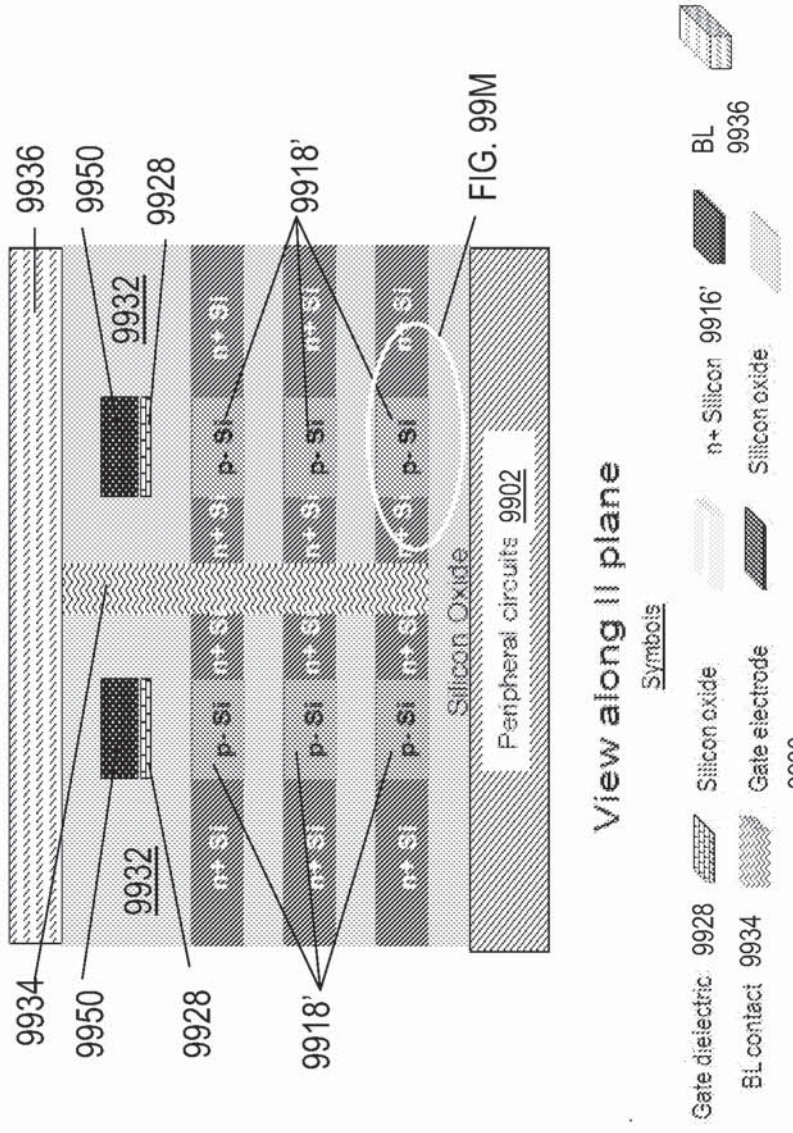

9936
9950
9928
9932
9918'
FIG. 99M
9934
9950
9928
9932
9918'
n+ Si
p- Si
Silicon Oxide
Peripheral circuits 9902
View along II plane
Symbols
Gate dielectric 9928
Silicon oxide
n+ Silicon 9916'
BL 9936
BL contact 9934
Gate electrode 9930
Silicon oxide

FIG. 99L1

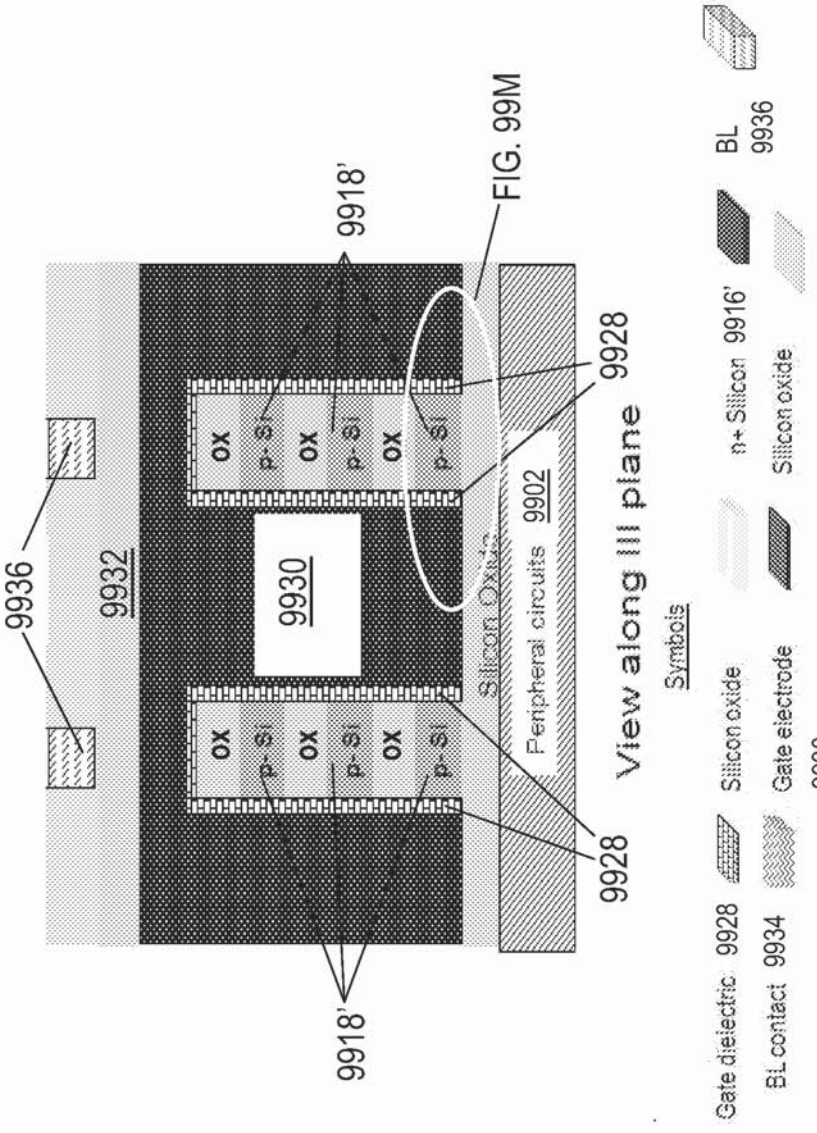

9936
9932
9930
9928
9928
9918'
9918'
FIG. 99M
View along III plane
Peripheral circuits 9902
Silicon Oxide
ox
p- Si
Symbols
Gate dielectric 9928
Bl contact 9934
Silicon oxide
Gate electrode
9930
n+ Silicon 9916'
Silicon oxide
BL
9936

FIG. 99L2

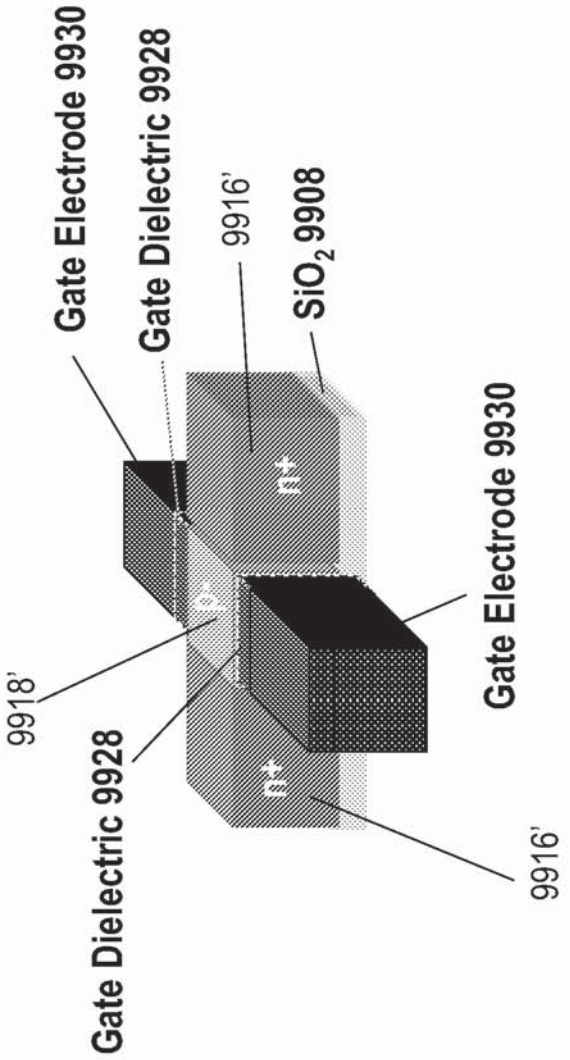

Gate Electrode 9930
Gate Dielectric 9928
9916'
SiO_2 9908
n+
9918'
Gate Dielectric 9928
Gate Electrode 9930
n+
9916'

FIG. 99M


Silicon Oxide 10004
Peripheral circuits with W wiring 10002
10014

FIG. 100A

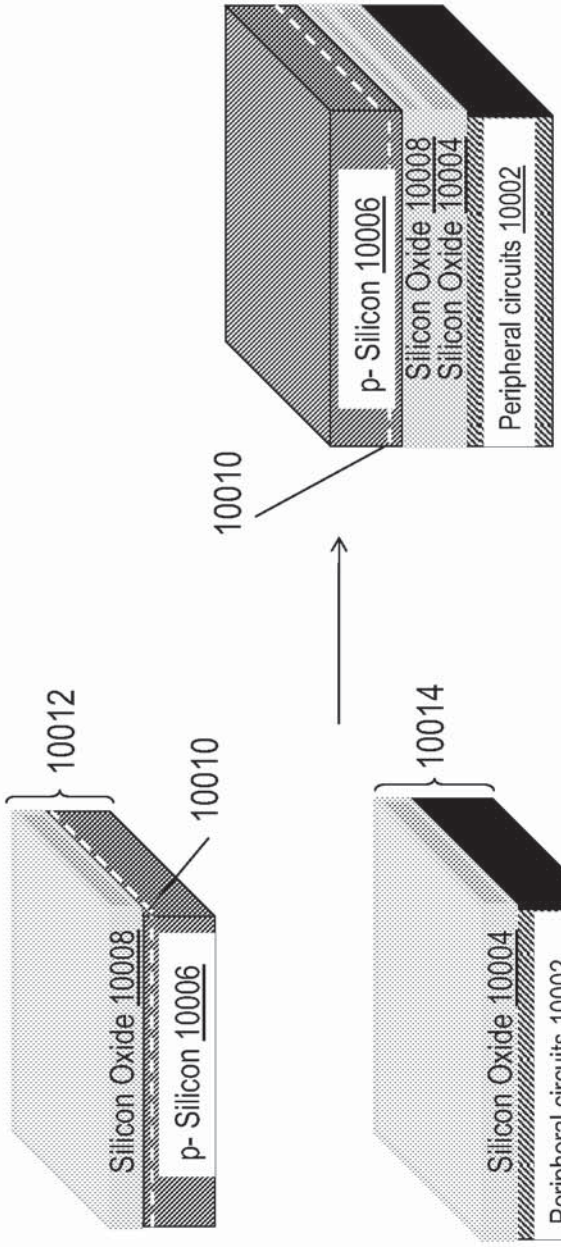

10012
10010
Silicon Oxide 10008
p- Silicon 10006
10010
p- Silicon 10006
Silicon Oxide 10008
Silicon Oxide 10004
Peripheral circuits 10002
10014
Silicon Oxide 10004
Peripheral circuits 10002

FIG. 100B

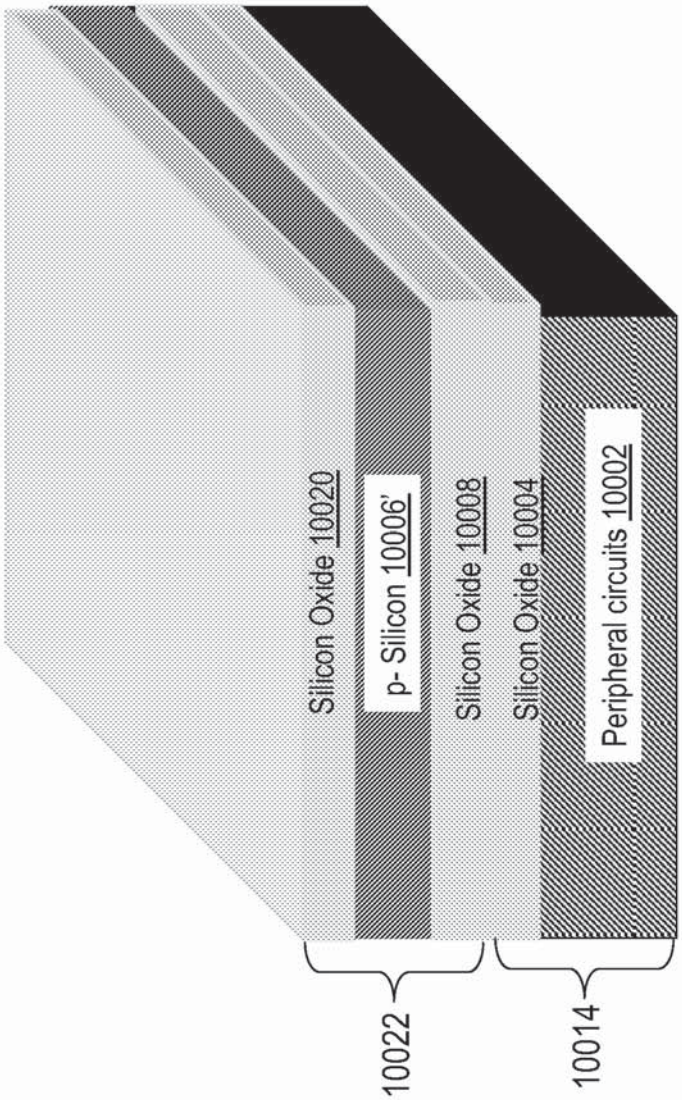

Silicon Oxide 10020
p- Silicon 10006'
Silicon Oxide 10008
Silicon Oxide 10004
Peripheral circuits 10002
10022
10014

FIG. 100C

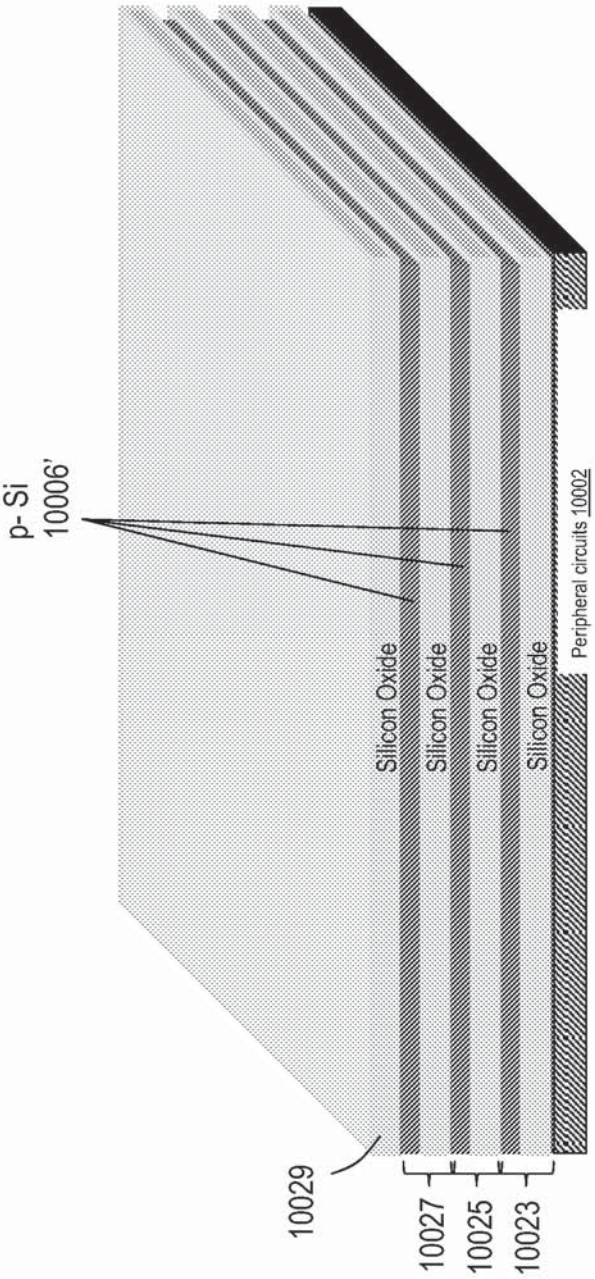

p- Si
10006'
Silicon Oxide
Silicon Oxide
Silicon Oxide
Silicon Oxide
Peripheral circuits 10002
10029
10027
10025
10023

FIG. 100D

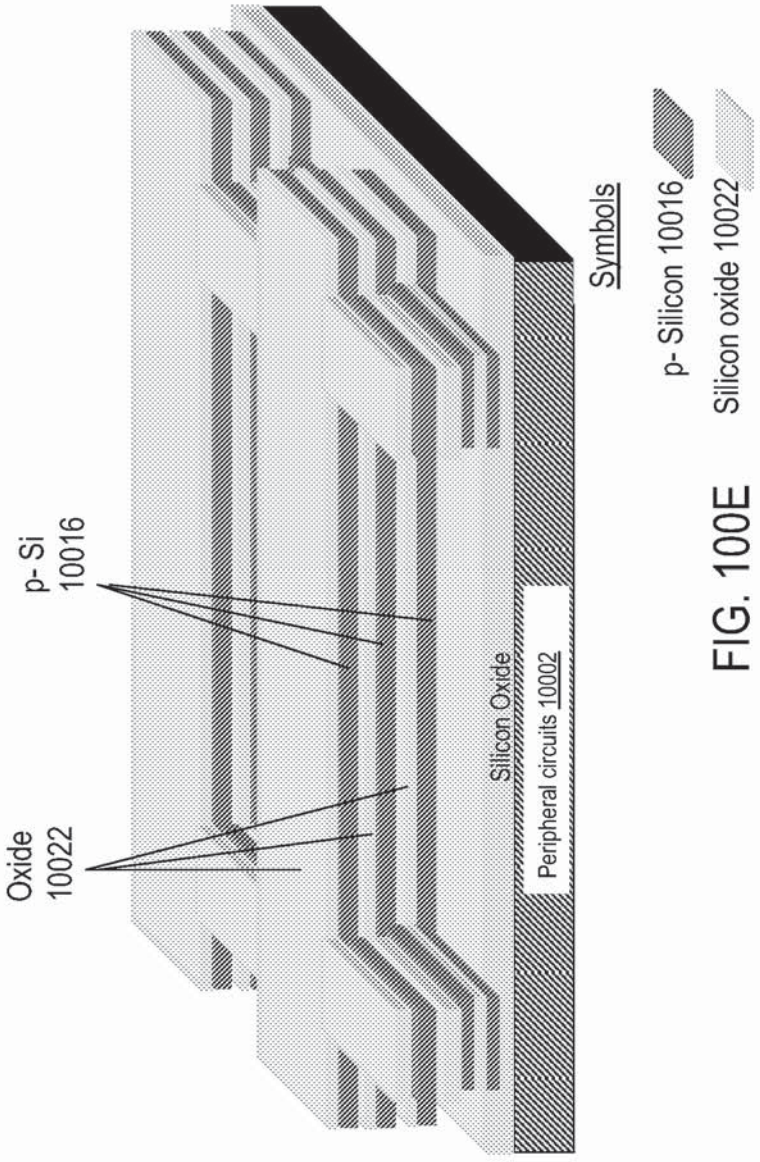

p- Si
10016
Oxide
10022
Silicon Oxide
Peripheral circuits 1002
Symbols
p- Silicon 10016
Silicon oxide 10022

FIG. 100E

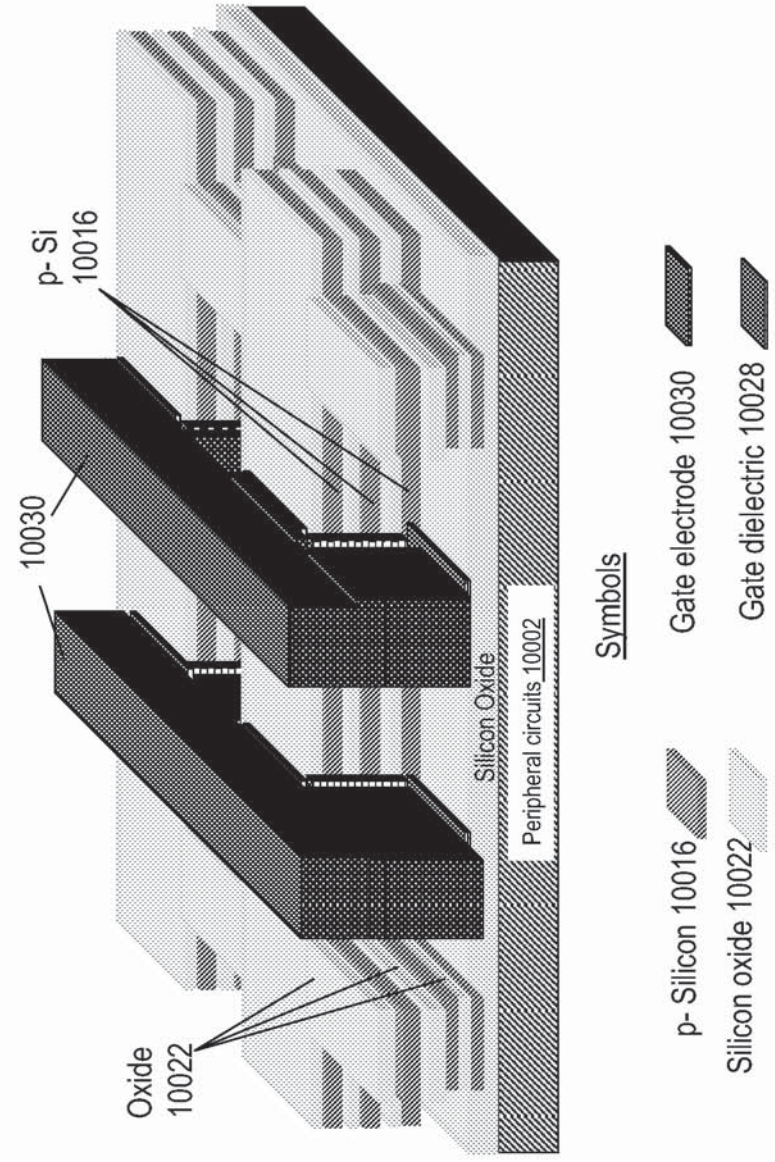

p- Si
10016
10030
Oxide
10022
Silicon Oxide
Peripheral circuits 10002
Symbols
p- Silicon 10016
Silicon oxide 10022
Gate electrode 10030
Gate dielectric 10028

FIG. 100F

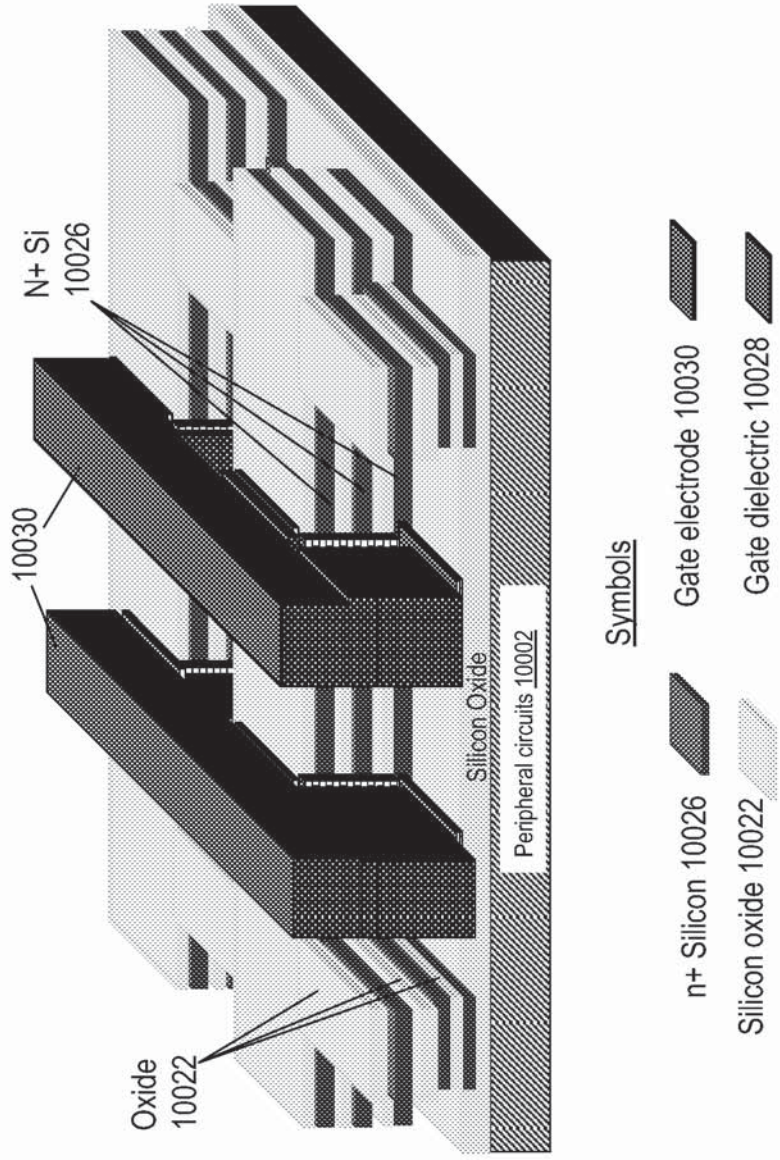

N+ Si
10026
10030
Oxide
10022
Silicon Oxide
Peripheral circuits 10002
Symbols
n+ Silicon 10026
Gate electrode 10030
Silicon oxide 10022
Gate dielectric 10028

FIG. 100G

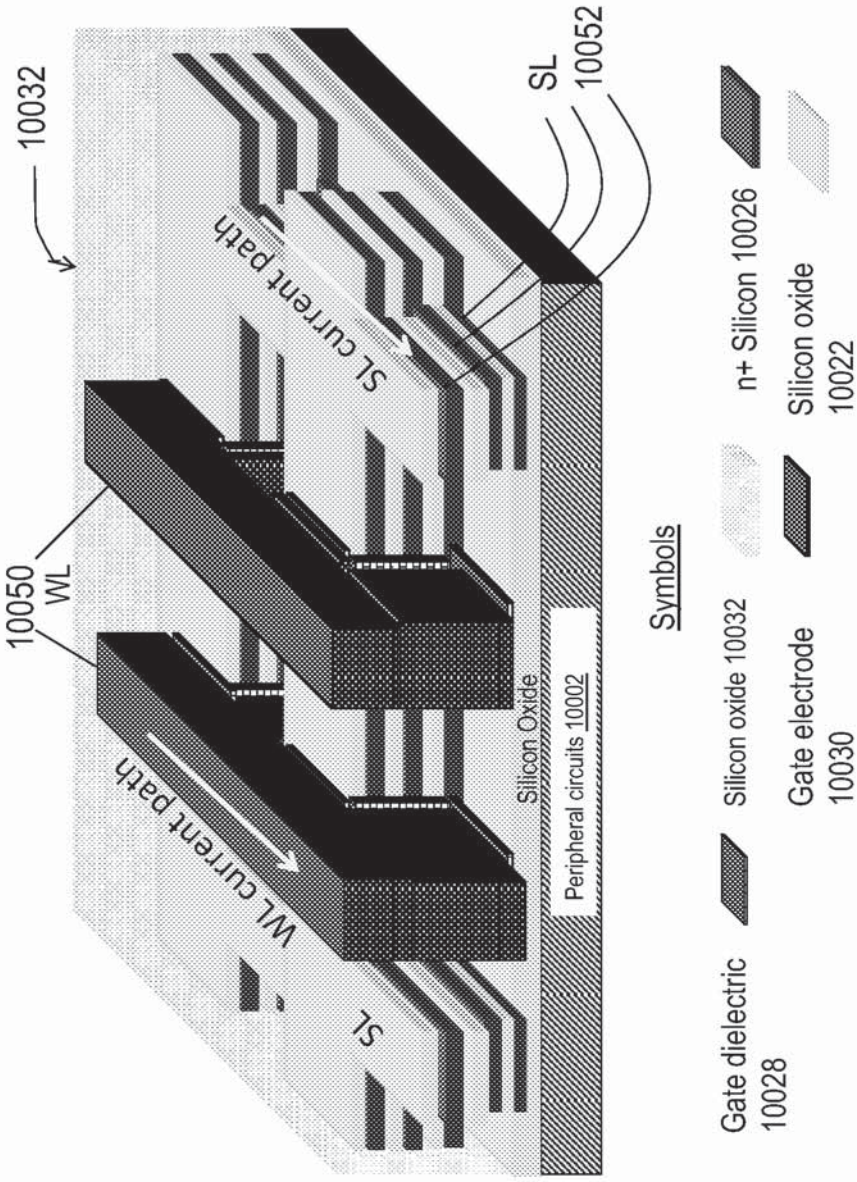

10032
SL
10052
SL current path
10050
WL
WL current path
SL
Silicon Oxide
Peripheral circuits 10002
Symbols
Gate dielectric 10028
Silicon oxide 10032
n+ Silicon 10026
Gate electrode 10030
Silicon oxide 10022

FIG. 100H

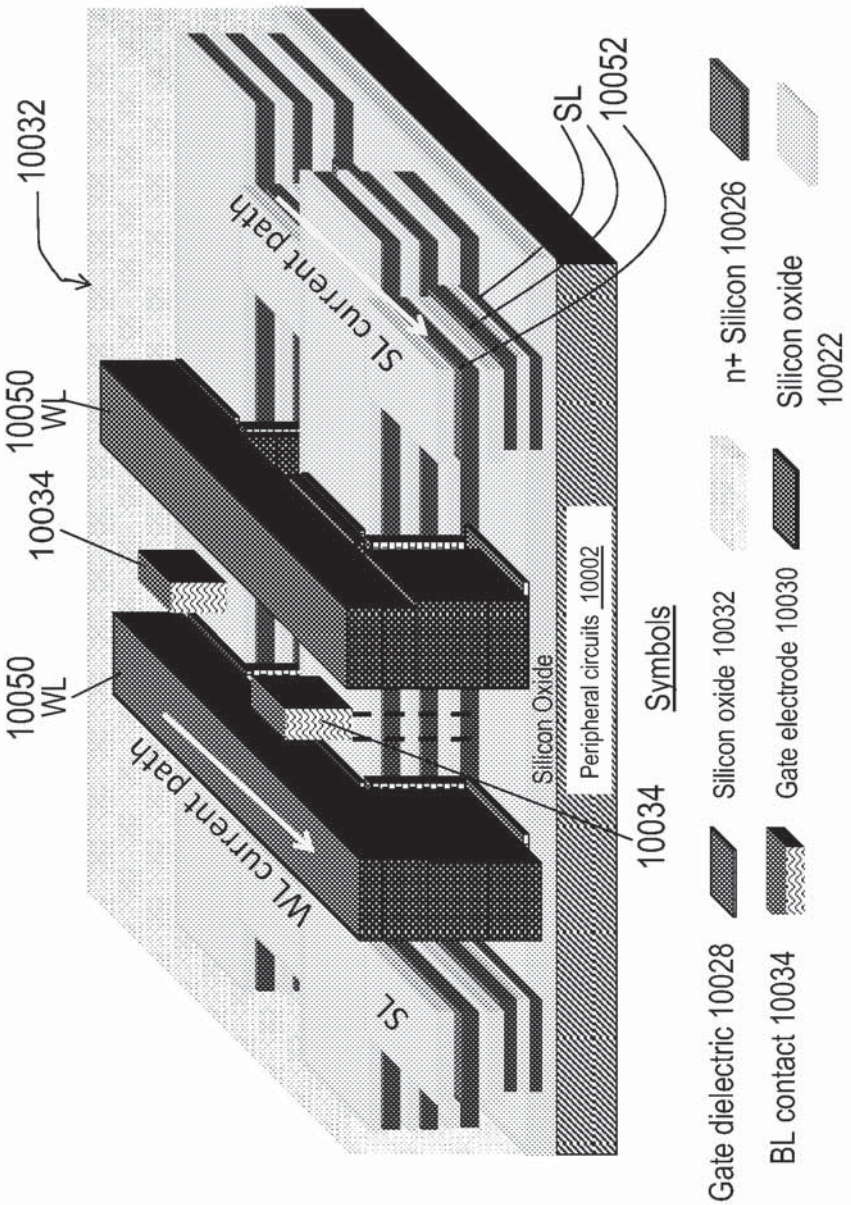

10032
10050
WL
10034
10050
WL
ML current path
SL current path
SL
10052
Silicon Oxide
Peripheral circuits 10002
10034
Symbols
Gate dielectric 10028
Silicon oxide 10032
n+ Silicon 10026
BL contact 10034
Gate electrode 10030
Silicon oxide
10022

FIG. 100I

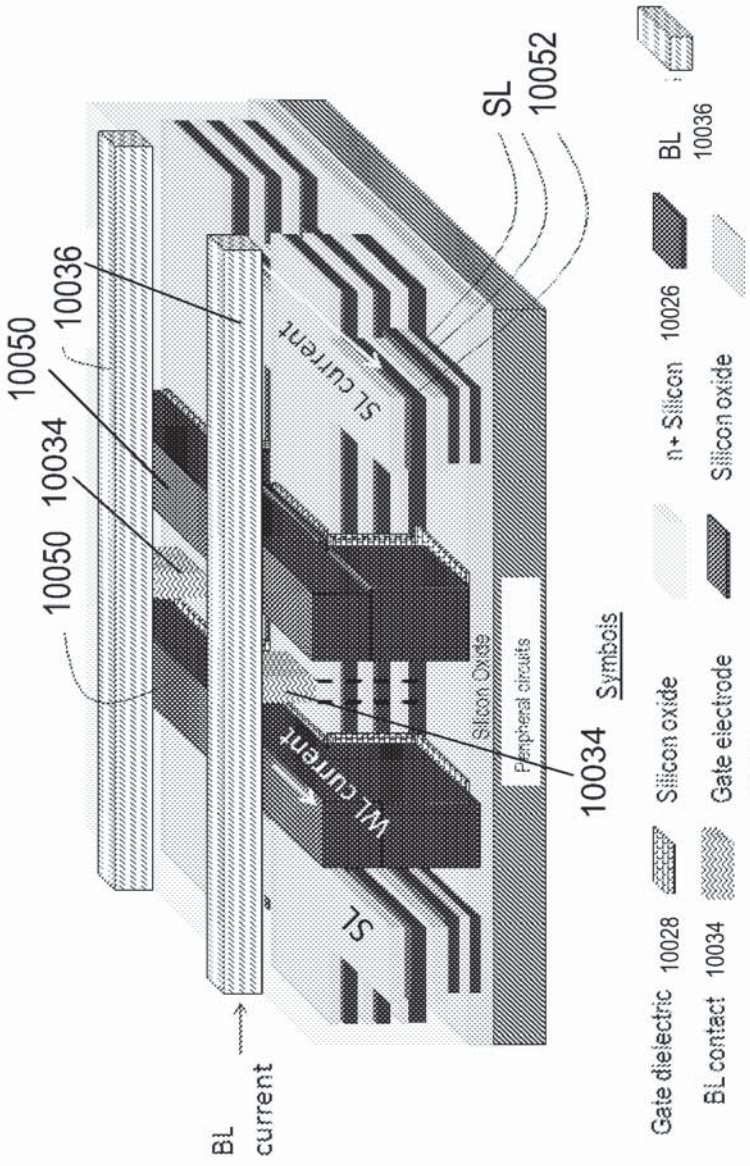

SL
10052
10036
10050
10034
10050
SL current
WL current
SL
BL
current
10034
Silicon Oxide
Peripheral circuits
Symbols
Gate dielectric 10028
BL contact 10034
Silicon oxide
Gate electrode
10030
n+ Silicon 10026
Silicon oxide
BL
10036

FIG. 100J

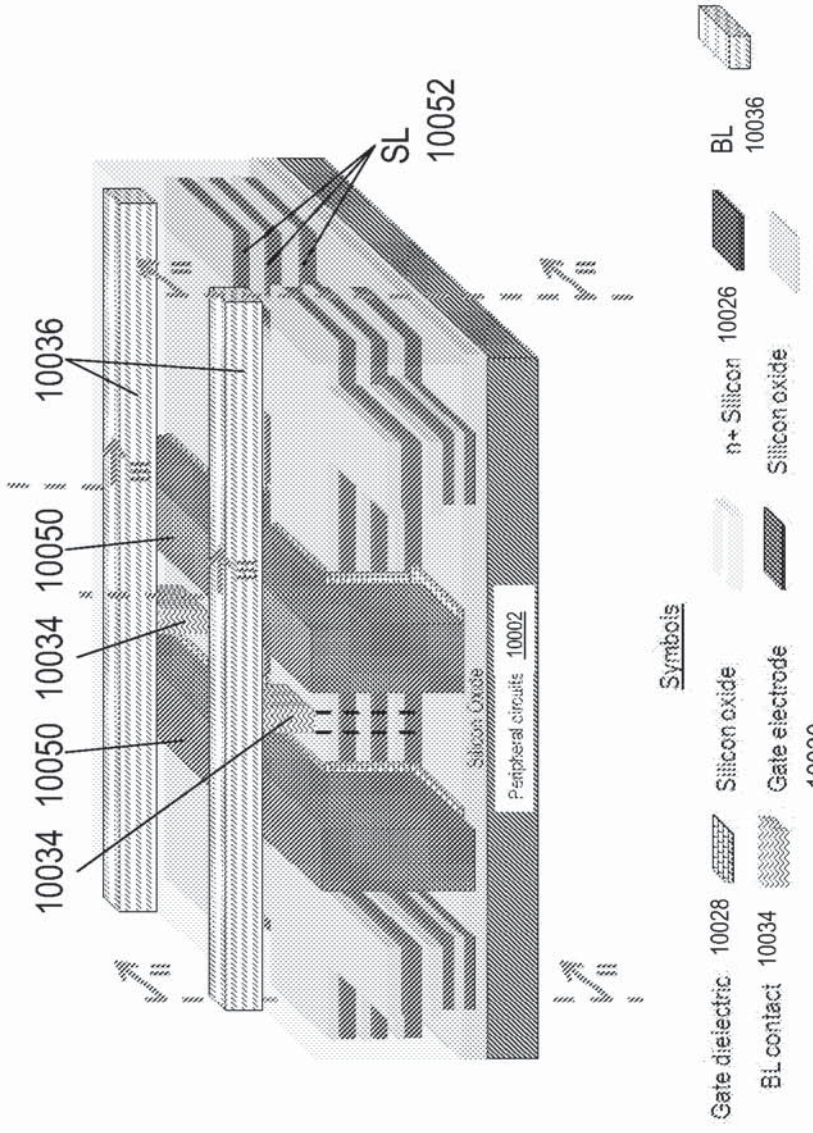

10034
10050
10034
10050
10036
SL
10052
Peripheral circuits 10002
Silicon oxide
Symbols
Gate dielectric 10028
Silicon oxide
n+ Silicon 10026
BL
10036
Bl contact 10034
Gate electrode
10030
Silicon oxide

FIG. 100K

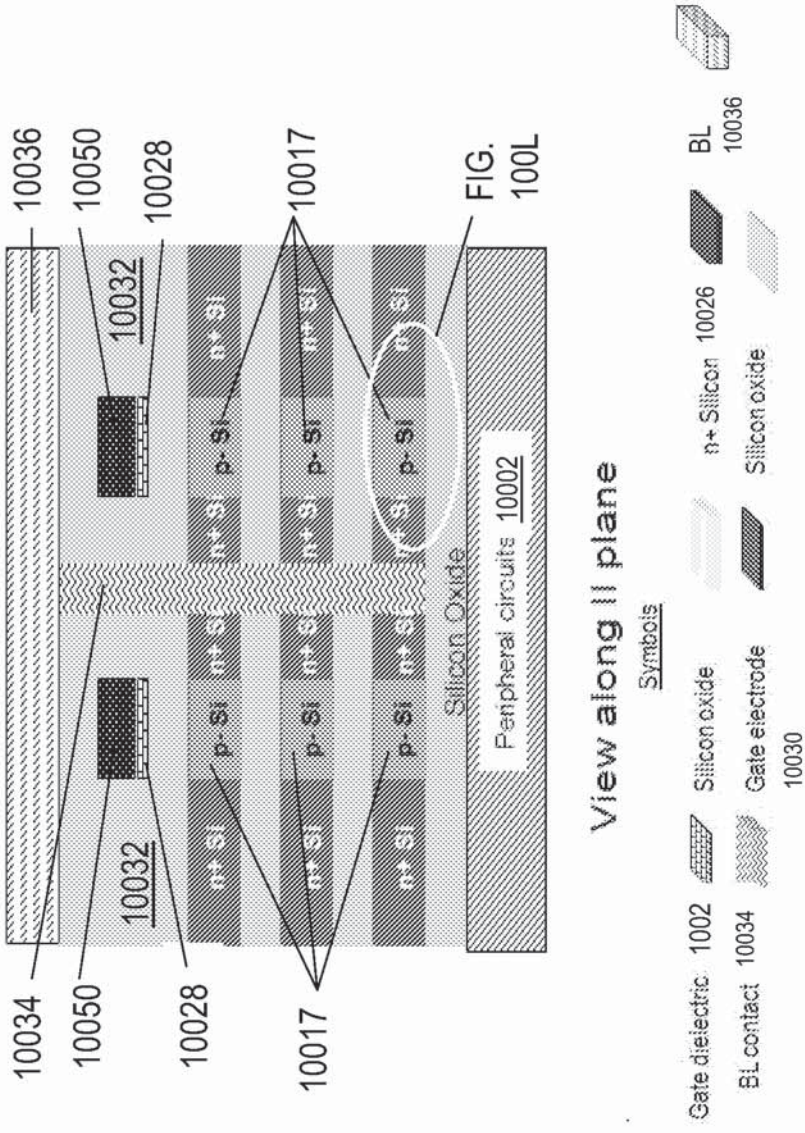

10036
10050
10028
10032
10017
FIG. 100L
10034
10050
10028
10032
10017
n+ Si
p- Si
Silicon Oxide
Peripheral circuits 10002
View along II plane
Symbols
Gate dielectric 1002
Silicon oxide
n+ Silicon 10026
BL 10036
BL contact 10034
Gate electrode 10030
Silicon oxide

FIG. 100K1

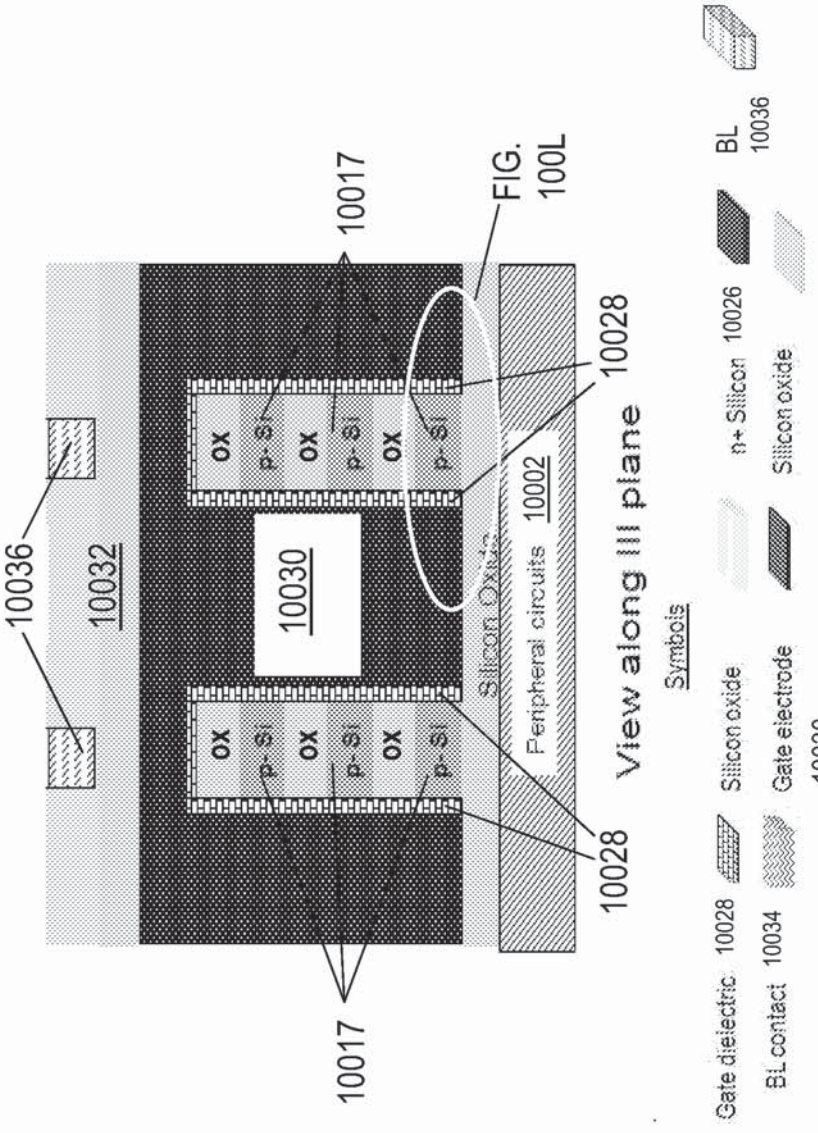

10036
10032
10030
10017
10017
FIG. 100L
10028
10028
ox
p- Si
Peripheral circuits 10002
Silicon Oxide
View along III plane
Symbols
Gate dielectric 10028
Silicon oxide
n+ Silicon 10026
BL 10036
BL contact 10034
Gate electrode 10030
Silicon oxide

FIG. 100K2

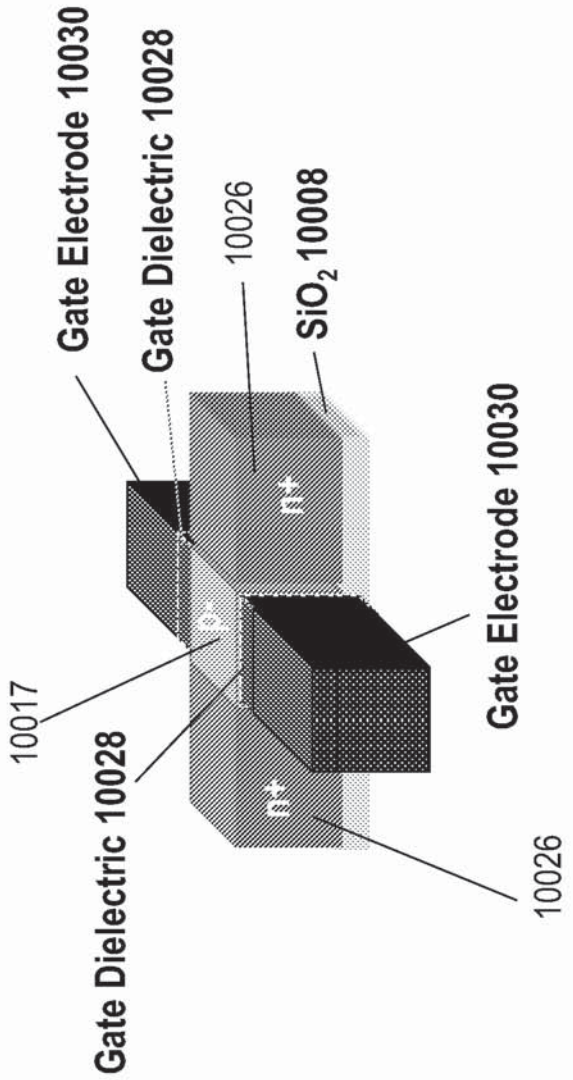

Gate Electrode 10030
Gate Dielectric 10028
10026
SiO_2 10008
n+
n+
10017
Gate Dielectric 10028
Gate Electrode 10030
10026

FIG. 100L


Silicon Oxide 10104
Peripheral circuits with W wiring 10102
10114

FIG. 101A

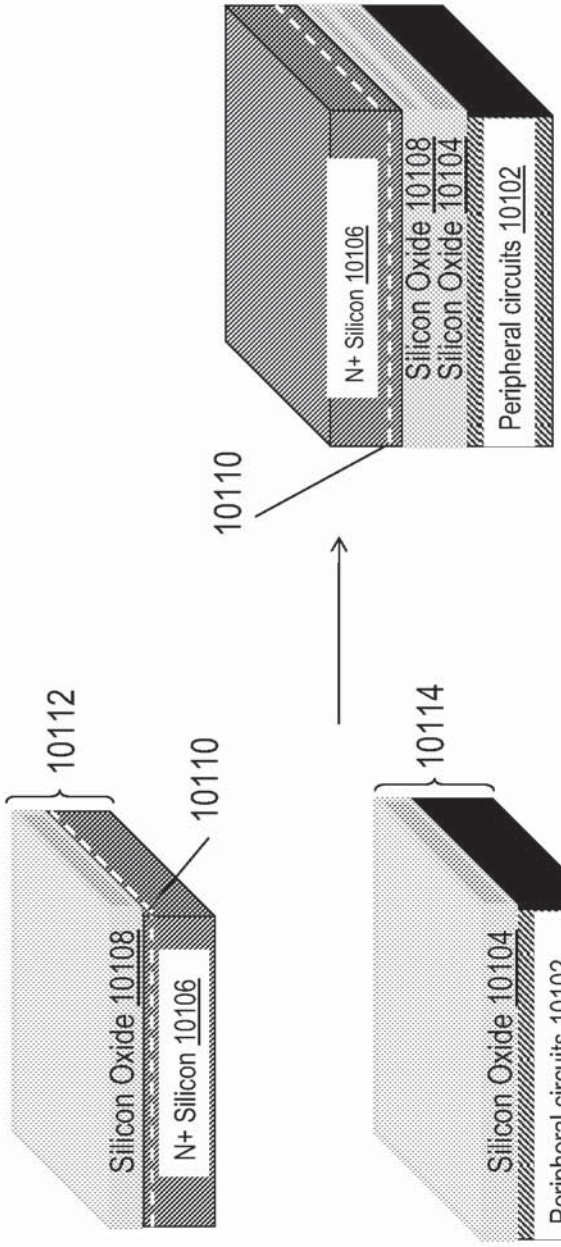

10112
10110
Silicon Oxide 10108
N+ Silicon 10106
10110
N+ Silicon 10106
Silicon Oxide 10108
Silicon Oxide 10104
Peripheral circuits 10102
10114
Silicon Oxide 10104
Peripheral circuits 10102

FIG. 101B

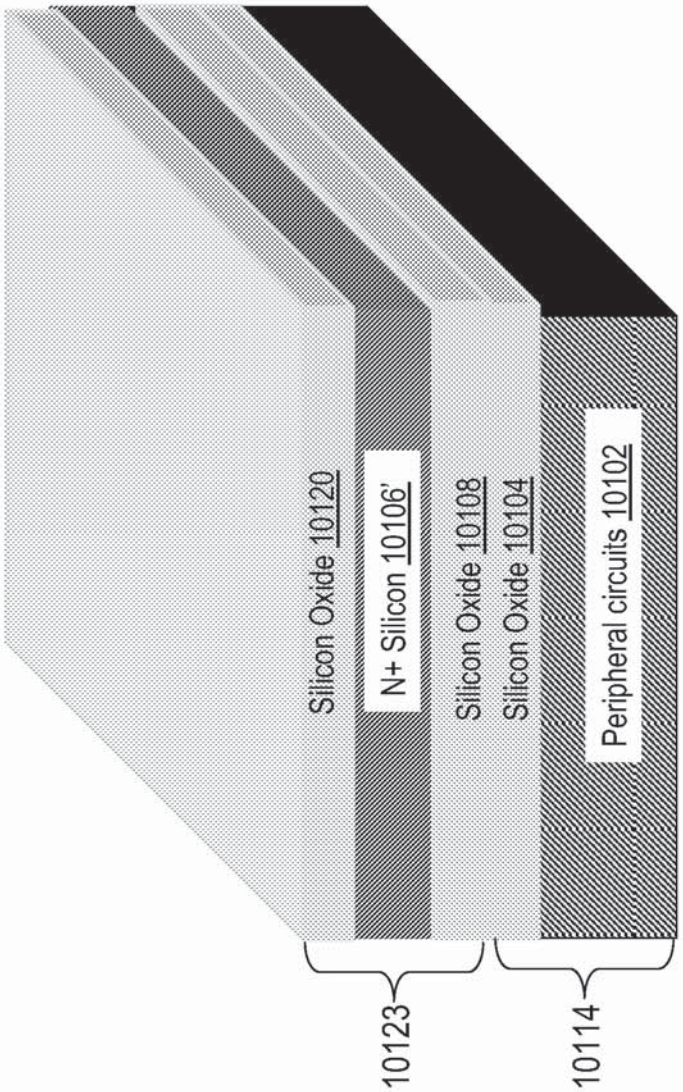

Silicon Oxide 10120
N+ Silicon 10106'
Silicon Oxide 10108
Silicon Oxide 10104
Peripheral circuits 10102
10123
10114

FIG. 101C

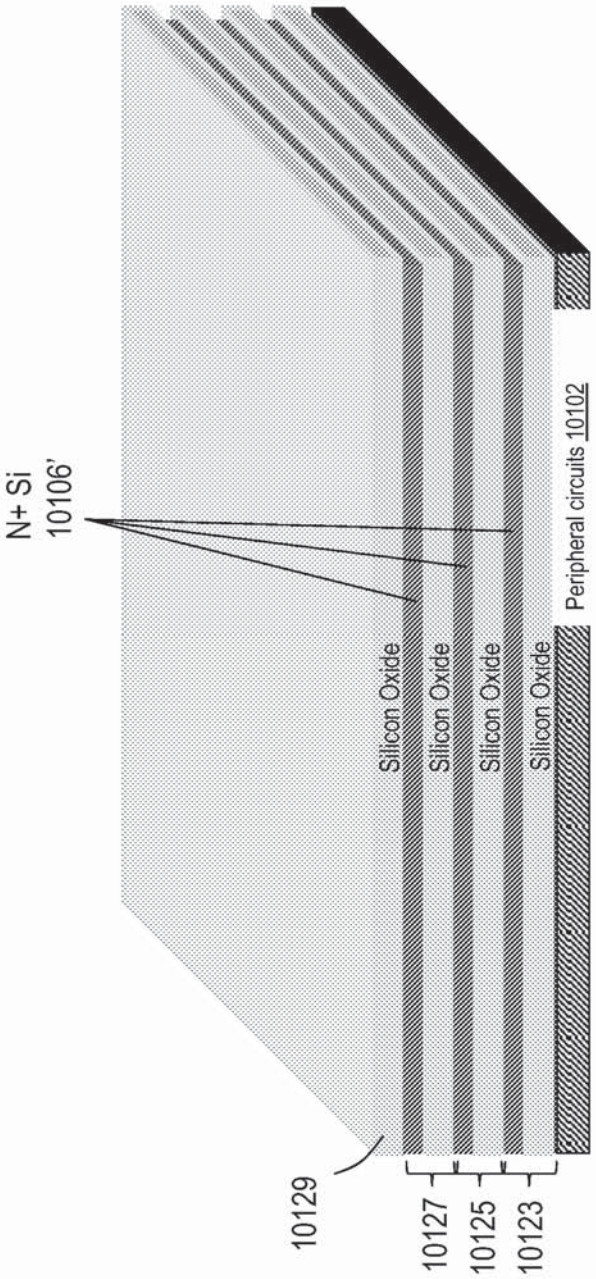

N+ Si
10106'
Silicon Oxide
Silicon Oxide
Silicon Oxide
Silicon Oxide
Peripheral circuits 10102
10129
10127
10125
10123

FIG. 101D

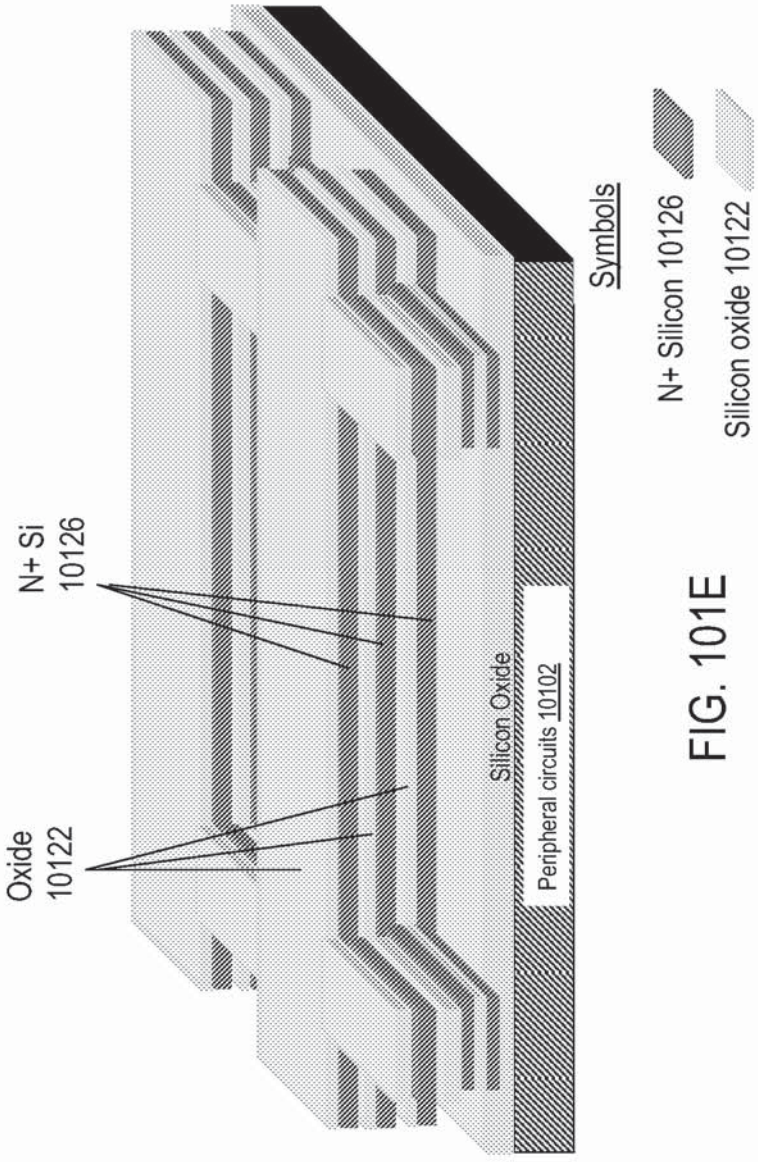

Oxide
10122
N+ Si
10126
Silicon Oxide
Peripheral circuits 10102
Symbols
N+ Silicon 10126
Silicon oxide 10122

FIG. 101E

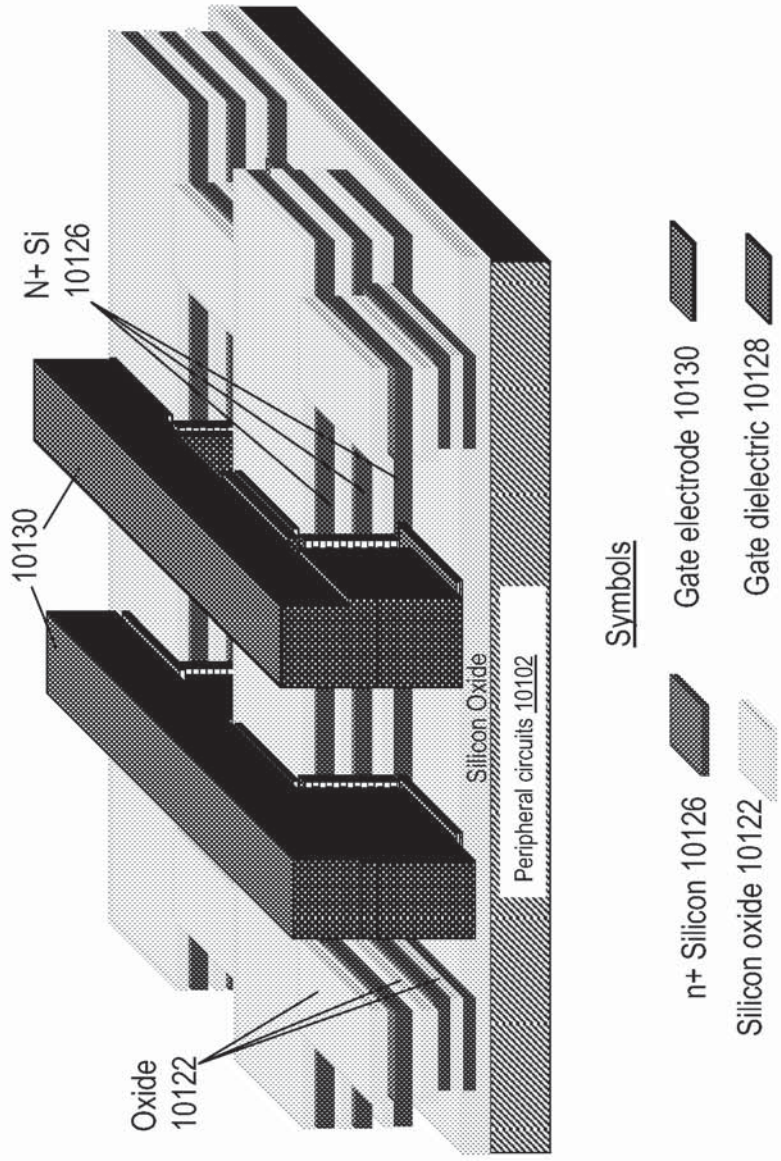

N+ Si
10126
10130
Oxide
10122
Silicon Oxide
Peripheral circuits 10102
Symbols
n+ Silicon 10126
Gate electrode 10130
Silicon oxide 10122
Gate dielectric 10128

FIG. 101F

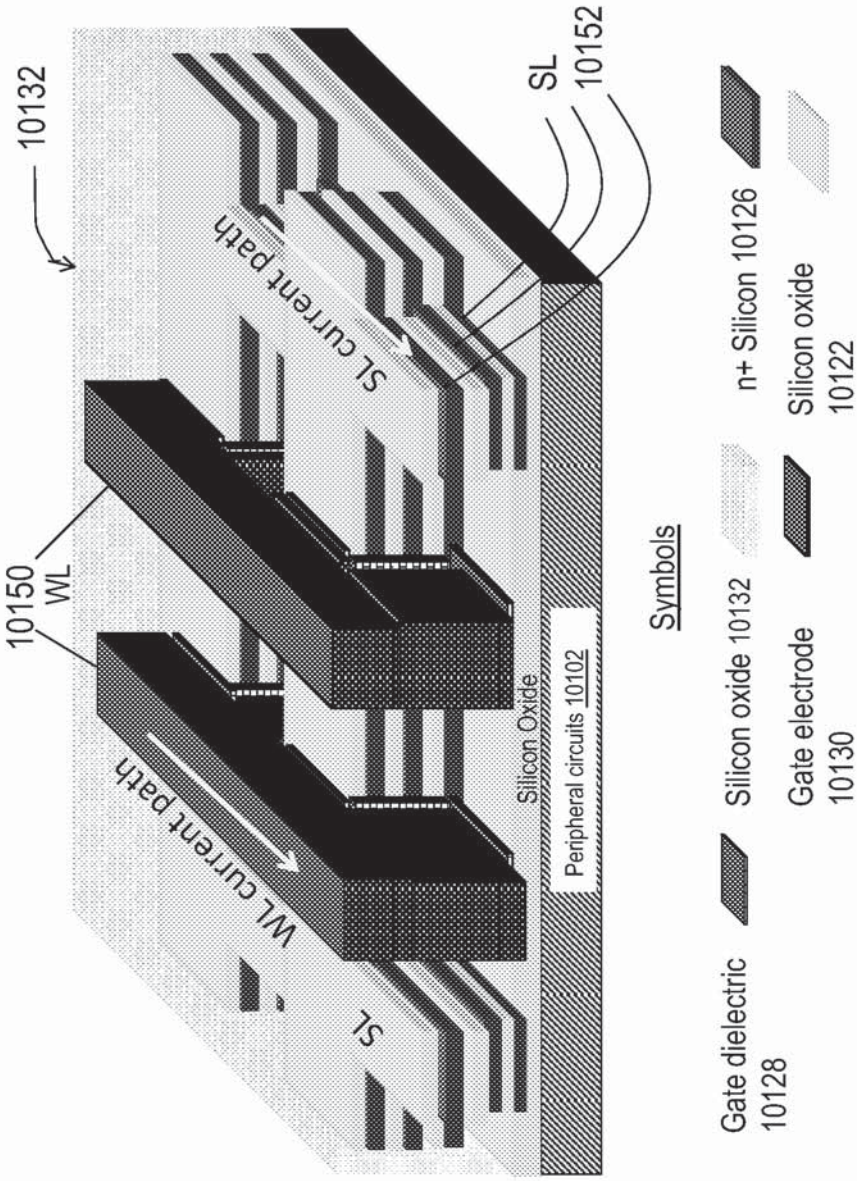

10132
SL
10152
SL current path
10150
WL
WL current path
SL
Silicon Oxide
Peripheral circuits 10102
Symbols
Gate dielectric 10128
Silicon oxide 10132
n+ Silicon 10126
Gate electrode 10130
Silicon oxide 10122

FIG. 101G

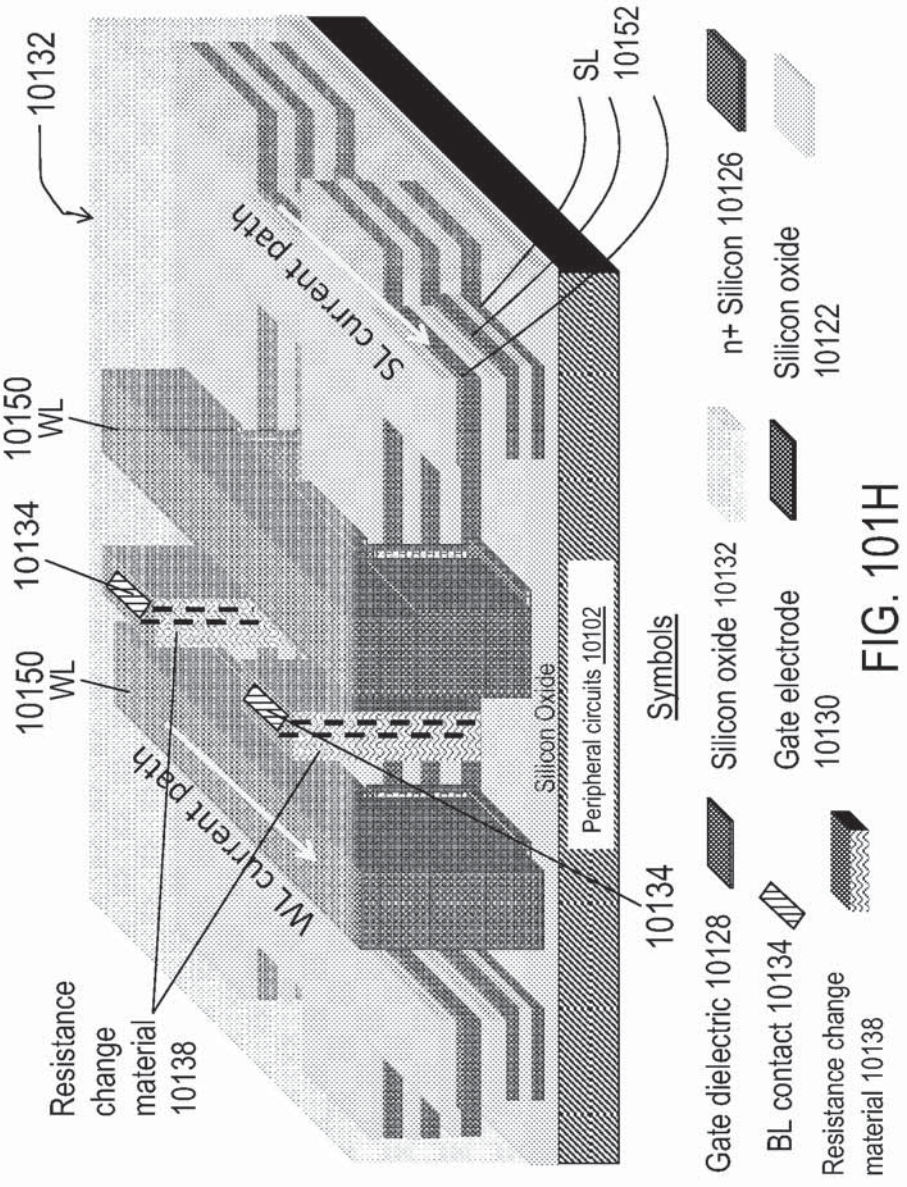

10132
SL
10152
SL current path
10150
WL
10134
10150
WL
WL current path
Resistance
change
material
10138
Silicon Oxide
Peripheral circuits 10102
10134
Symbols
Gate dielectric 10128
Silicon oxide 10132
n+ Silicon 10126
BL contact 10134
Gate electrode
10130
Silicon oxide
10122
Resistance change
material 10138

FIG. 101H

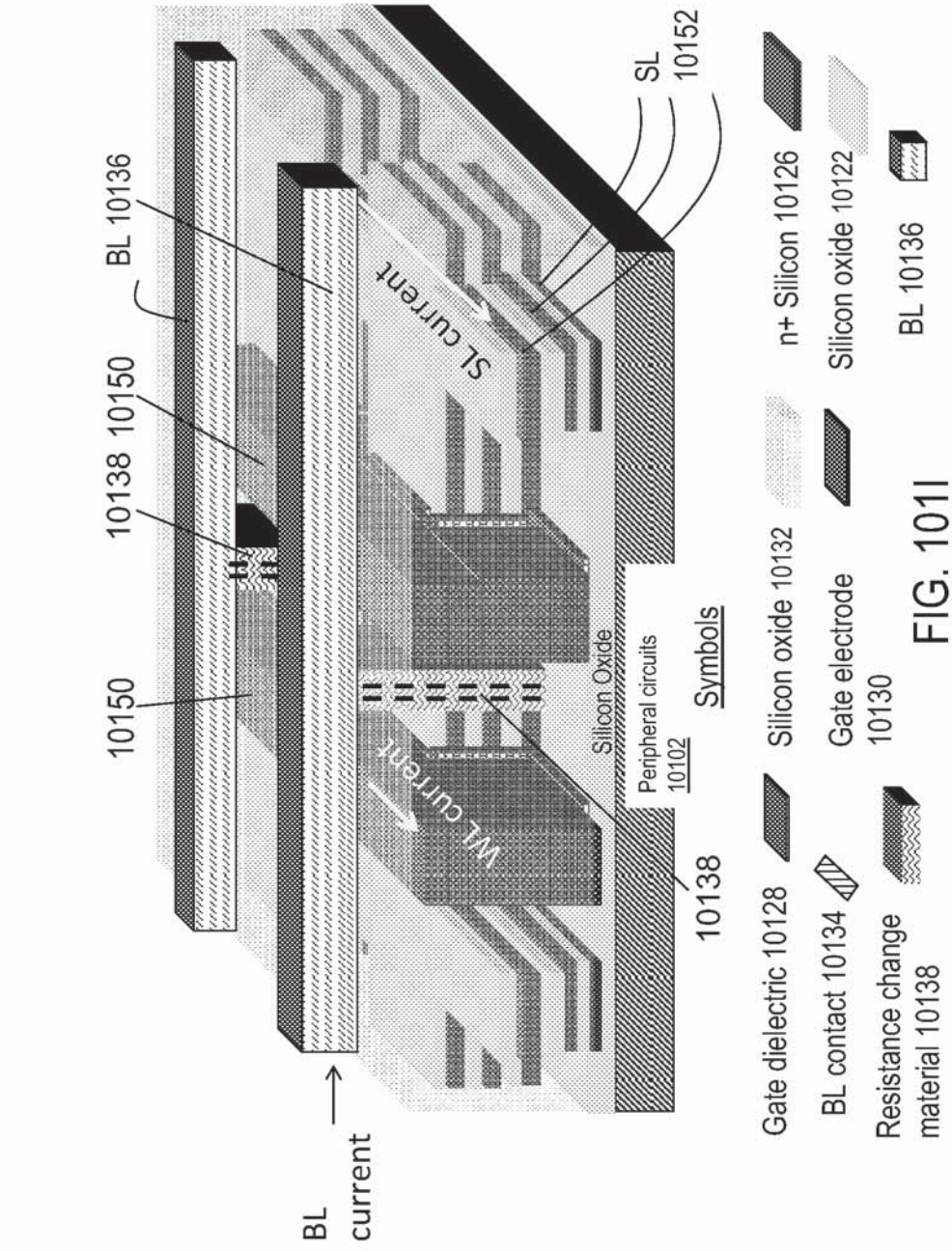

BL 10136
10138 10150
10150
SL
10152
SL current
WL current
Silicon Oxide
Peripheral circuits
10102
10138
BL
current
Symbols
Gate dielectric 10128
Silicon oxide 10132
n+ Silicon 10126
BL contact 10134
Gate electrode
10130
Silicon oxide 10122
Resistance change
material 10138
BL 10136

FIG. 101I

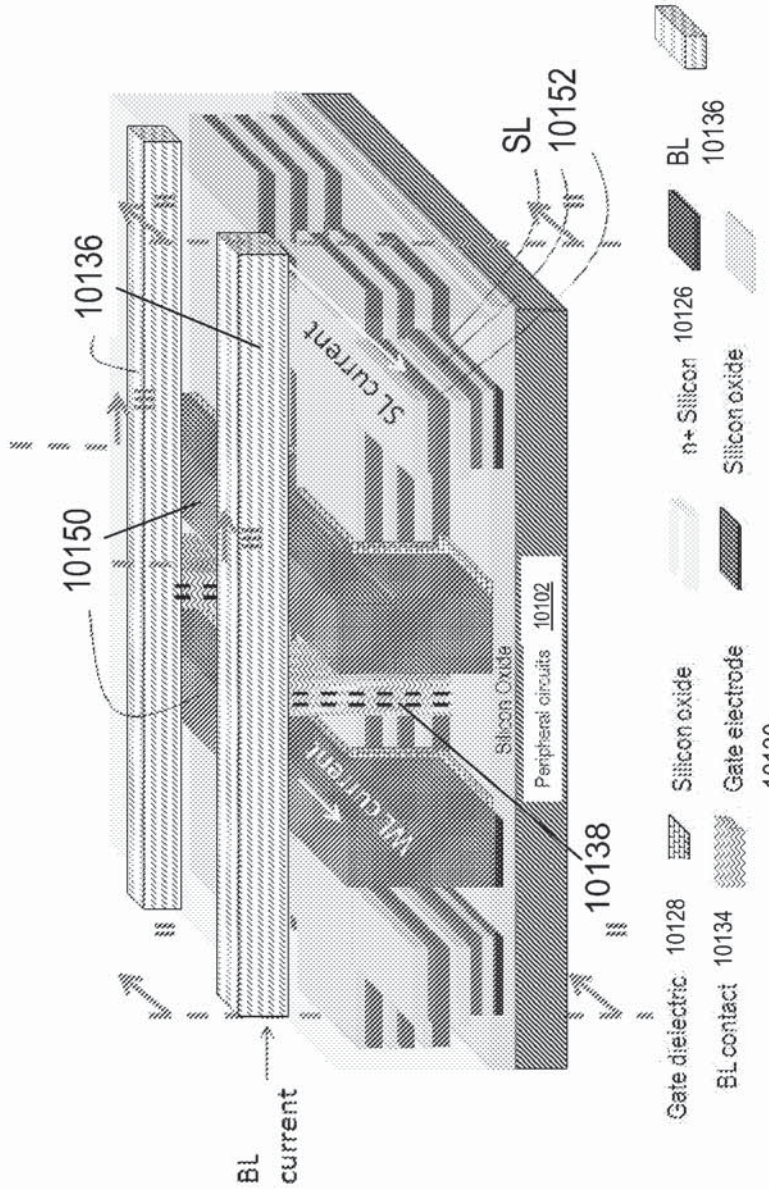

10136
10150
SL current
SL
10152
BL
10136
n+ Silicon 10126
Silicon oxide
Silicon Oxide
Peripheral circuits 10102
WL current
10138
BL
current
Gate dielectric 10128
Silicon oxide
Bl contact 10134
Gate electrode
10130
Resistance change
material 10138

FIG. 101J

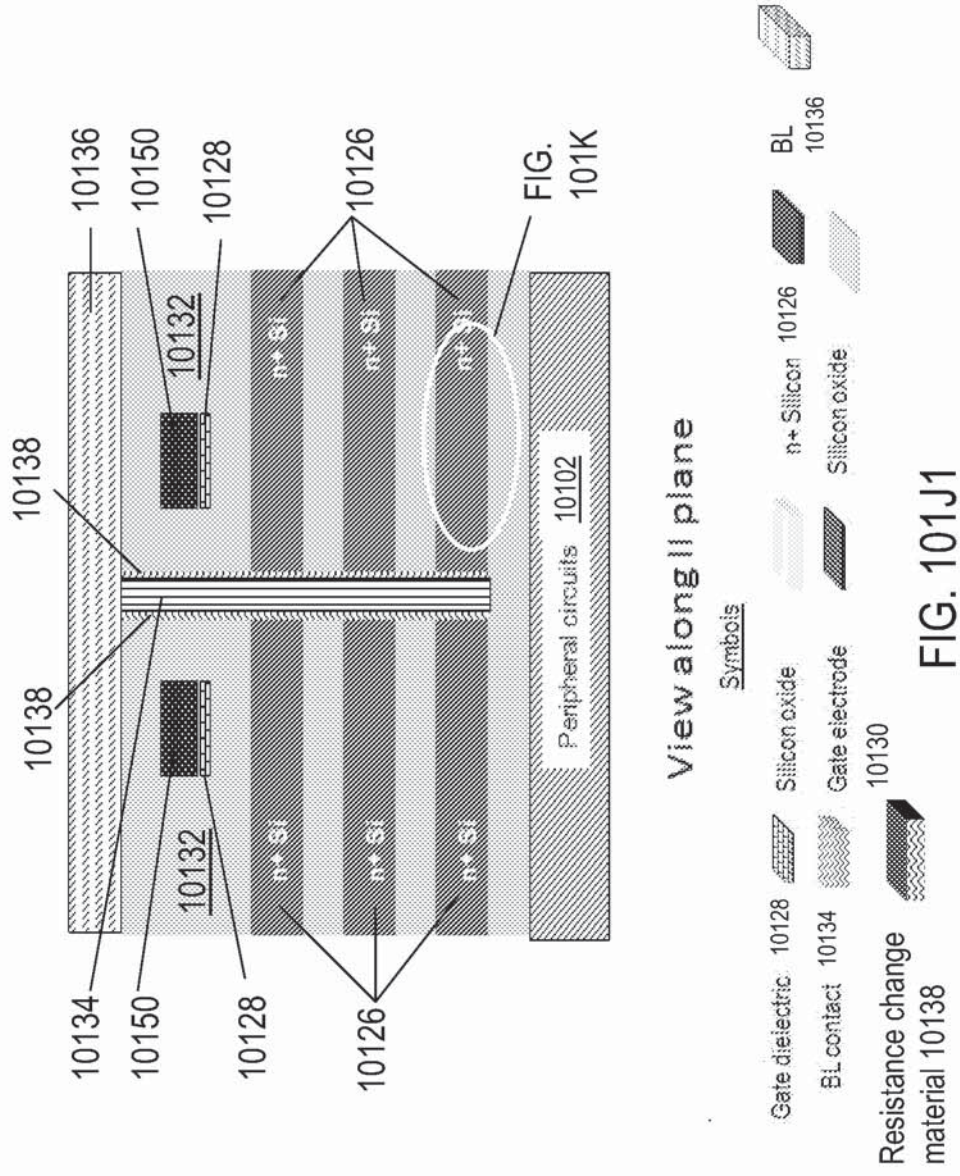

10136
10150
10128
10126
FIG. 101K
10132
10138
10138
n+ Si
n+ Si
n+ Si
n+ Si
n+ Si
n+ Si
Peripheral circuits 10102
10134
10150
10128
10126
View along II plane
Symbols
Gate dielectric 10128
Silicon oxide
n+ Silicon 10126
BL 10136
BL contact 10134
Gate electrode 10130
Silicon oxide
Resistance change material 10138

FIG. 101J1

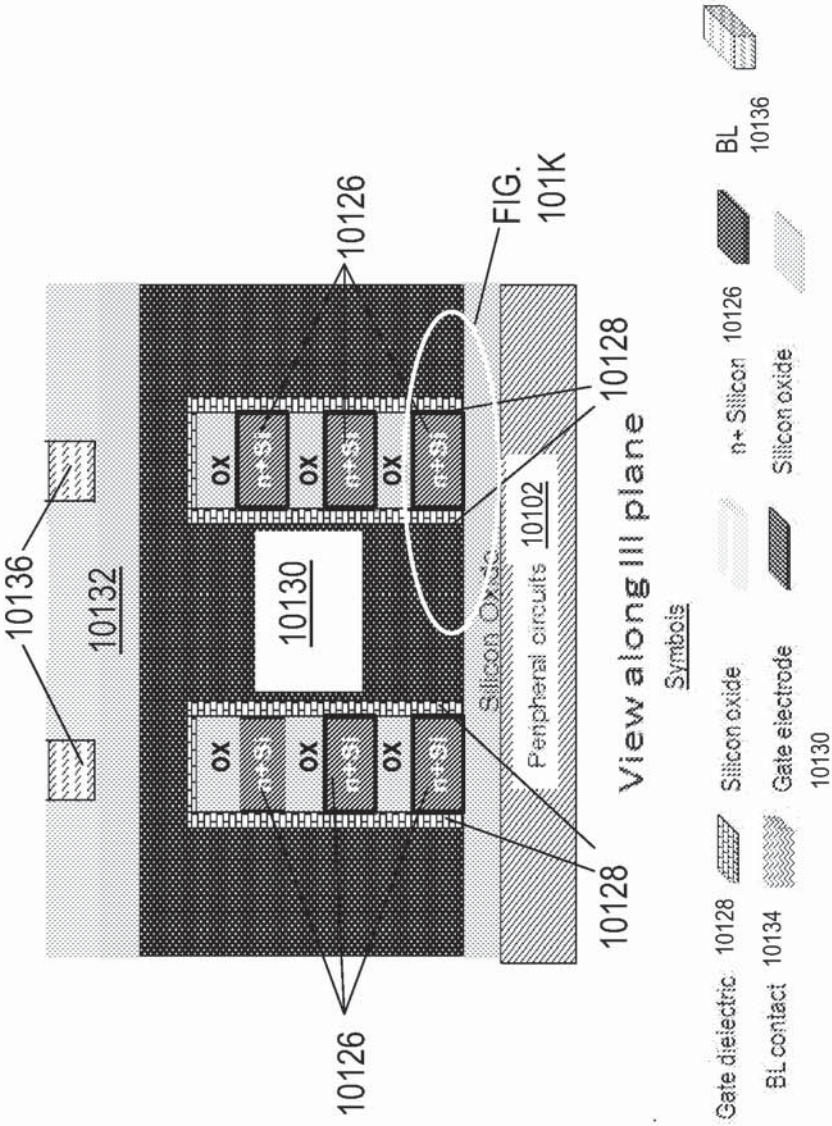

10136
10132
10130
10126
10126
FIG. 101K
10128
10128
Silicon Oxide
Peripheral circuits 10102
View along III plane
Symbols
Gate dielectric 10128
Silicon oxide
n+ Silicon 10126
BL 10136
BL contact 10134
Gate electrode 10130
Silicon oxide
ox
n+Si

FIG. 101J2

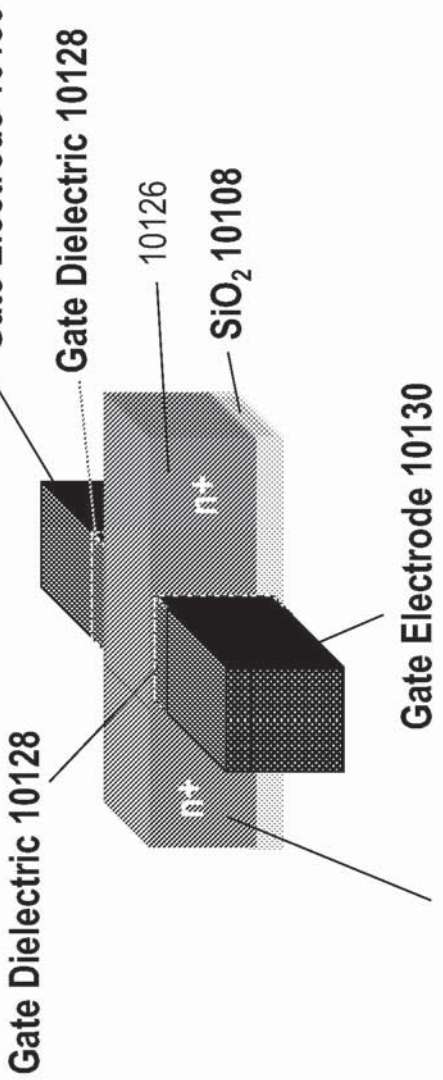

Gate Electrode 10130
Gate Dielectric 10128
10126
SiO_2 10108
n+
n+
Gate Electrode 10130
Gate Dielectric 10128
10126

FIG. 101K


Silicon Oxide 10204
Peripheral circuits with W wiring 10202
10214

FIG. 102A

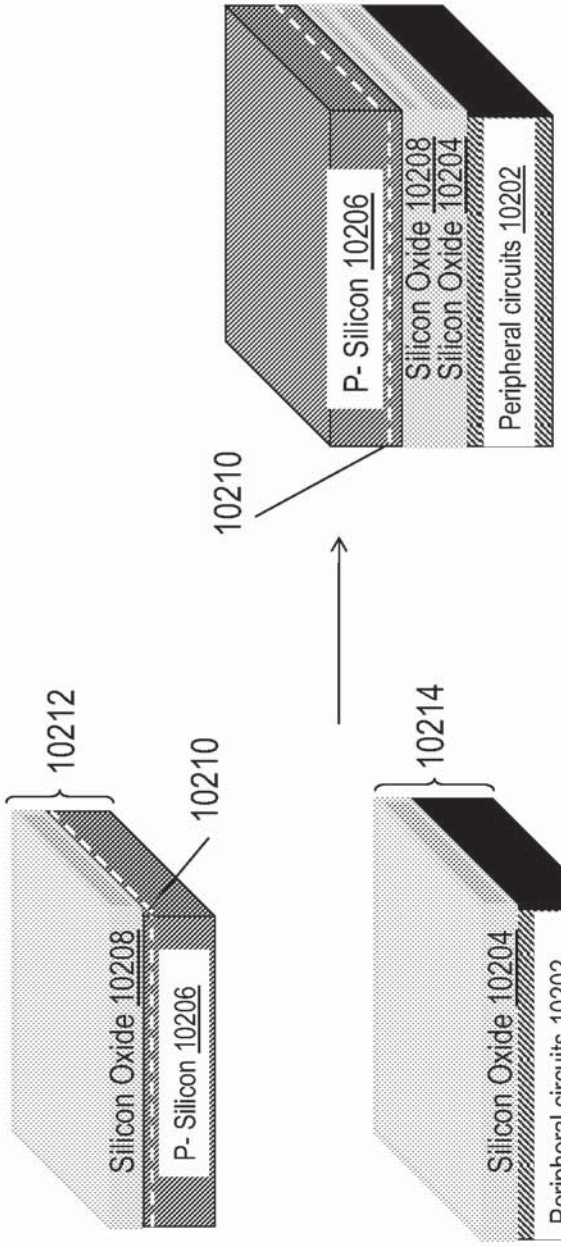

10212
10210
Silicon Oxide 10208
P- Silicon 10206
10214
Silicon Oxide 10204
Peripheral circuits 10202
10210
P- Silicon 10206
Silicon Oxide 10208
Silicon Oxide 10204
Peripheral circuits 10202

FIG. 102B

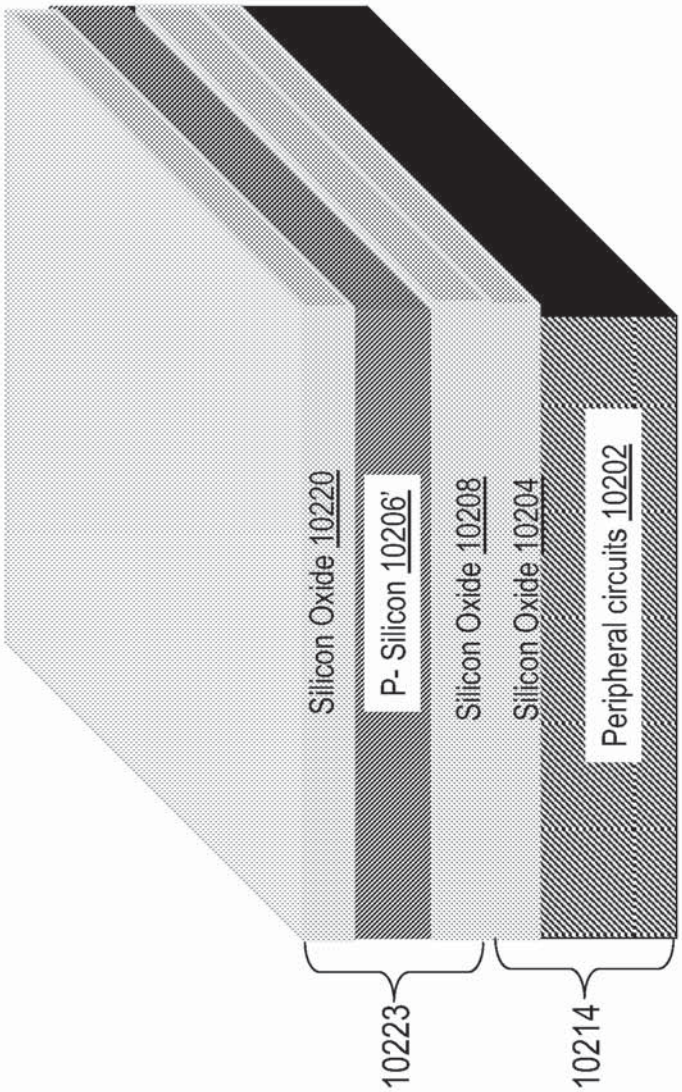

Silicon Oxide 10220
P- Silicon 10206'
Silicon Oxide 10208
Silicon Oxide 10204
Peripheral circuits 10202
10223
10214

FIG. 102C

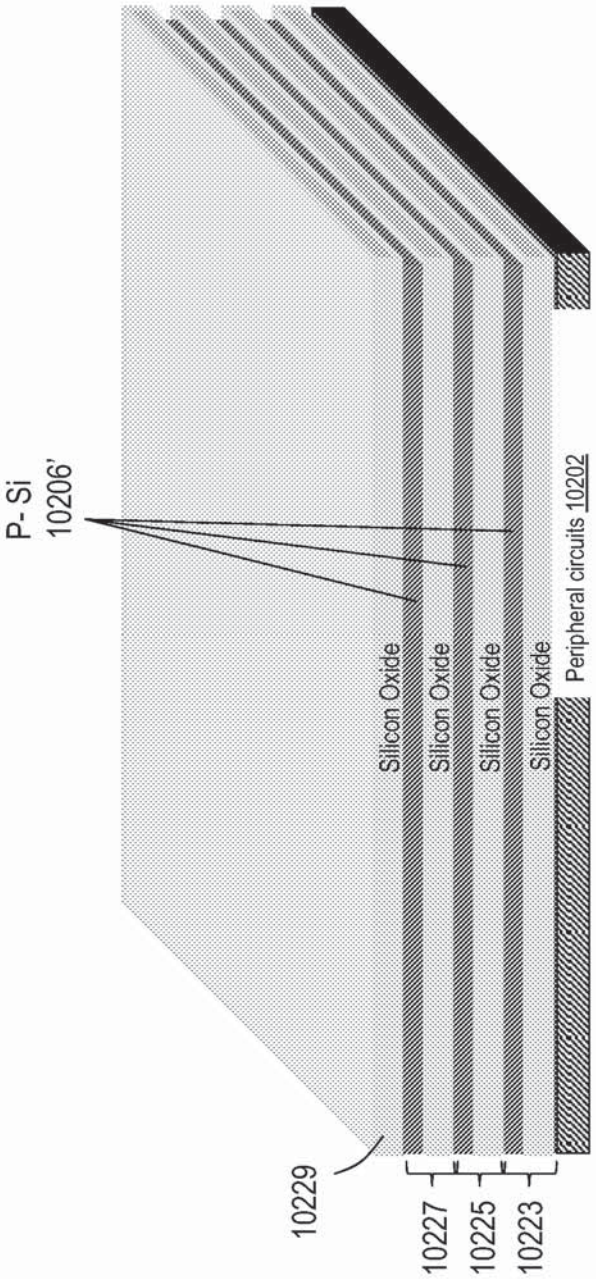

P- Si
10206'
Silicon Oxide
Silicon Oxide
Silicon Oxide
Silicon Oxide
Peripheral circuits 10202
10229
10227
10225
10223

FIG. 102D

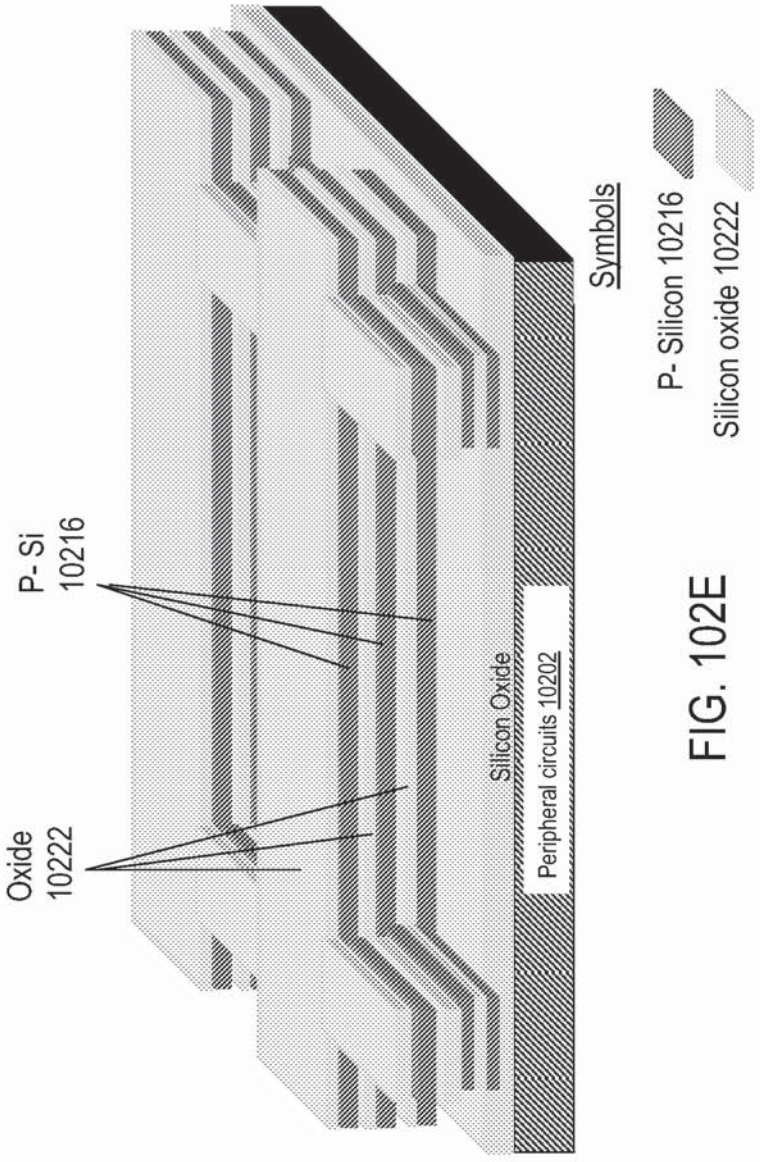

P- Si
10216
Oxide
10222
Silicon Oxide
Peripheral circuits 10202
Symbols
P- Silicon 10216
Silicon oxide 10222

FIG. 102E

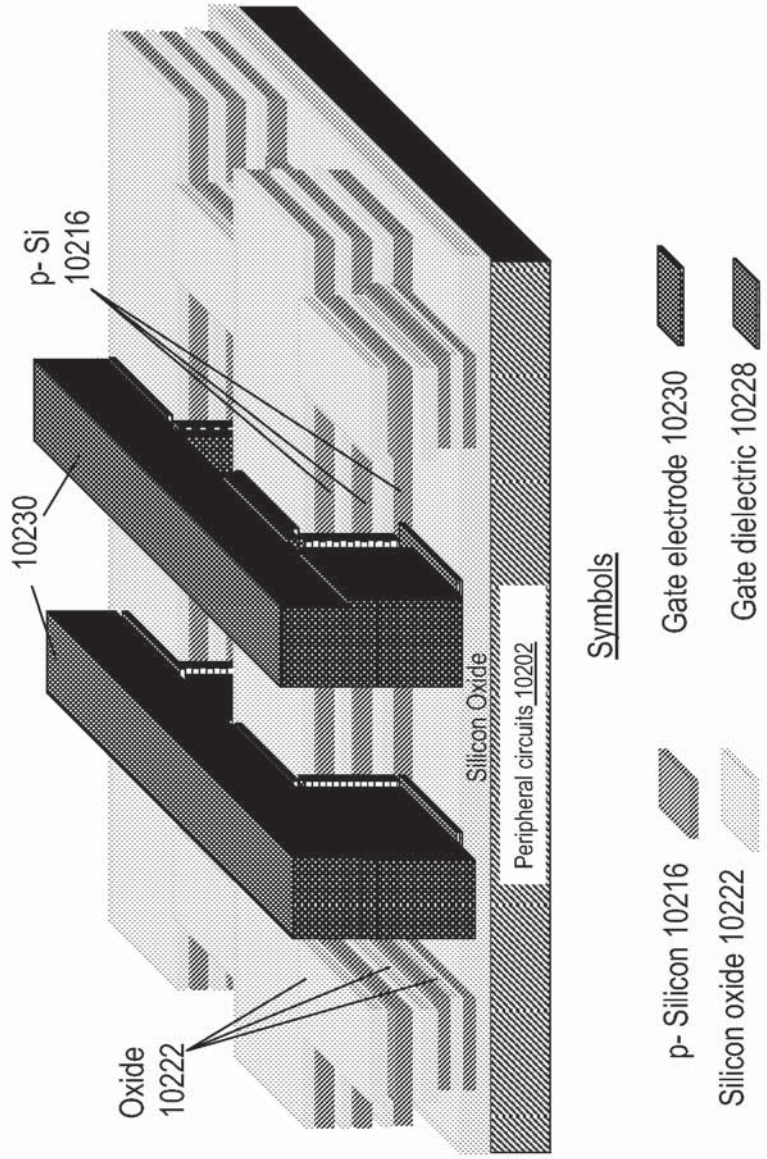

p- Si
10216
10230
Oxide
10222
Silicon Oxide
Peripheral circuits 10202
Symbols
p- Silicon 10216
Silicon oxide 10222
Gate electrode 10230
Gate dielectric 10228

FIG. 102F

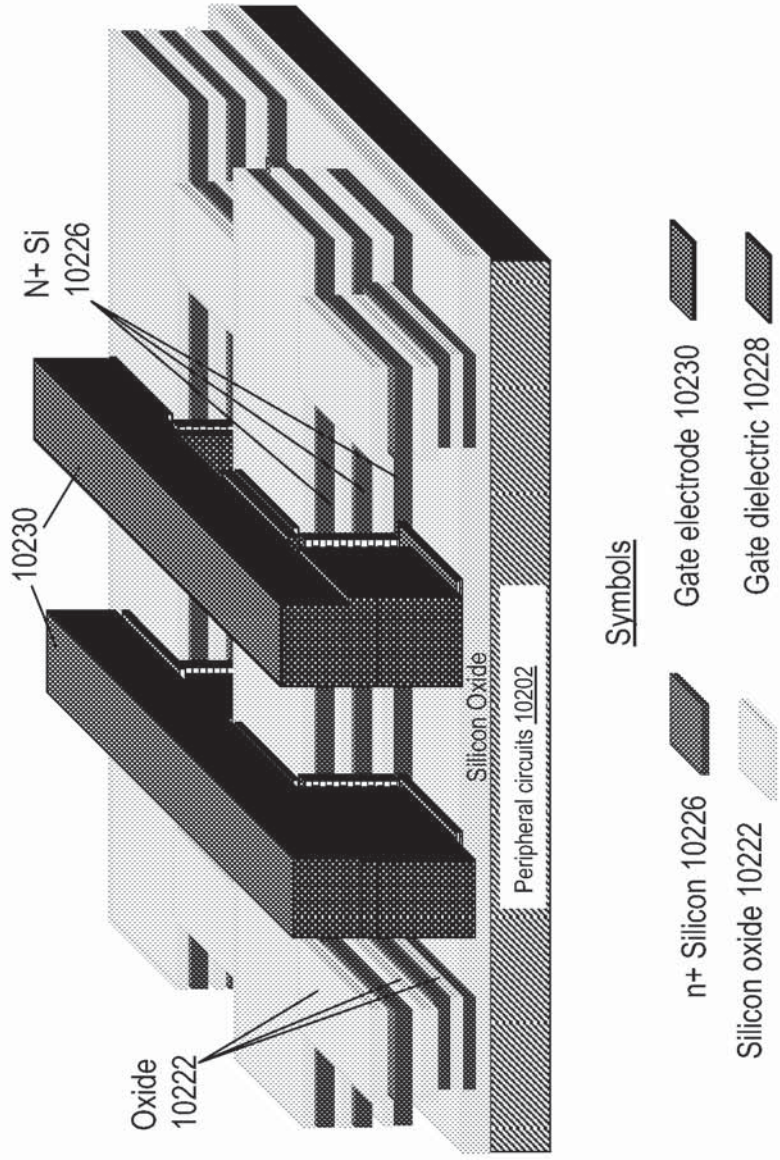

N+ Si
10226
10230
Oxide
10222
Silicon Oxide
Peripheral circuits 10202
Symbols
n+ Silicon 10226
Gate electrode 10230
Silicon oxide 10222
Gate dielectric 10228

FIG. 102G

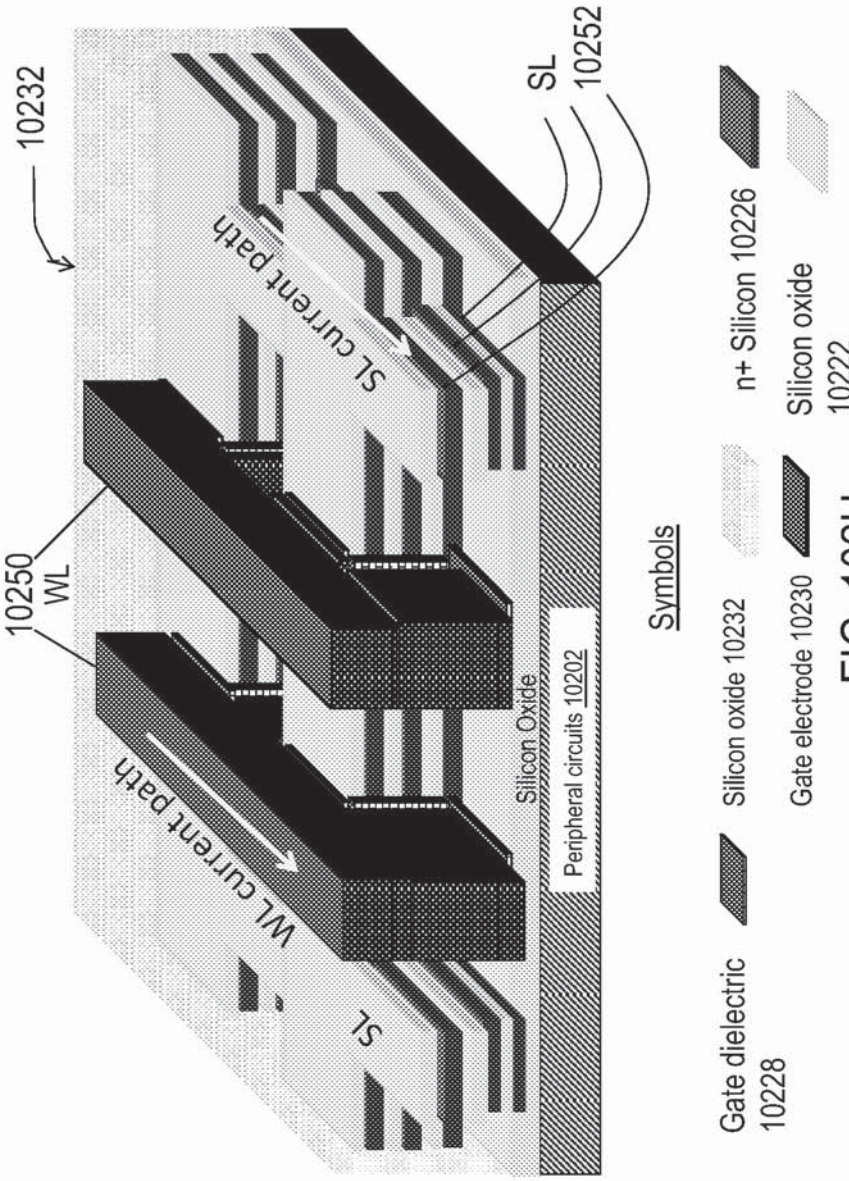

10232
SL
10252
SL current path
10250
WL
WL current path
SL
Silicon Oxide
Peripheral circuits 10202
Symbols
Gate dielectric 10228
Silicon oxide 10232
Gate electrode 10230
n+ Silicon 10226
Silicon oxide 10222

FIG. 102H

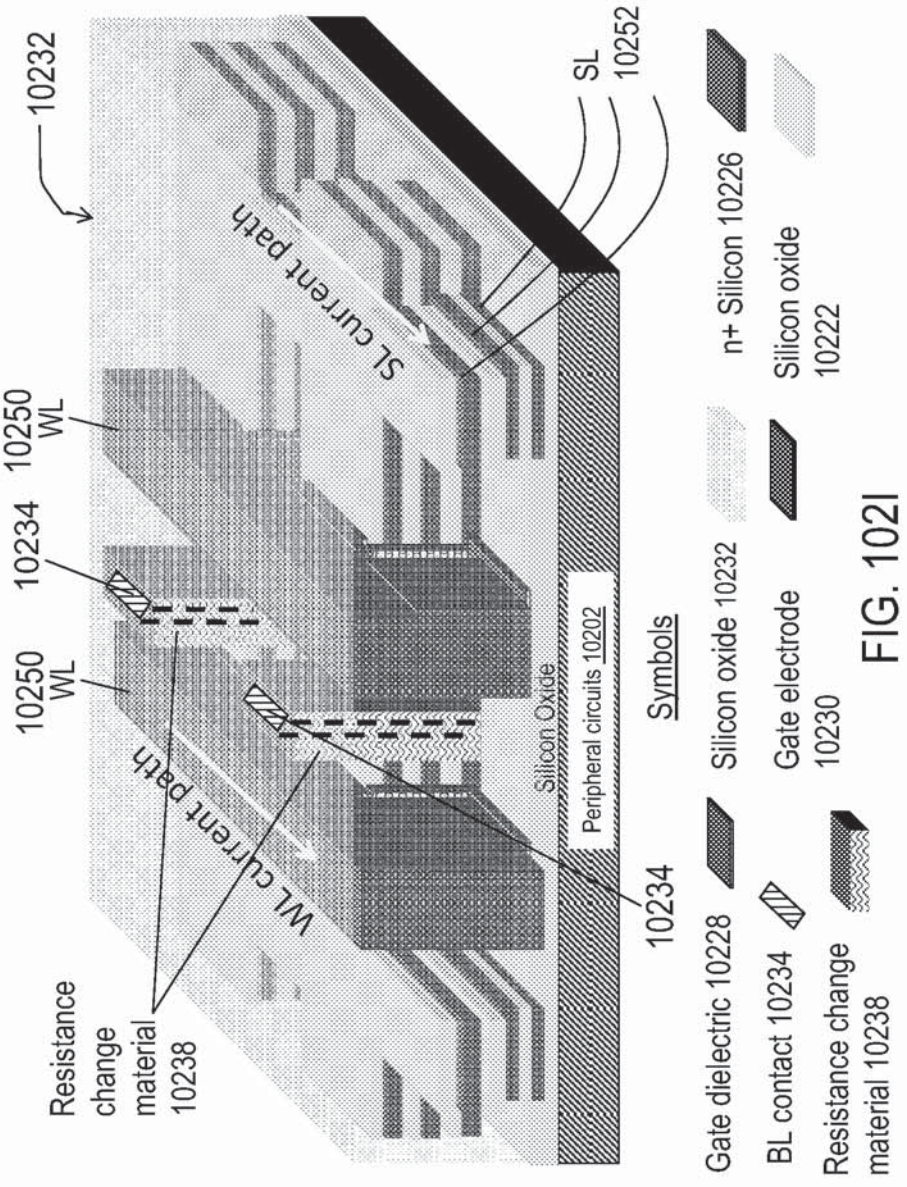

10232
SL
10252
SL current path
10250
WL
10234
10250
WL
WL current path
Resistance
change
material
10238
Silicon Oxide
Peripheral circuits 10202
10234
Symbols
Gate dielectric 10228
Silicon oxide 10232
n+ Silicon 10226
BL contact 10234
Gate electrode
10230
Silicon oxide
10222
Resistance change
material 10238

FIG. 102I

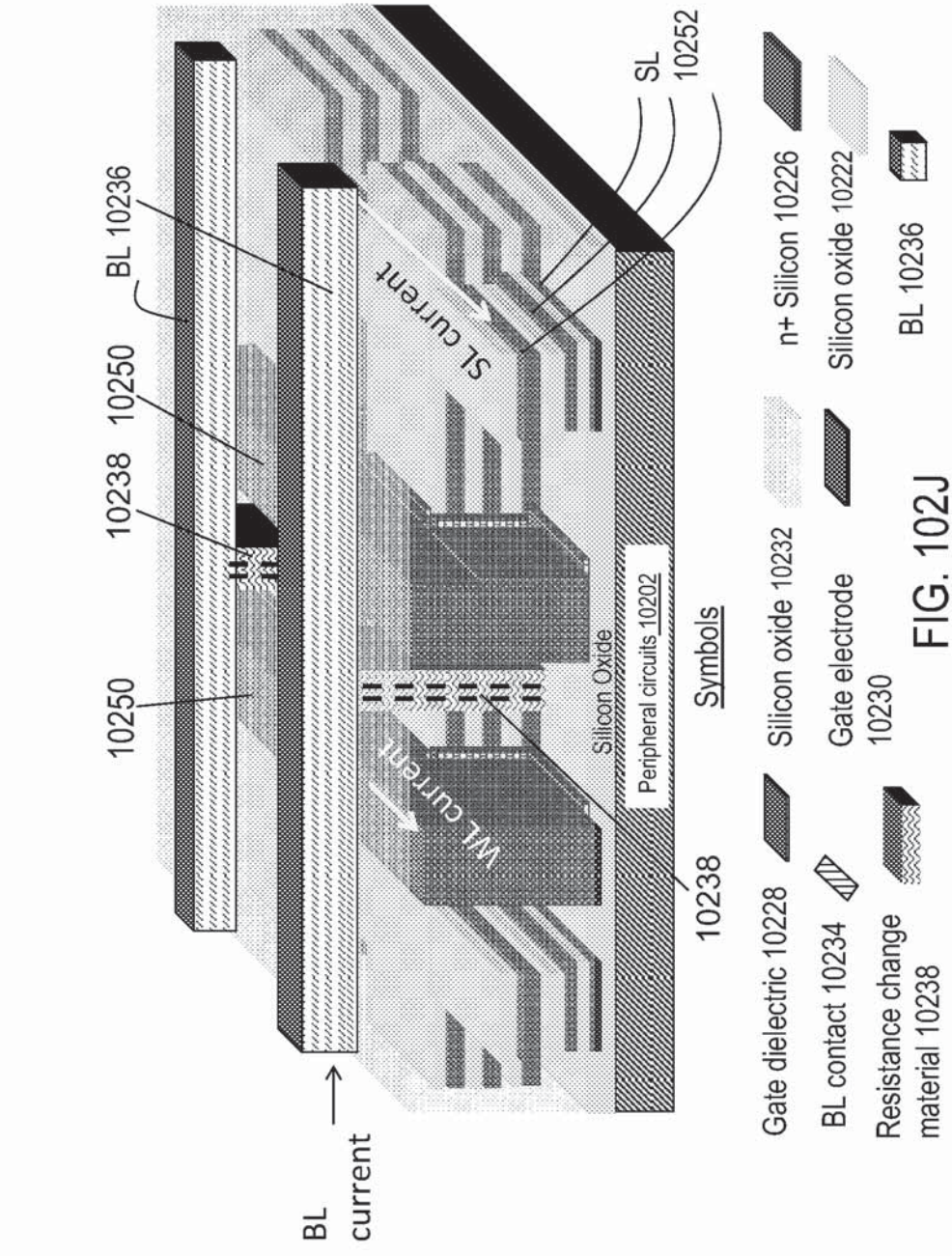

BL 10236
10250
10238
10250
SL
10252
SL current
WL current
Silicon Oxide
Peripheral circuits 10202
10238
BL current
Symbols
Gate dielectric 10228
Silicon oxide 10232
n+ Silicon 10226
BL contact 10234
Gate electrode 10230
Silicon oxide 10222
Resistance change material 10238
BL 10236

FIG. 102J

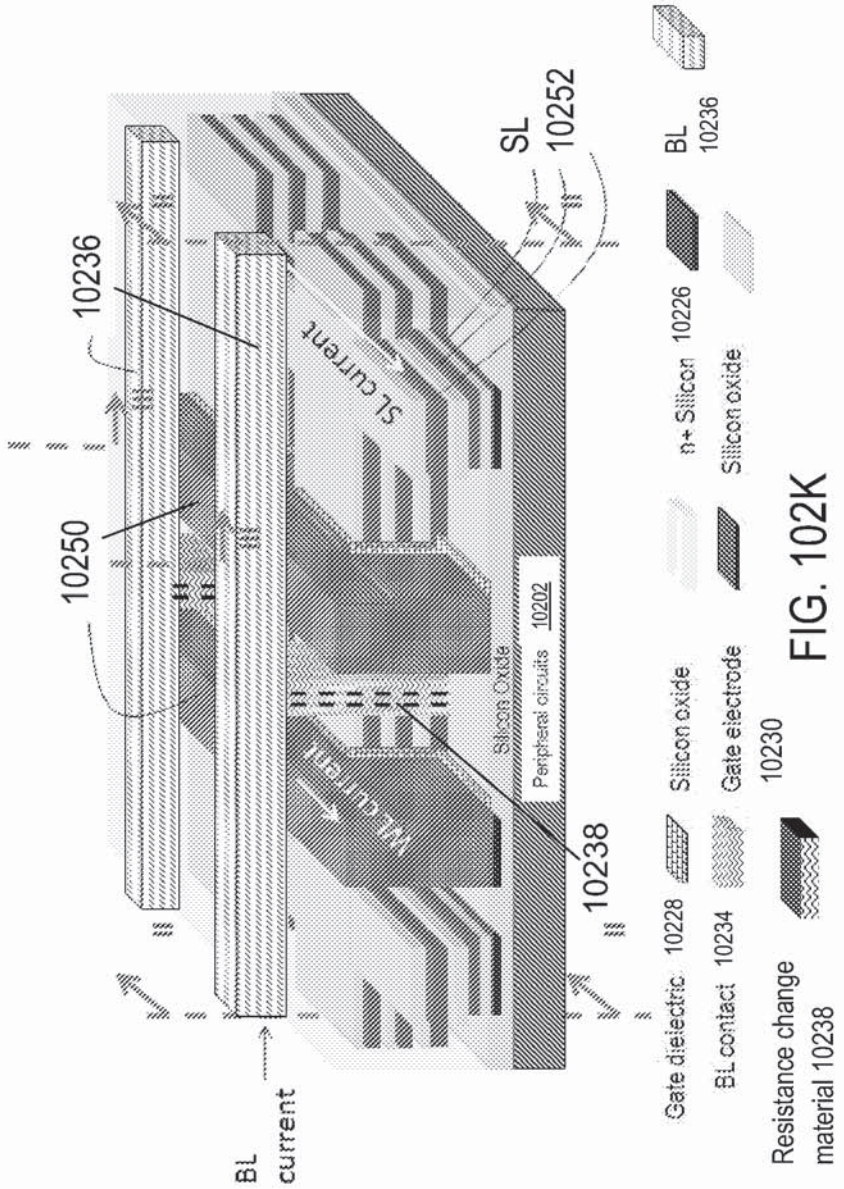

10236
10250
SL
10252
BL
10236
SL current
WL current
Silicon Oxide
Peripheral circuits 10202
10238
BL
current
n+ Silicon 10226
Silicon oxide
Gate dielectric 10228
Silicon oxide
BL contact 10234
Gate electrode
10230
Resistance change
material 10238

FIG. 102K

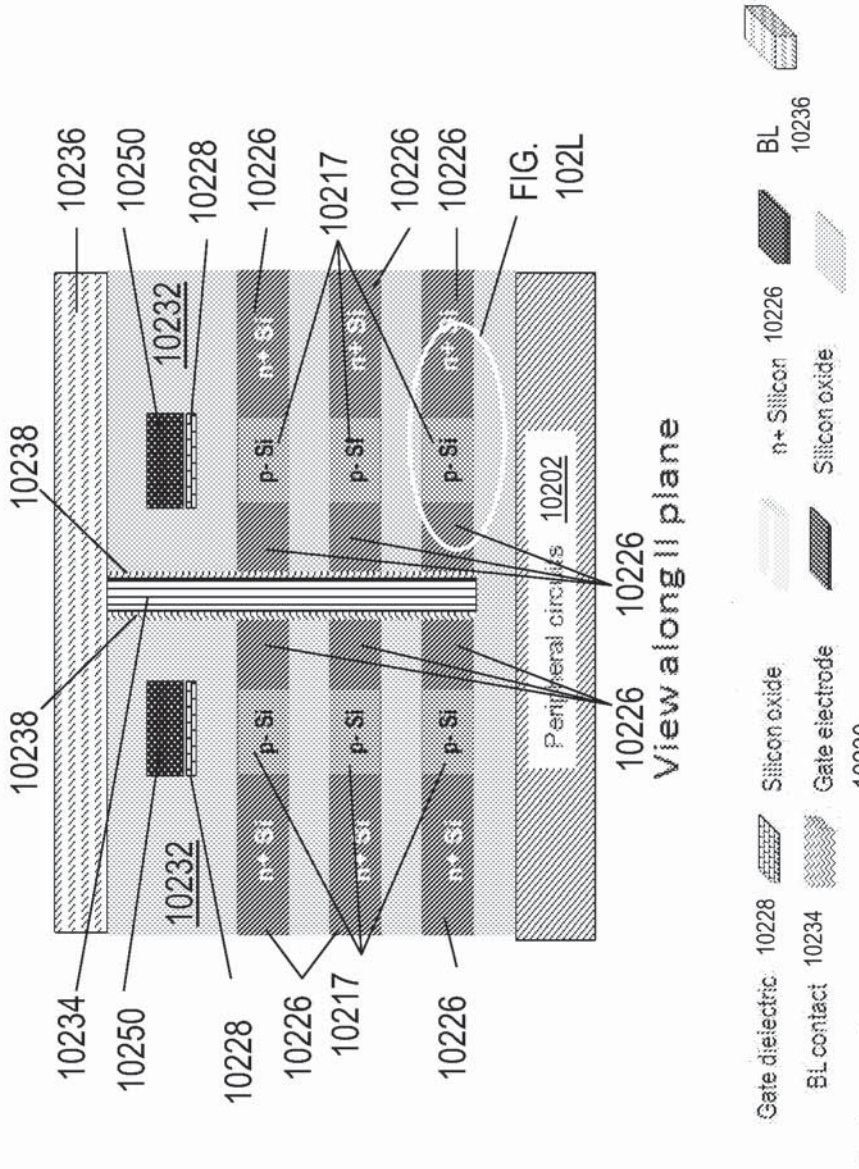

10236
10250
10228
10226
10217
10226
10226
FIG. 102L
10238
10232
p- Si
n+ Si
10234
10250
10228
10226
10217
10226
10238
10232
10226
10226
Peripheral circuits 10202
View along II plane
Gate dielectric 10228
Silicon oxide
n+ Silicon 10226
BL 10236
BL contact 10234
Gate electrode 10230
Silicon oxide
Resistance change material 10238

FIG. 102K1

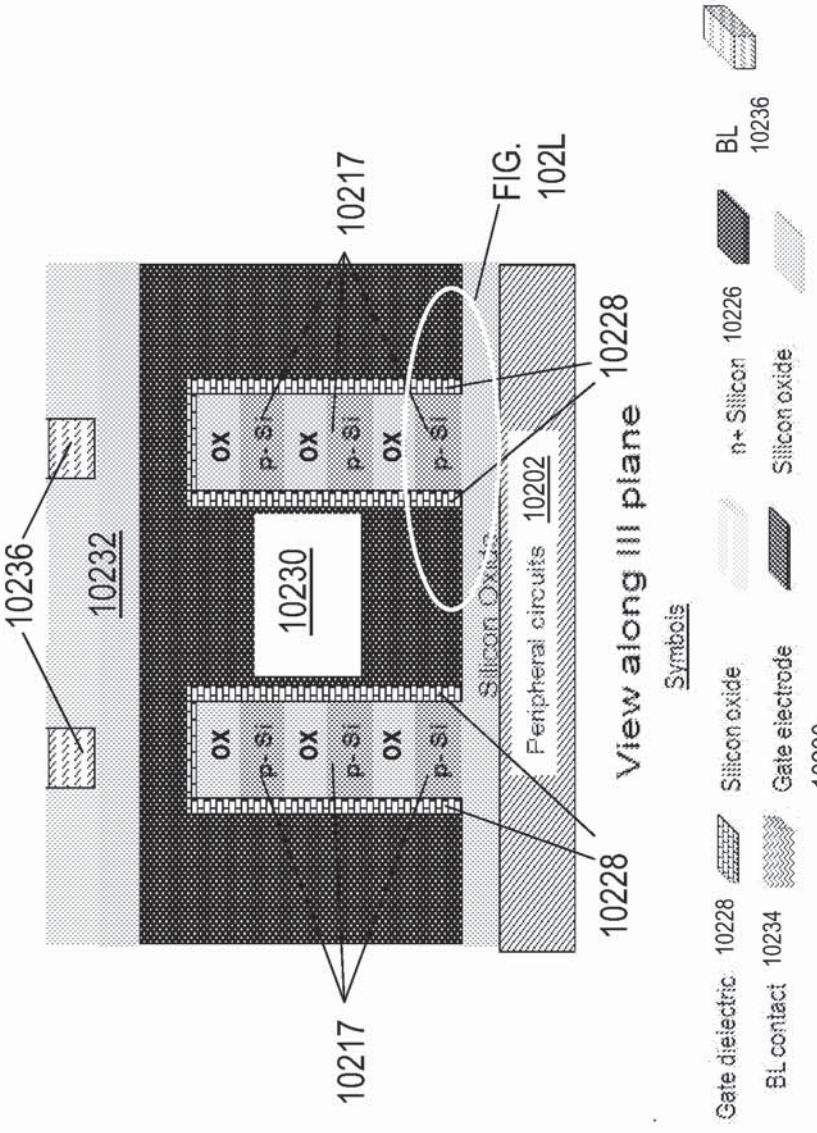

10236
10232
10230
10217
10217
FIG. 102L
10228
10228
View along III plane
Peripheral circuits 10202
Silicon Oxide
ox
p- Si
Symbols
Gate dielectric 10228
Silicon oxide
n+ Silicon 10226
BL 10236
BL contact 10234
Gate electrode 10230
Silicon oxide

FIG. 102K2

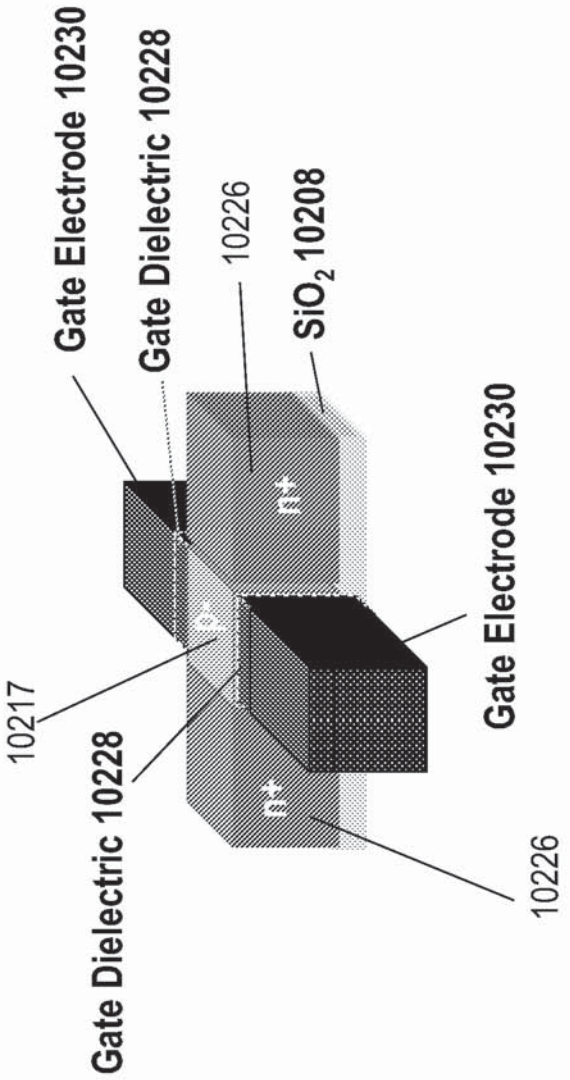

Gate Electrode 10230
Gate Dielectric 10228
10226
SiO_2 10208
n+
n+
10217
Gate Dielectric 10228
Gate Electrode 10230
10226

FIG. 102L


Silicon Oxide 10304
Peripheral circuits with W wiring 10302
10314

FIG. 103A

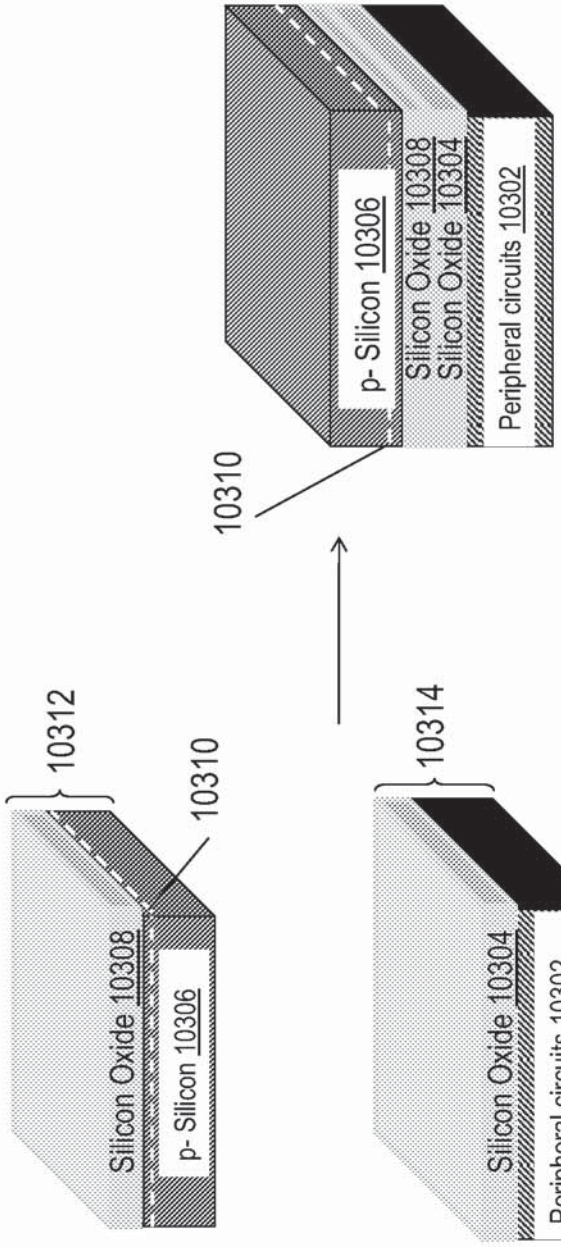

10312
10310
Silicon Oxide 10308
p- Silicon 10306
10310
p- Silicon 10306
Silicon Oxide 10308
Silicon Oxide 10304
Peripheral circuits 10302
10314
Silicon Oxide 10304
Peripheral circuits 10302

FIG. 103B

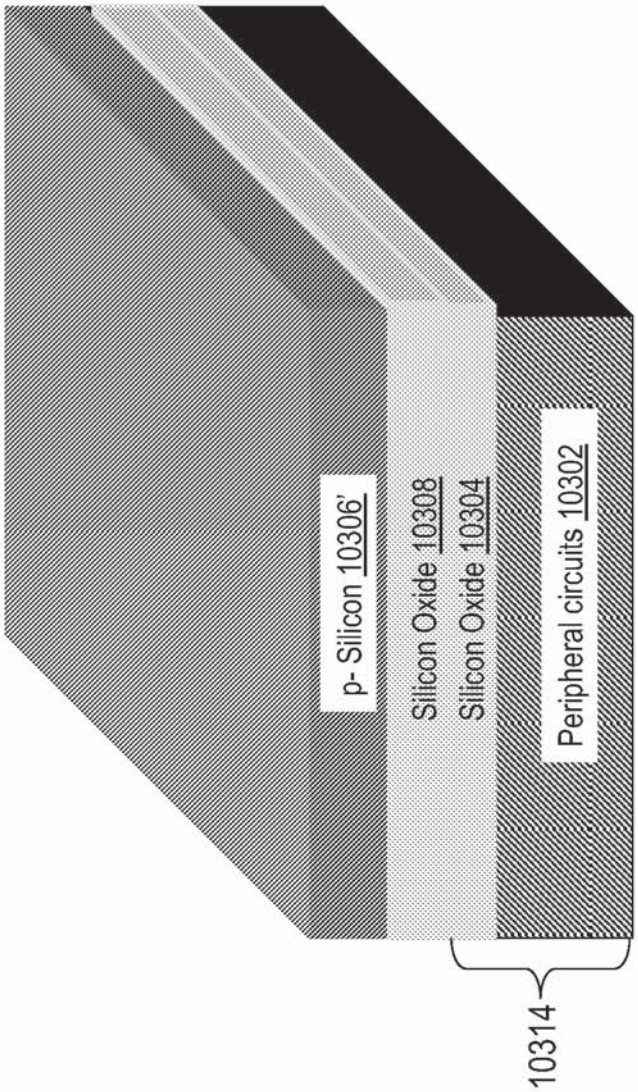

p- Silicon 10306'
Silicon Oxide 10308
Silicon Oxide 10304
Peripheral circuits 10302
10314

FIG. 103C

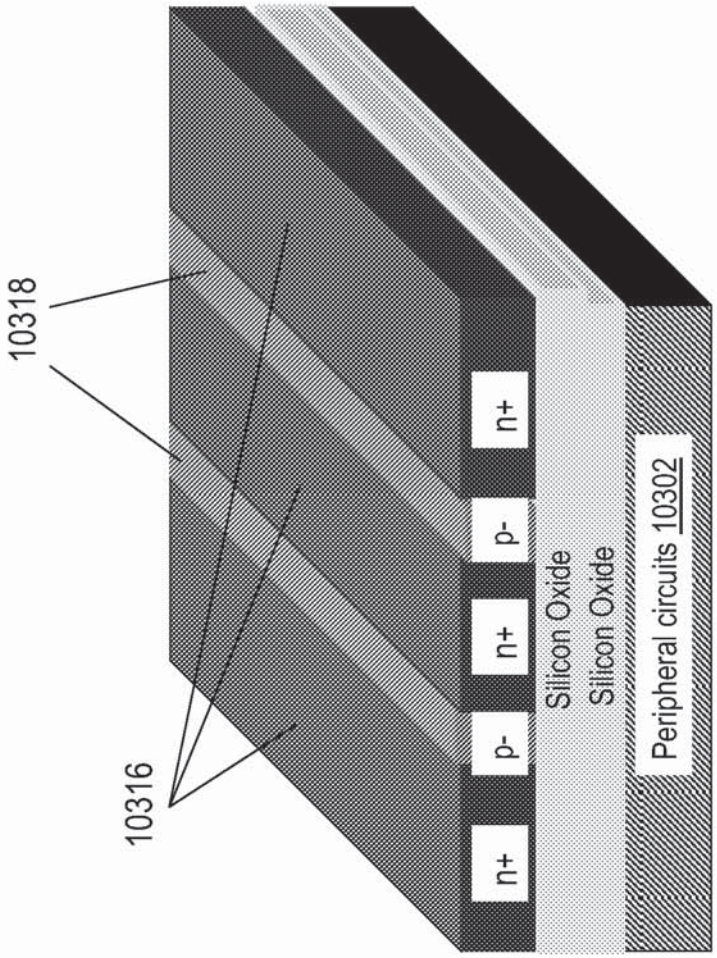

10318
10316
n+
p-
n+
p-
n+
Silicon Oxide
Silicon Oxide
Peripheral circuits 10302

FIG. 103D

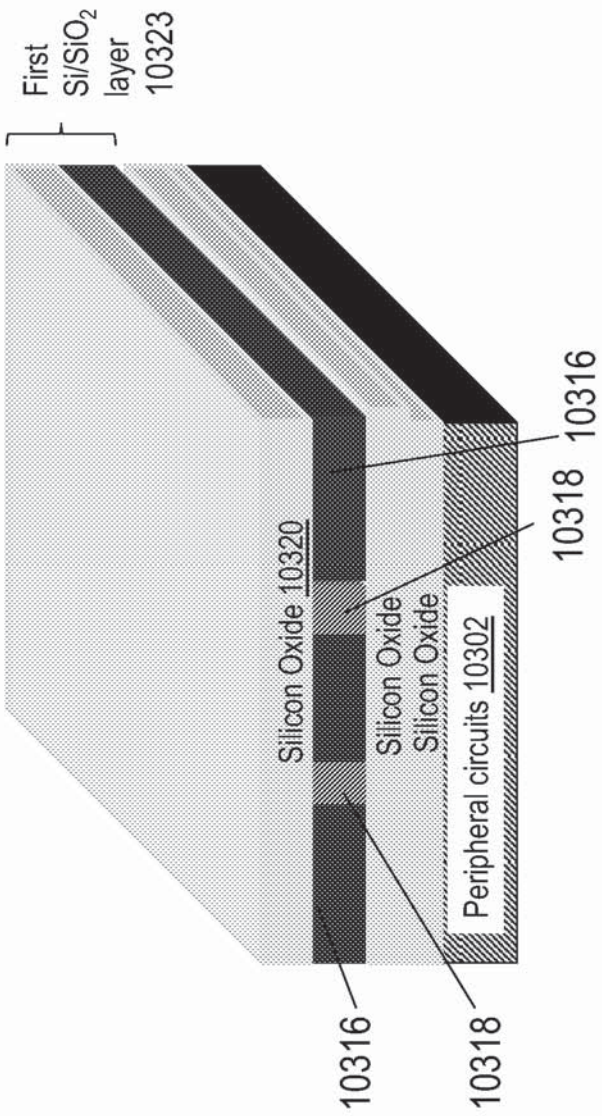

First
Si/SiO2
layer
10323
Silicon Oxide 10320
Silicon Oxide
Silicon Oxide
Peripheral circuits 10302
10316
10318
10316
10318

FIG. 103E

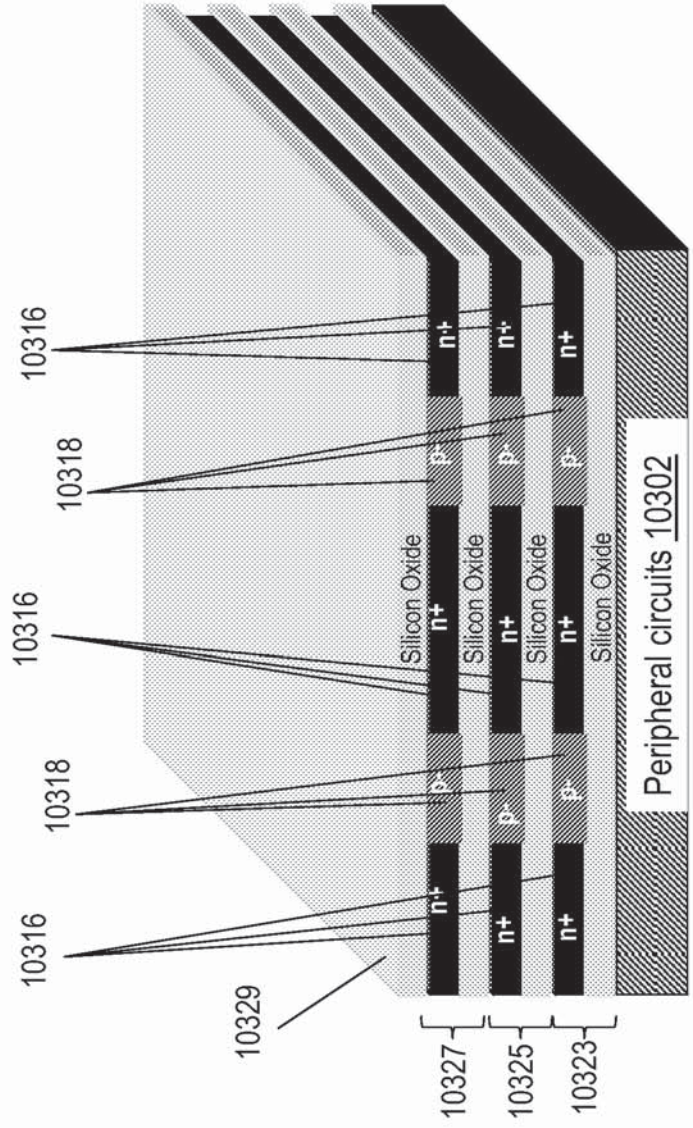

10316
10318
10316
10318
10316
10329
10327
10325
10323
Silicon Oxide
Silicon Oxide
Silicon Oxide
Silicon Oxide
n+
p-
Peripheral circuits 10302

FIG. 103F

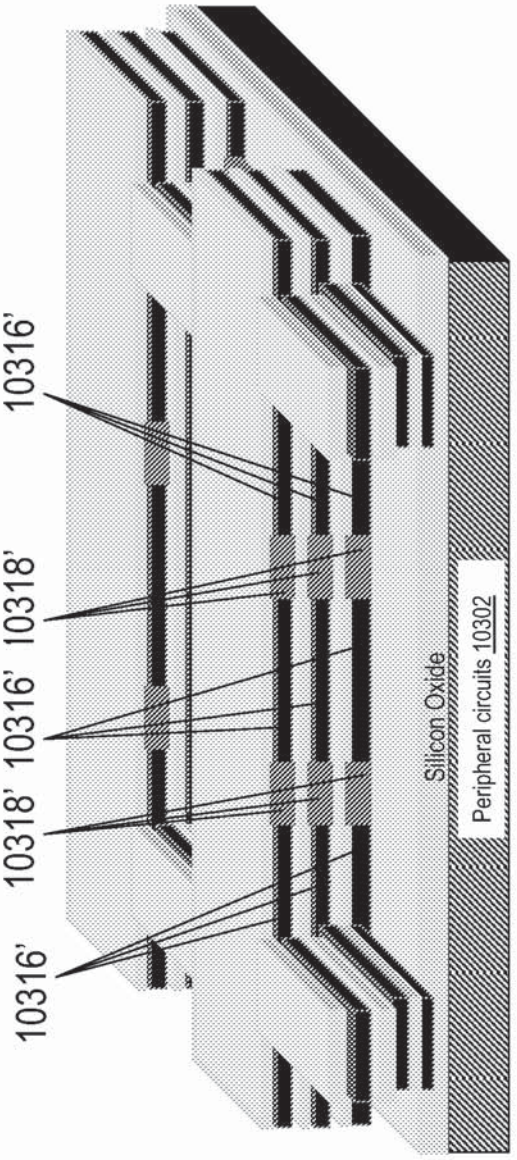

10316'
10318'
10316'
10318'
10316'
Silicon Oxide
Peripheral circuits 10302
Symbols
p- Silicon 10318'
Silicon oxide
n+ Silicon 10316'

FIG. 103G

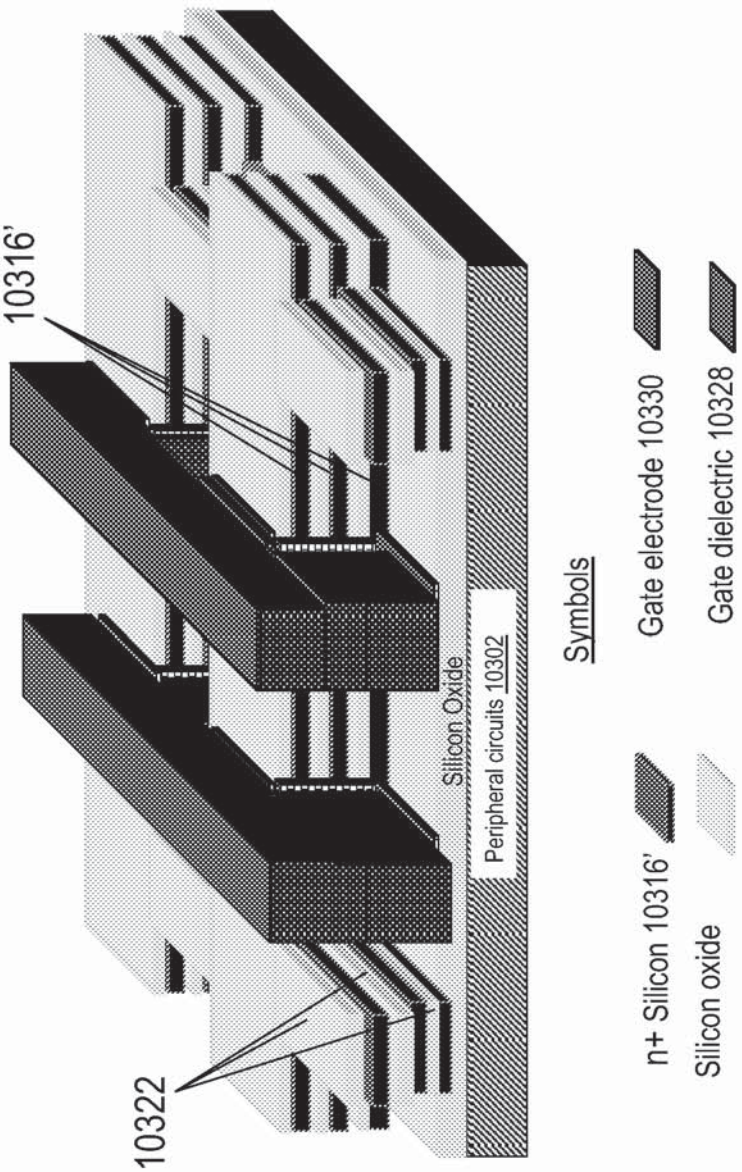

10316'
10322
Silicon Oxide
Peripheral circuits 10302
Symbols
n+ Silicon 10316'
Silicon oxide
Gate electrode 10330
Gate dielectric 10328

FIG. 103H

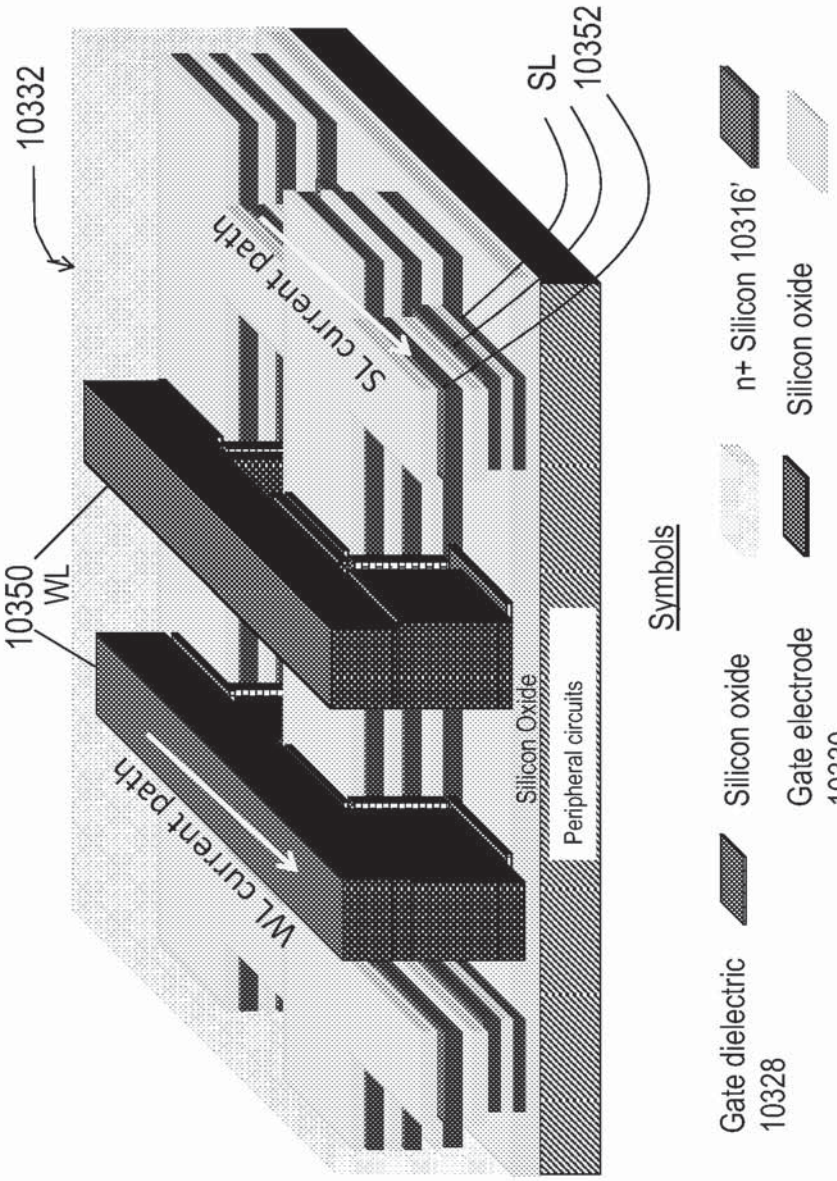

10332
SL
10352
SL current path
10350
WL
WL current path
Silicon Oxide
Peripheral circuits
Symbols
Gate dielectric
10328
Silicon oxide
Gate electrode
10330
n+ Silicon 10316'
Silicon oxide

FIG. 103I

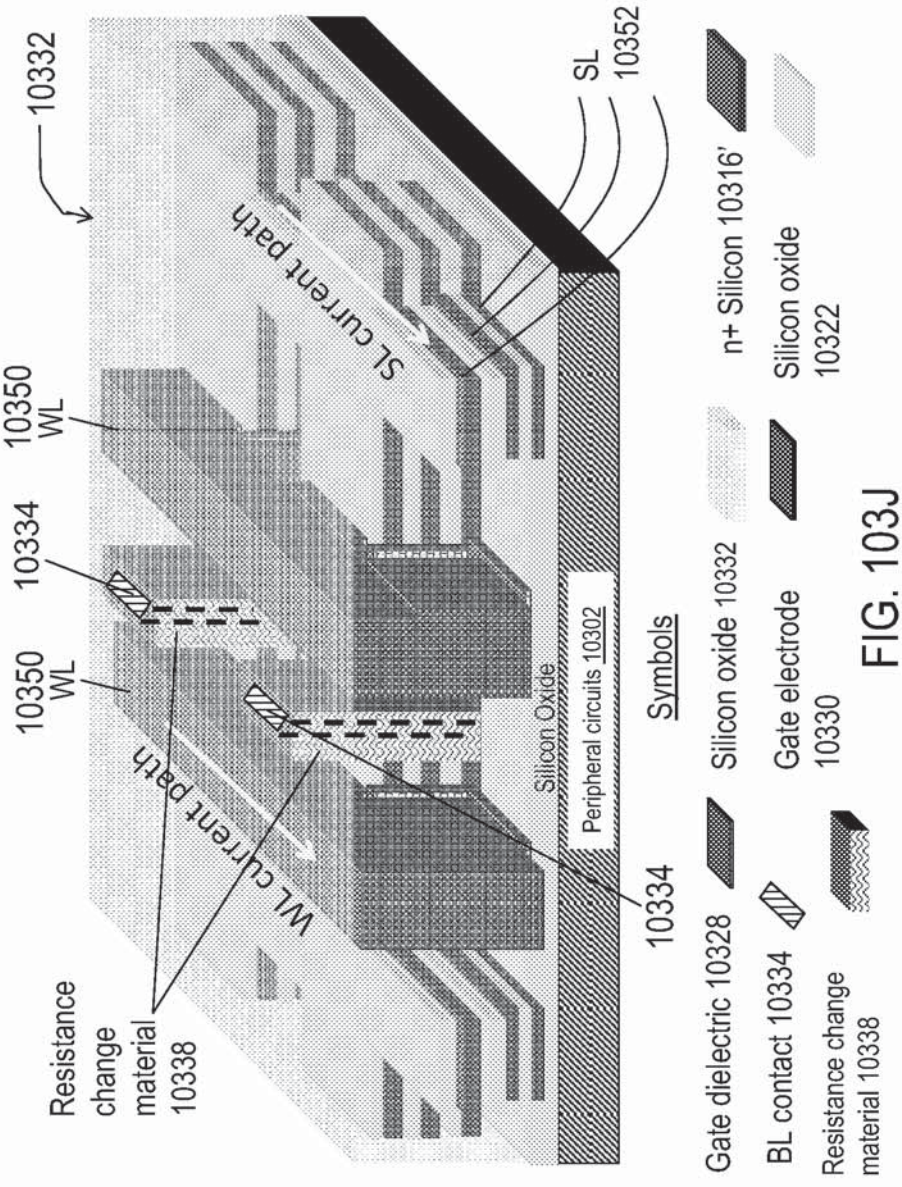

10332
SL
10352
SL current path
10350
WL
10334
10350
WL
WL current path
Resistance
change
material
10338
Silicon Oxide
Peripheral circuits 10302
10334
Symbols
Gate dielectric 10328
Silicon oxide 10332
n+ Silicon 10316'
BL contact 10334
Gate electrode
10330
Silicon oxide
10322
Resistance change
material 10338

FIG. 103J

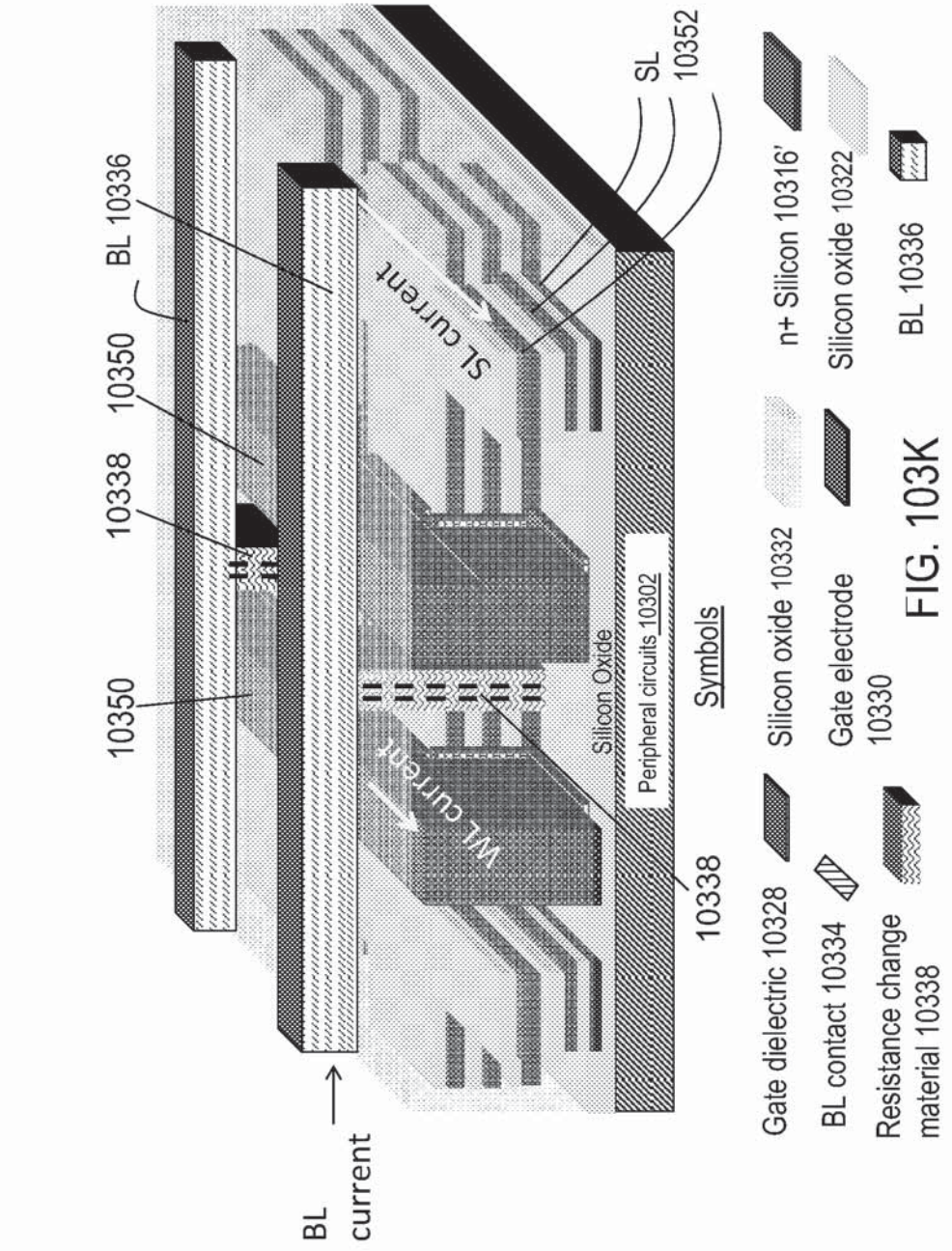

BL 10336
10350
10338
10350
SL
10352
SL current
WL current
Silicon Oxide
Peripheral circuits 10302
10338
BL current
Symbols
Gate dielectric 10328
Silicon oxide 10332
n+ Silicon 10316'
BL contact 10334
Gate electrode 10330
Silicon oxide 10322
Resistance change material 10338
BL 10336

FIG. 103K

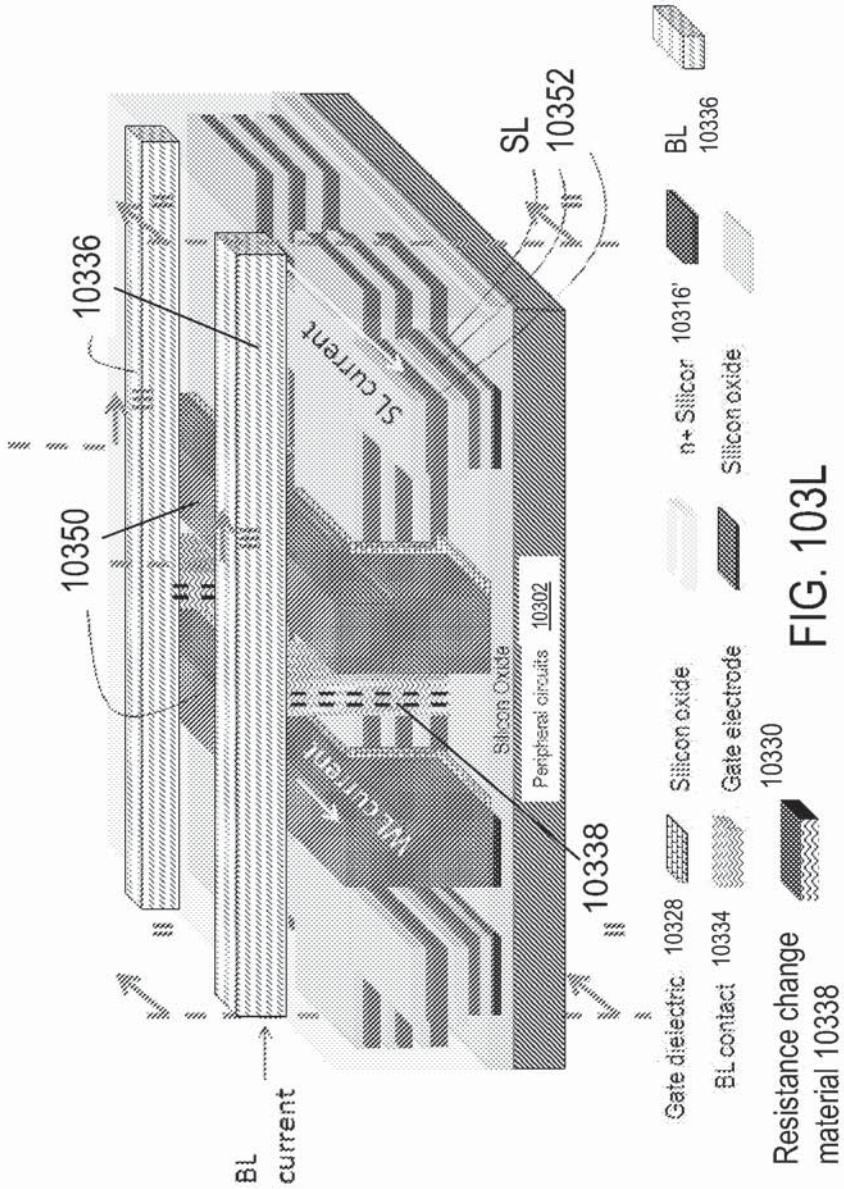

10336
10350
SL
10352
BL
10336
SL current
WL current
Silicon Oxide
Peripheral circuits 10302
10338
BL
current
n+ Silicon 10316'
Silicon oxide
Gate dielectric 10328
Silicon oxide
BL contact 10334
Gate electrode
10330
Resistance change
material 10338

FIG. 103L

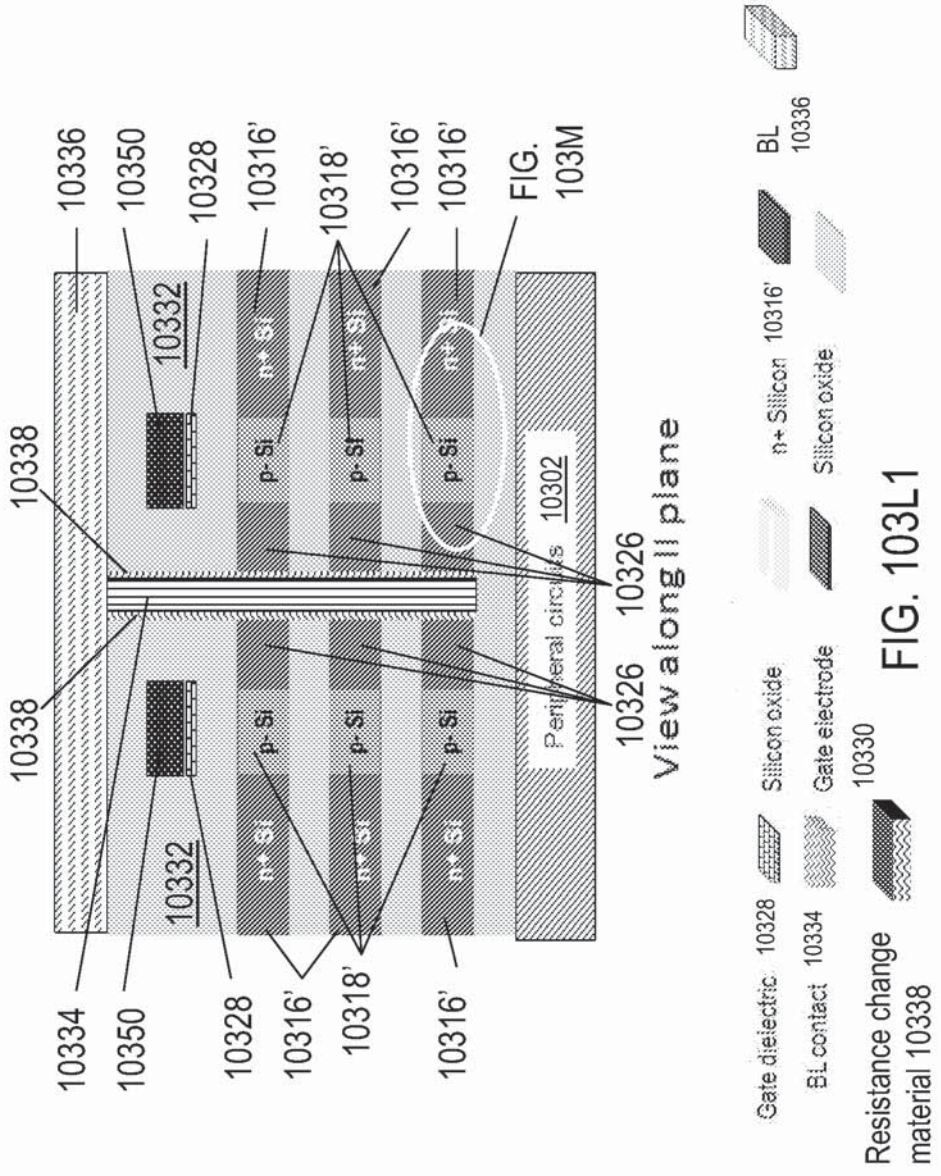

10336
10350
10328
10316'
10318'
10316'
10316'
FIG. 103M
10338
10332
10332
p- Si
n+ Si
10338
10334
10350
10328
10316'
10318'
10316'
Peripheral circuits 10302
10326
10326
View along II plane
Gate dielectric 10328
Silicon oxide
n+ Silicon 10316'
BL 10336
BL contact 10334
Gate electrode
Silicon oxide
10330
Resistance change material 10338

FIG. 103L1

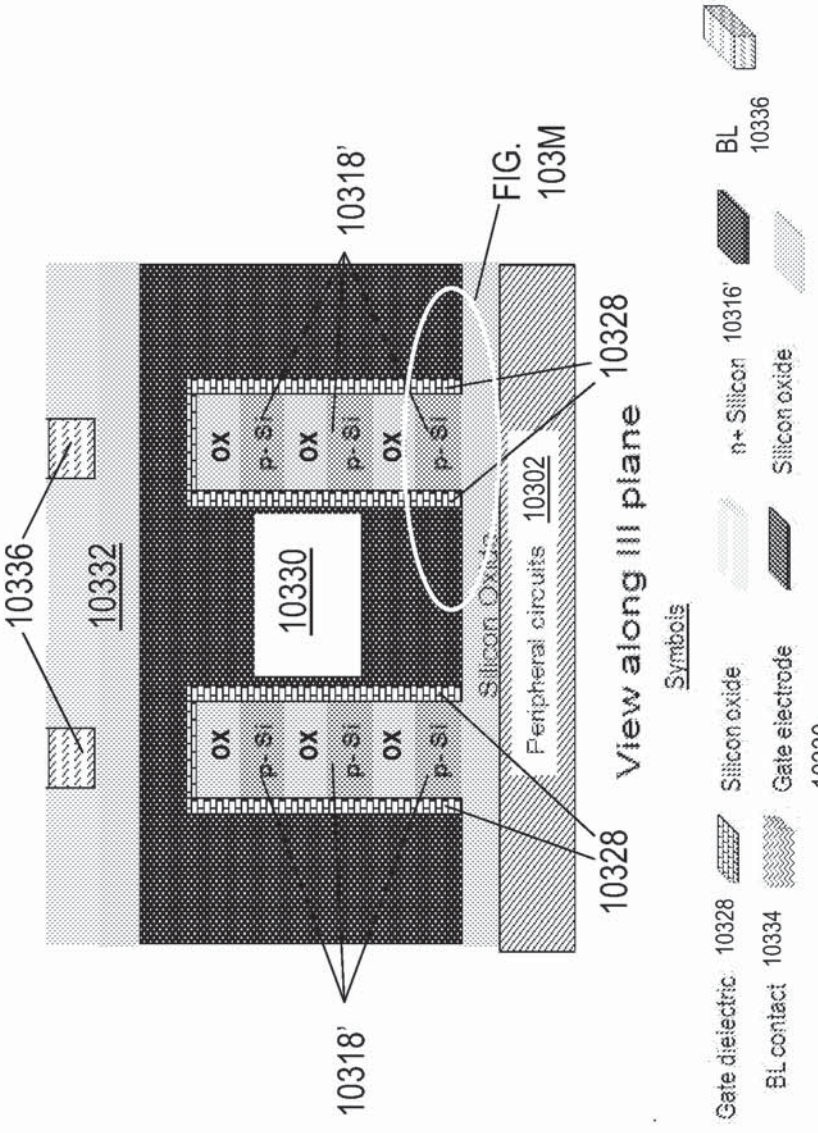

10336
10332
10330
10318'
10318'
FIG. 103M
10328
10328
View along III plane
Peripheral circuits 10302
Silicon Oxide
ox
p- Si
Symbols
Gate dielectric 10328
Silicon oxide
n+ Silicon 10316'
BL 10336
BL contact 10334
Gate electrode 10330
Silicon oxide

FIG. 103L2

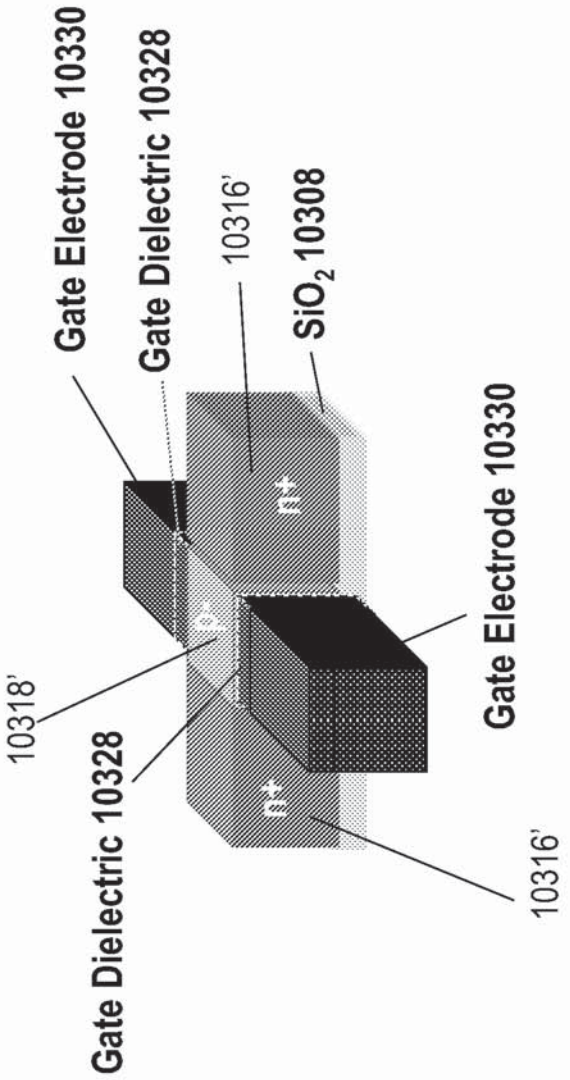

Gate Electrode 10330
Gate Dielectric 10328
10316'
SiO_2 10308
n+
n+
10318'
Gate Dielectric 10328
Gate Electrode 10330
10316'

FIG. 103M

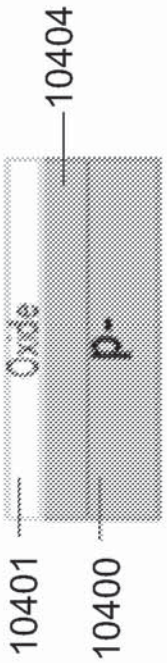


FIG. 104A

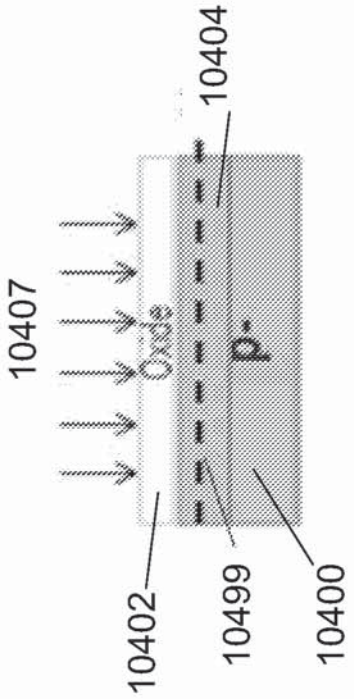


FIG. 104B

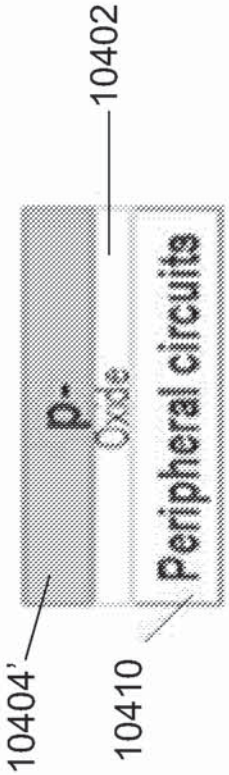


FIG. 104C

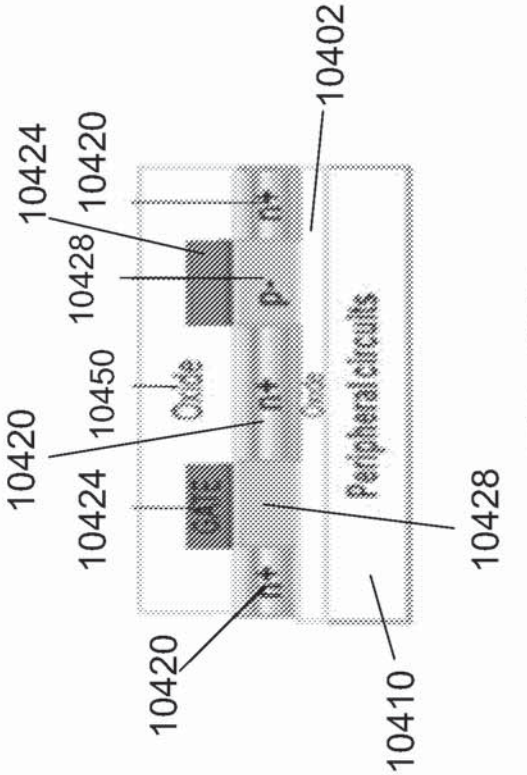

10402
10424
10420
10428
10450
10420
10424
10428
10420
10410
n+
p-
Oxide
Gate
Peripheralcircuits

FIG. 104D

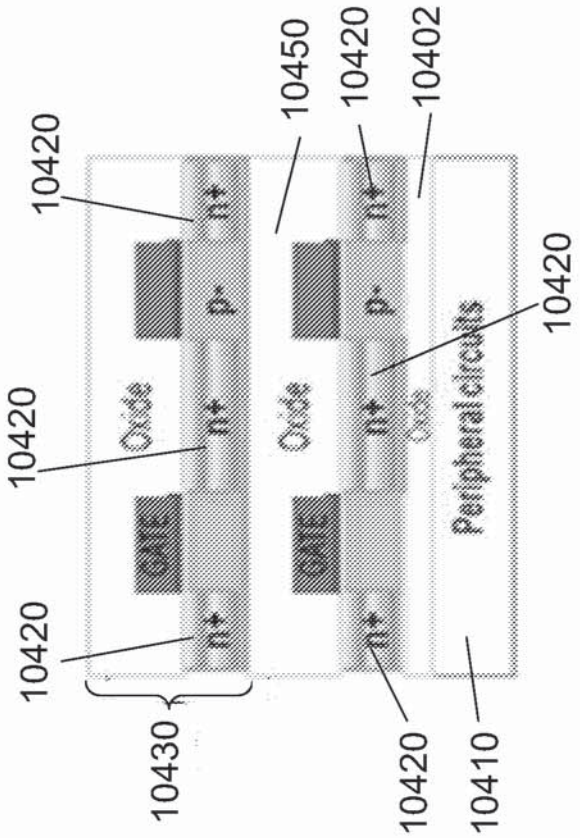

10420
10450
10420
10402
10420
n+
p-
n+
Oxide
Oxide
Oxide
GATE
GATE
Peripheral circuits
10420
10420
10420
10430
10420
10410

FIG. 104E

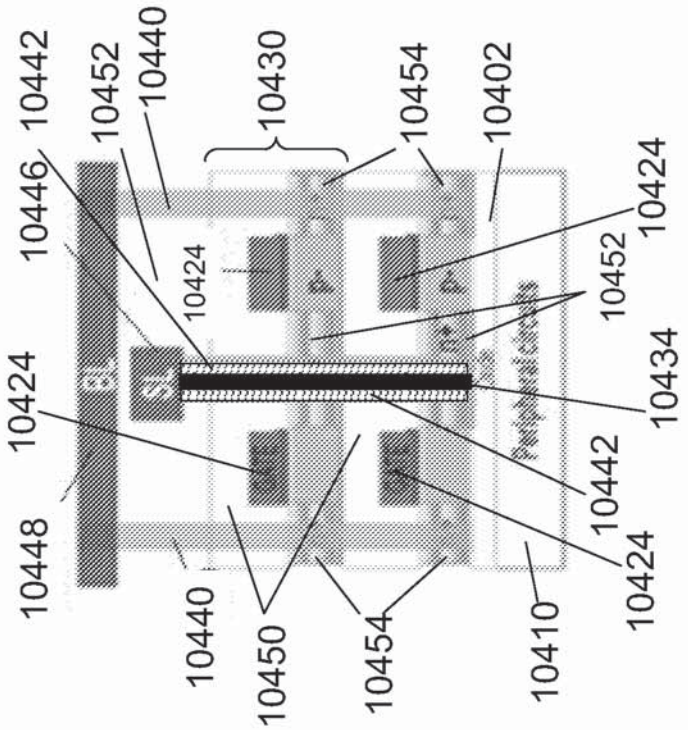

10442
10452
10440
10430
10454
10402
10446
10424
10424
10452
10424
10434
10424
10442
10448
10424
10440
10450
10454
10410

FIG. 104F

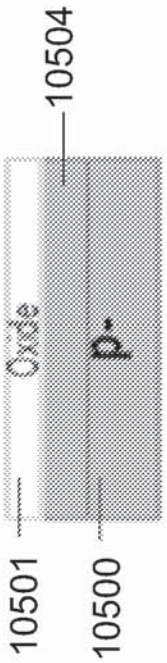


FIG. 105A

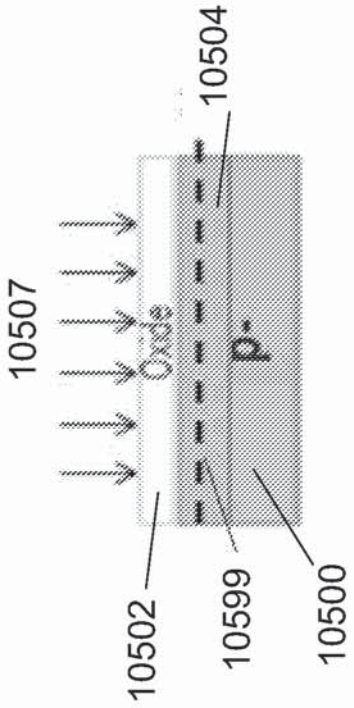


FIG. 105B

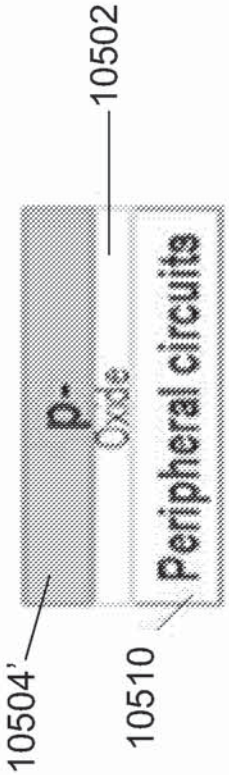


FIG. 105C

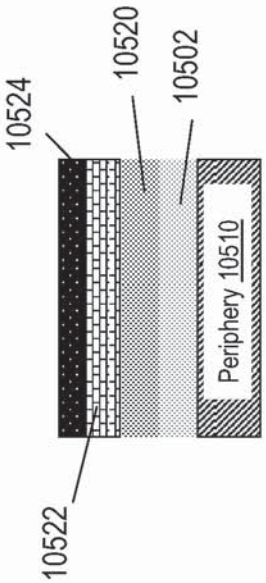


FIG. 105D

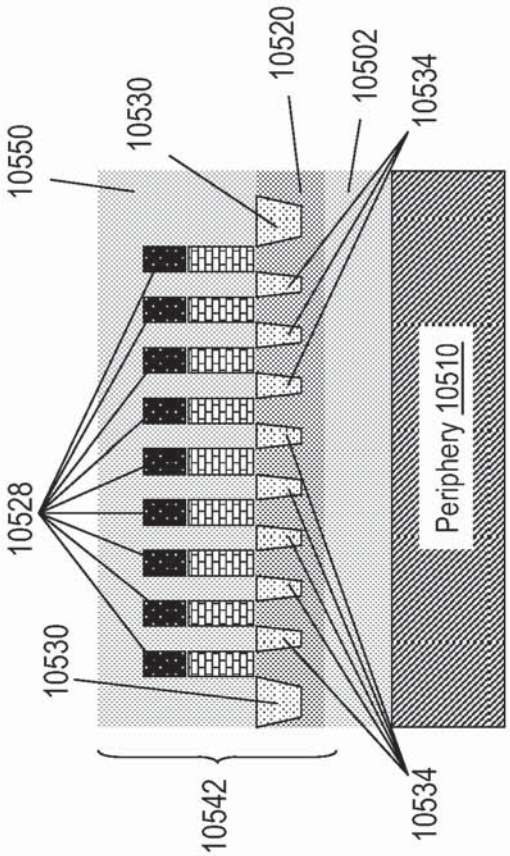

10550
10530
10520
10502
10534
10528
10530
Periphery 10510
10542
10534

FIG. 105E

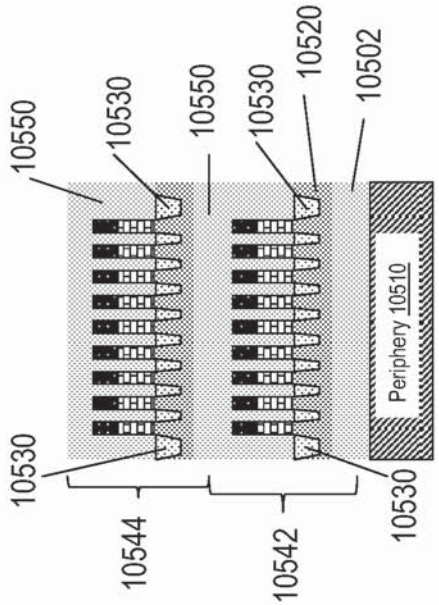

10550
10530
10550
10530
10520
10502
Periphery 10510
10530
10530
10544
10542

FIG. 105F

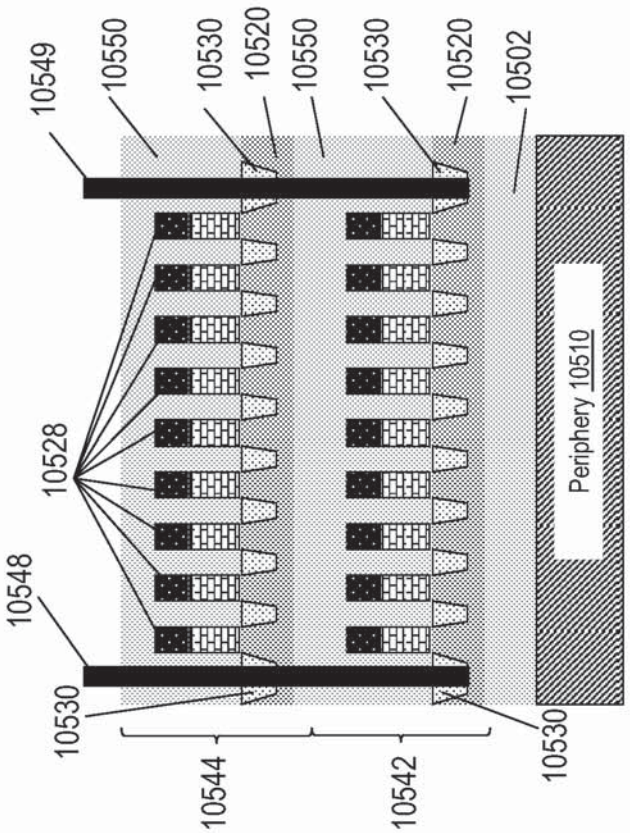

10549
10550
10530
10520
10550
10530
10520
10502
10528
10548
10530
10544
10542
10530
Periphery 10510

FIG. 105G


Silicon Oxide 10604
Peripheral circuits with W wiring 10602
10614

FIG. 106A

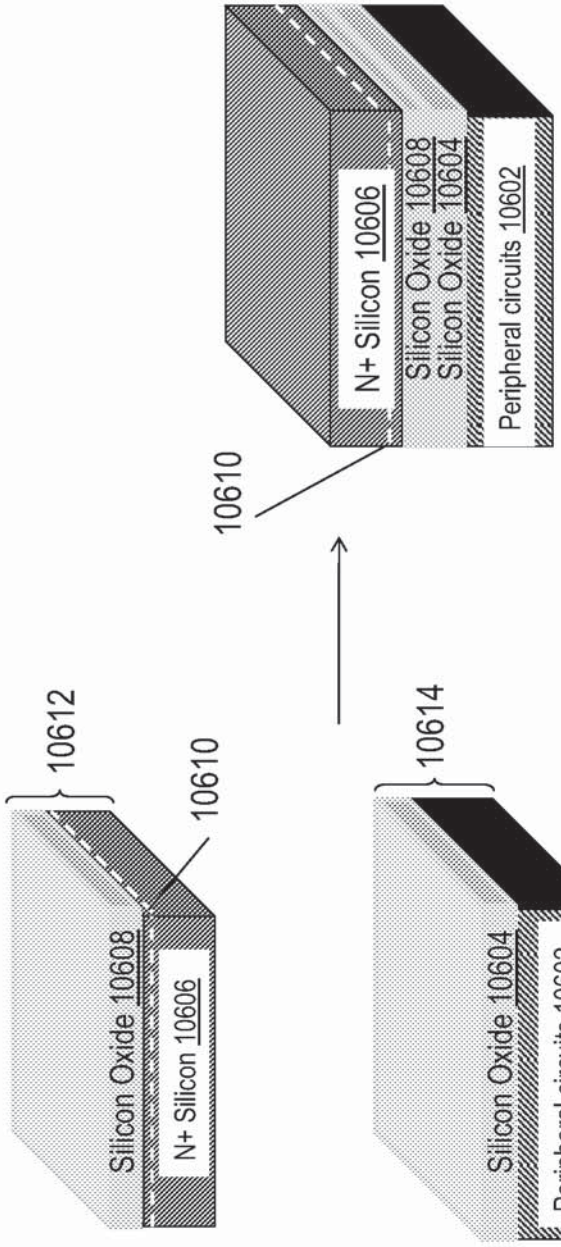

10612
10610
Silicon Oxide 10608
N+ Silicon 10606
10614
Silicon Oxide 10604
Peripheral circuits 10602
10610
N+ Silicon 10606
Silicon Oxide 10608
Silicon Oxide 10604
Peripheral circuits 10602

FIG. 106B

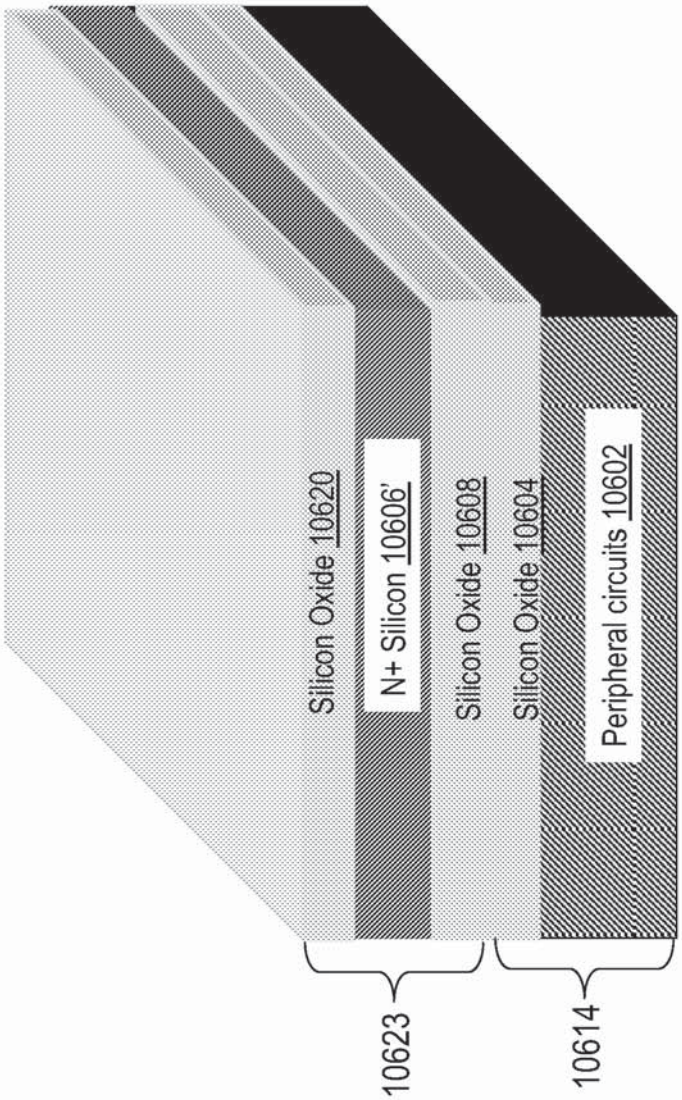

Silicon Oxide 10620
N+ Silicon 10606'
Silicon Oxide 10608
Silicon Oxide 10604
Peripheral circuits 10602
10623
10614

FIG. 106C

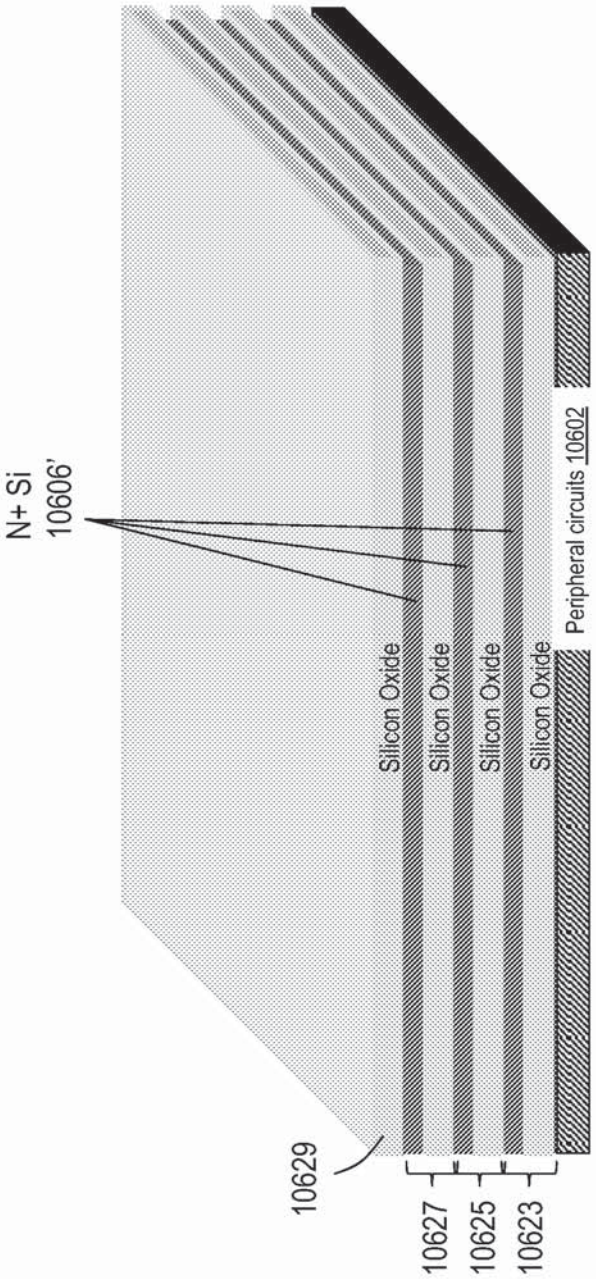

N+ Si
10606'
Silicon Oxide
Silicon Oxide
Silicon Oxide
Silicon Oxide
Peripheral circuits 10602
10629
10627
10625
10623

FIG. 106D

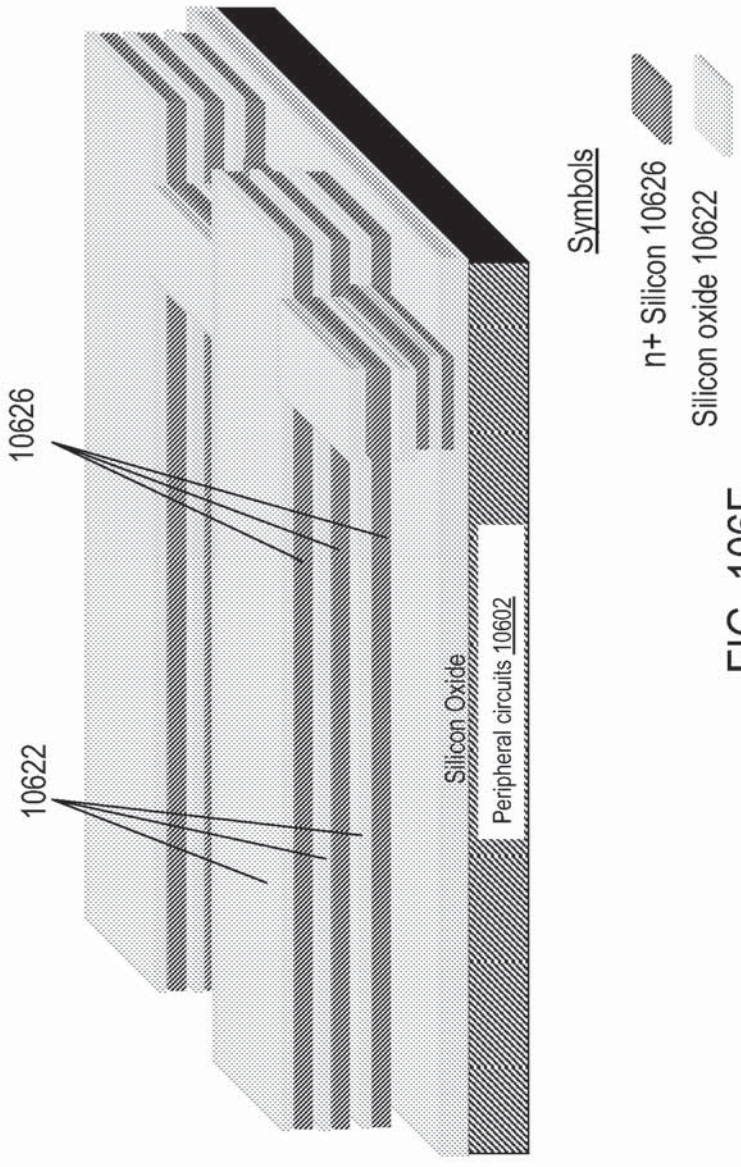

10626
10622
Silicon Oxide
Peripheral circuits 10602
Symbols
n+ Silicon 10626
Silicon oxide 10622

FIG. 106E

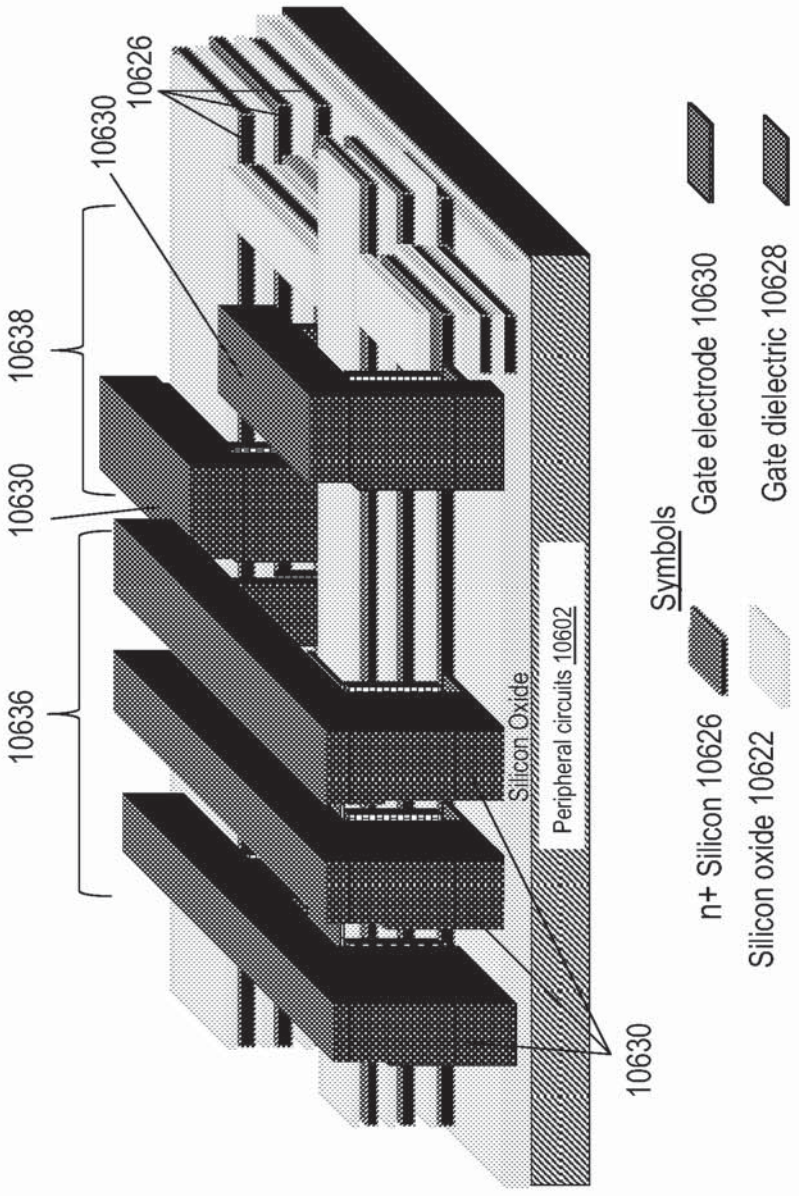

10626
10630
10638
10630
10636
10630
Silicon Oxide
Peripheral circuits 10602
Symbols
Gate electrode 10630
Gate dielectric 10628
n+ Silicon 10626
Silicon oxide 10622

FIG. 106F

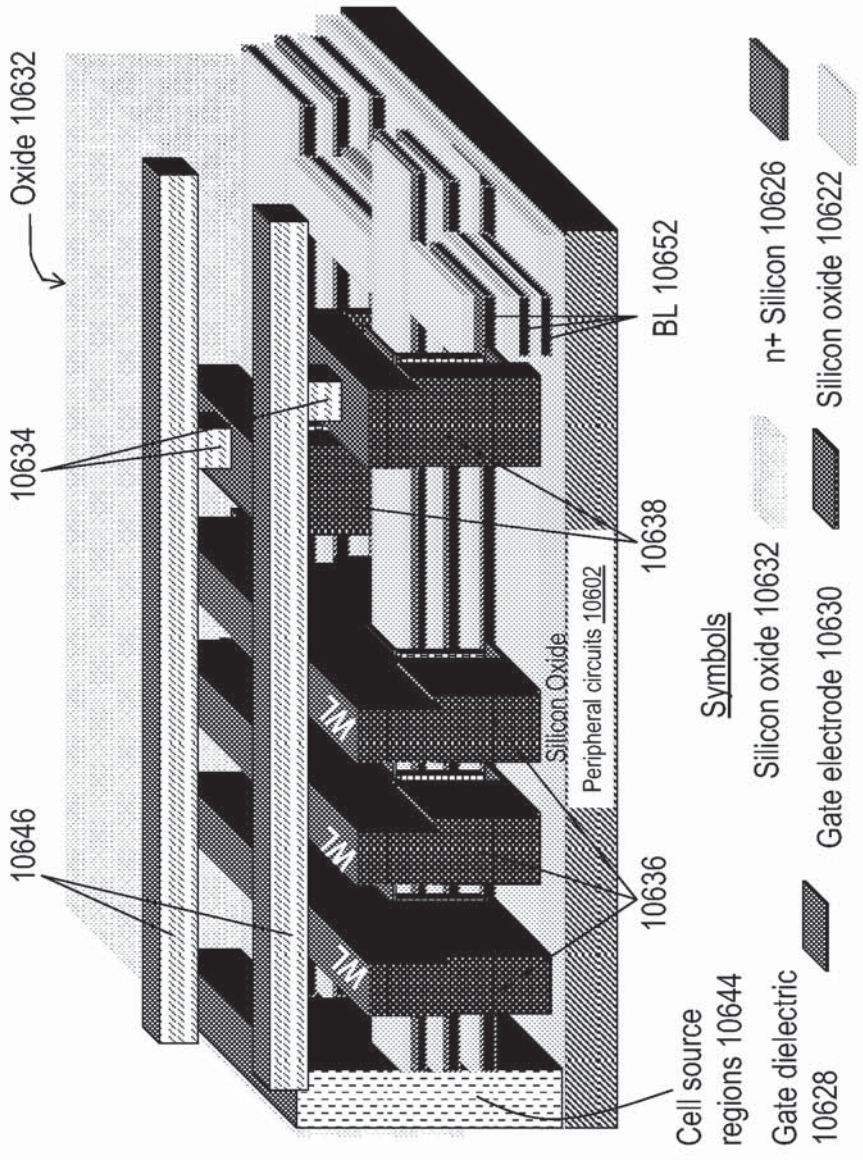

Oxide 10632
10634
10646
10636
10638
BL 10652
WL
WL
WL
Silicon Oxide
Peripheral circuits 10602
Cell source regions 10644
Gate dielectric 10628
Symbols
Silicon oxide 10632
Gate electrode 10630
n+ Silicon 10626
Silicon oxide 10622

FIG. 106G

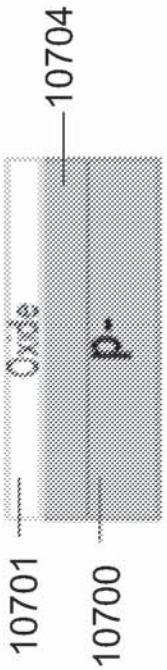


FIG. 107A

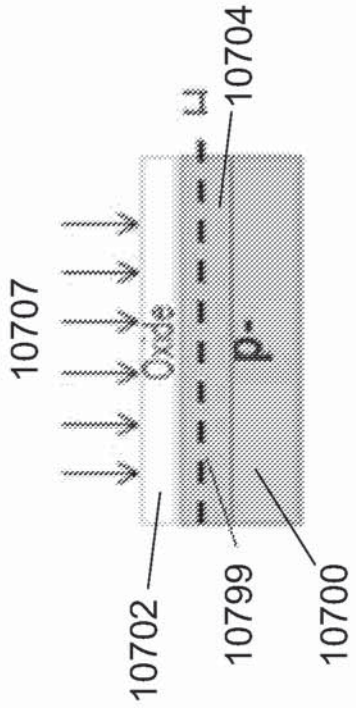


FIG. 107B

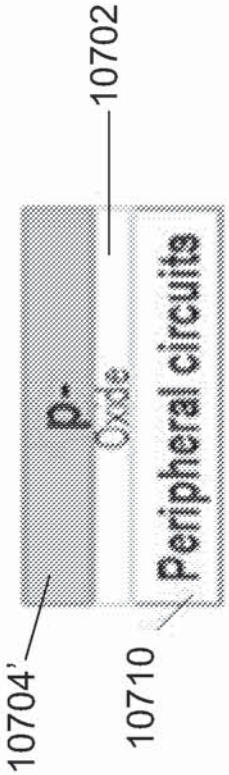


FIG. 107C

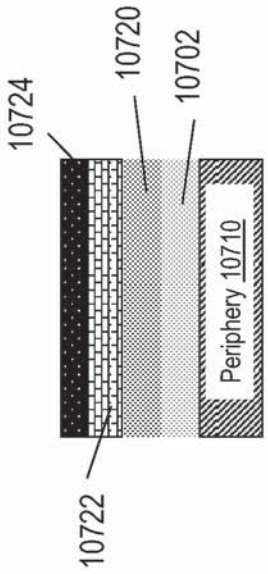


FIG. 107D

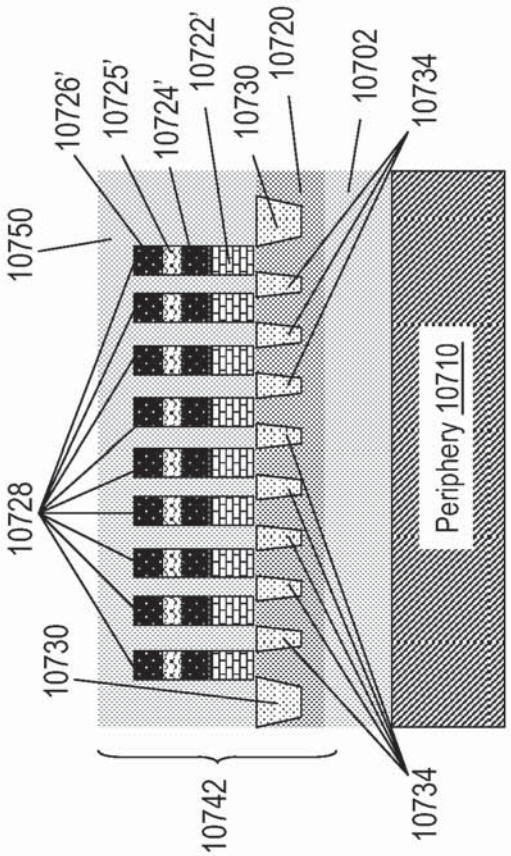

10750
10726'
10725'
10724'
10722'
10730
10720
10702
10734
10728
10730
Periphery 10710
10742
10734

FIG. 107E

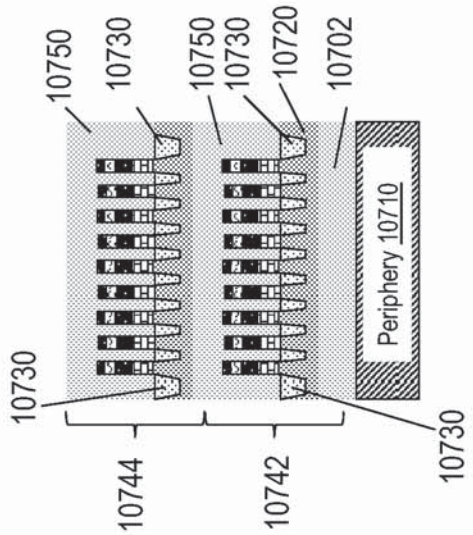

10750
10730
10750
10730
10720
10702
Periphery 10710
10730
10730
10744
10742

FIG. 107F

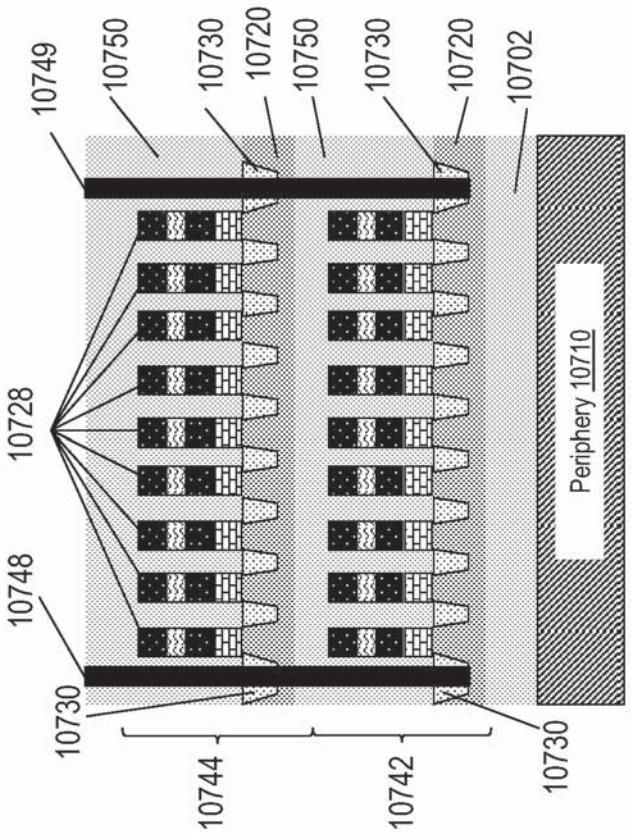

10749
10750
10730
10720
10750
10730
10720
10702
10728
10748
10730
10744
10742
10730
Periphery 10710

FIG. 107G


Silicon Oxide 10804
Peripheral circuits with W wiring 10802
10814

FIG. 108A

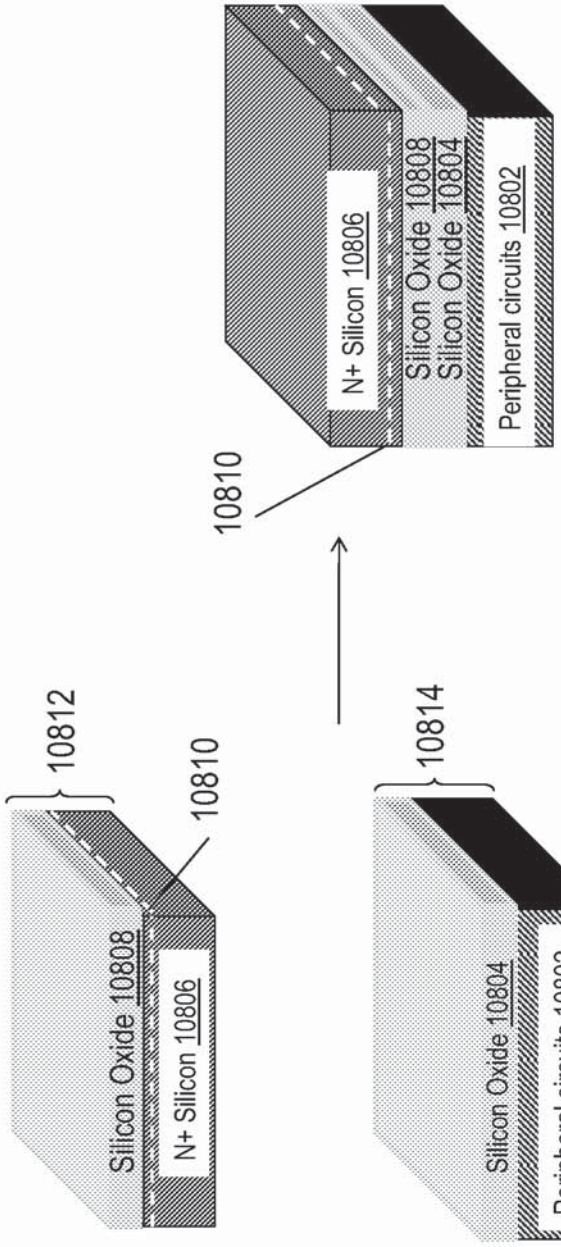

10812
10810
Silicon Oxide 10808
N+ Silicon 10806
10810
N+ Silicon 10806
Silicon Oxide 10808
Silicon Oxide 10804
Peripheral circuits 10802
10814
Silicon Oxide 10804
Peripheral circuits 10802

FIG. 108B

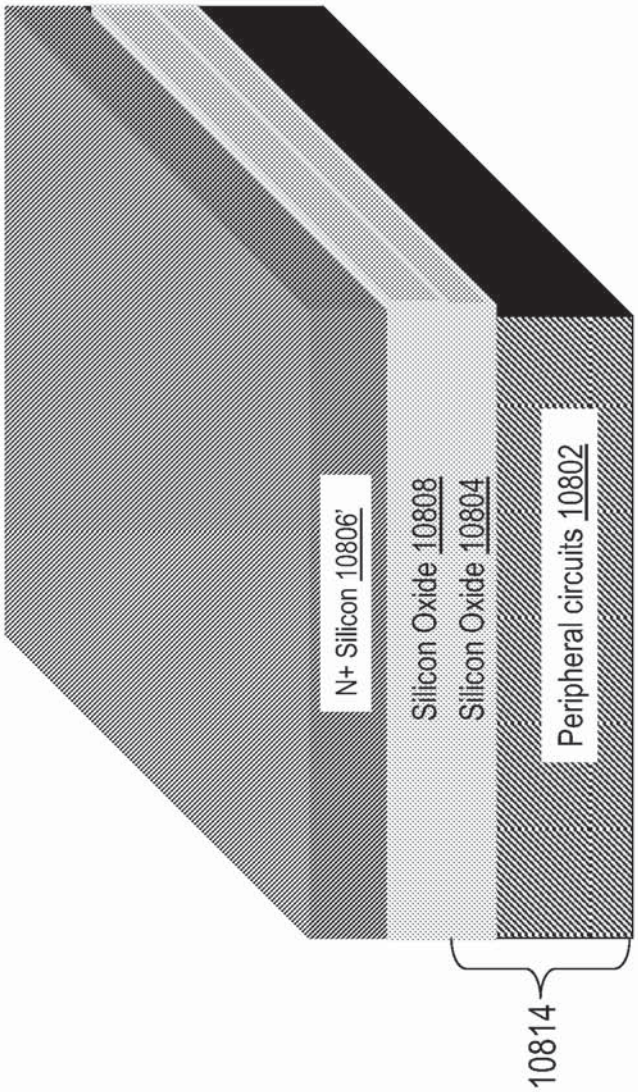

N+ Silicon 10806'
Silicon Oxide 10808
Silicon Oxide 10804
Peripheral circuits 10802
10814

FIG. 108C

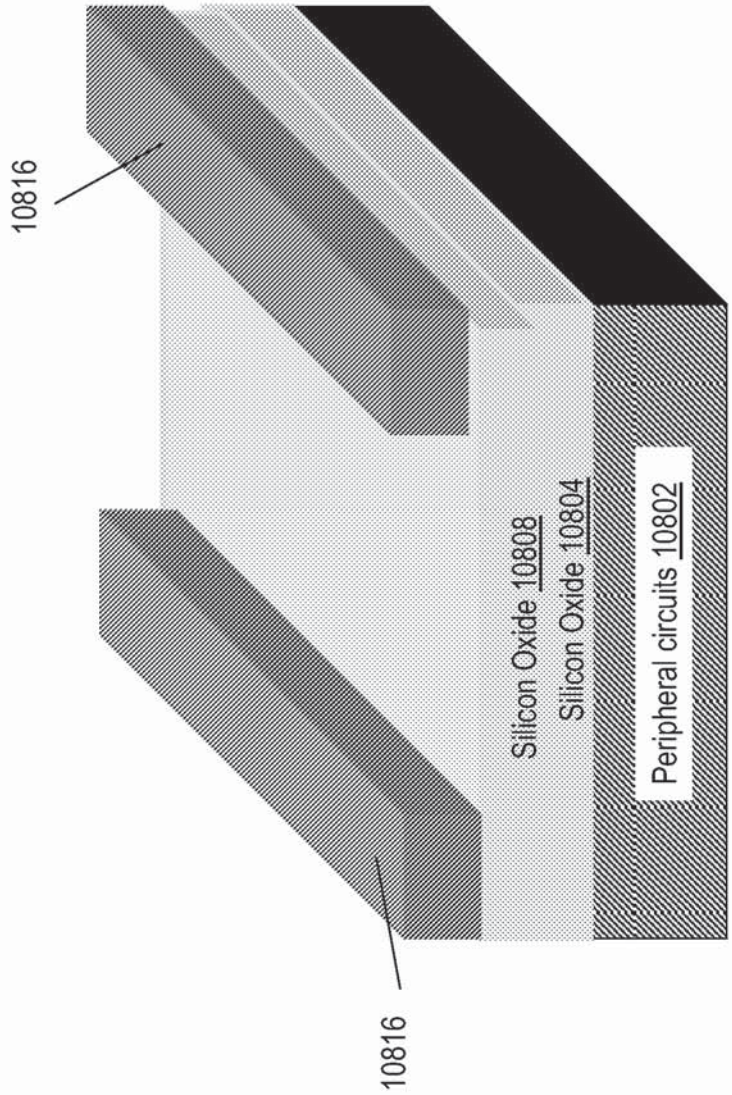

10816
Silicon Oxide 10808
Silicon Oxide 10804
Peripheral circuits 10802
10816

FIG. 108D

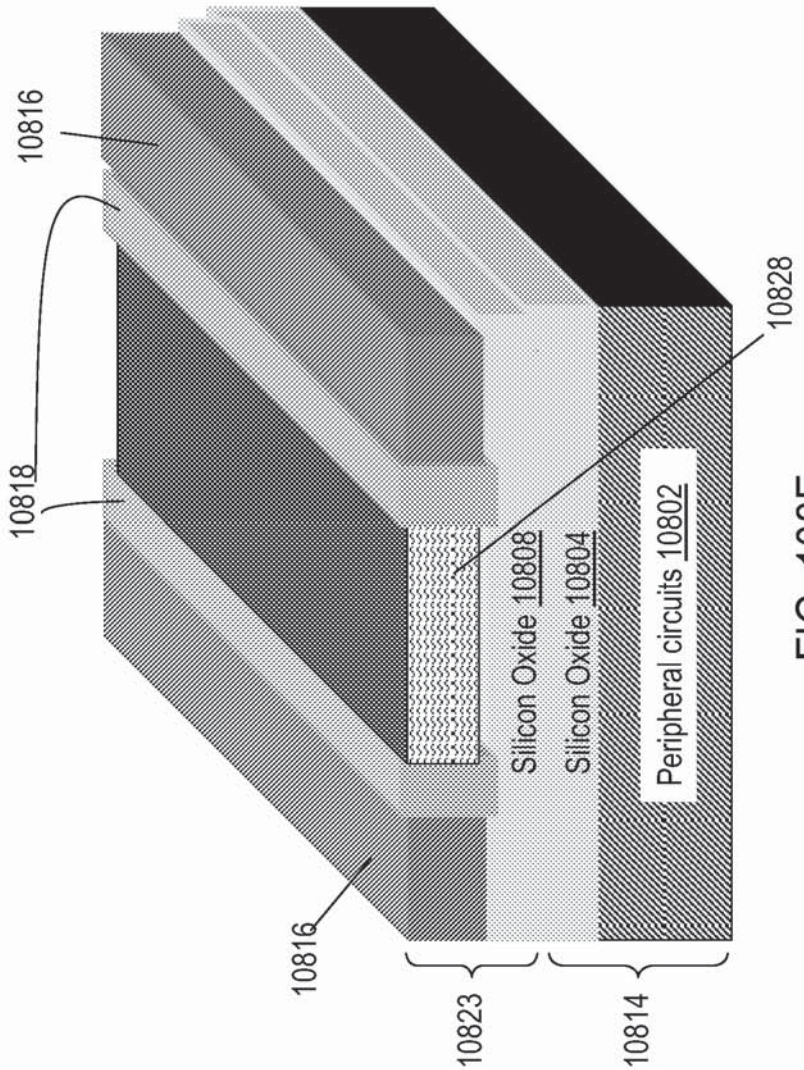

10816
10818
10816
10823
10814
Silicon Oxide 10808
Silicon Oxide 10804
Peripheral circuits 10802
10828

FIG. 108E

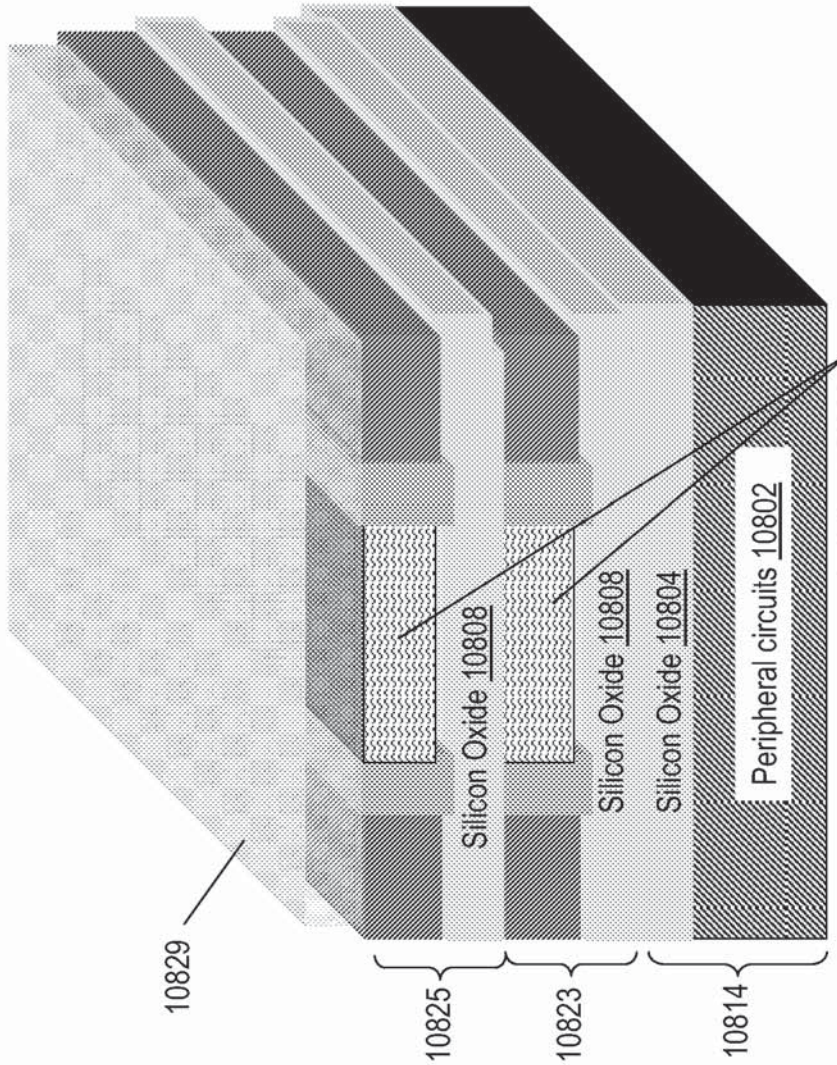

10829
10825
10823
10814
Silicon Oxide 10808
Silicon Oxide 10808
Silicon Oxide 10804
Peripheral circuits 10802
10828

FIG. 108F

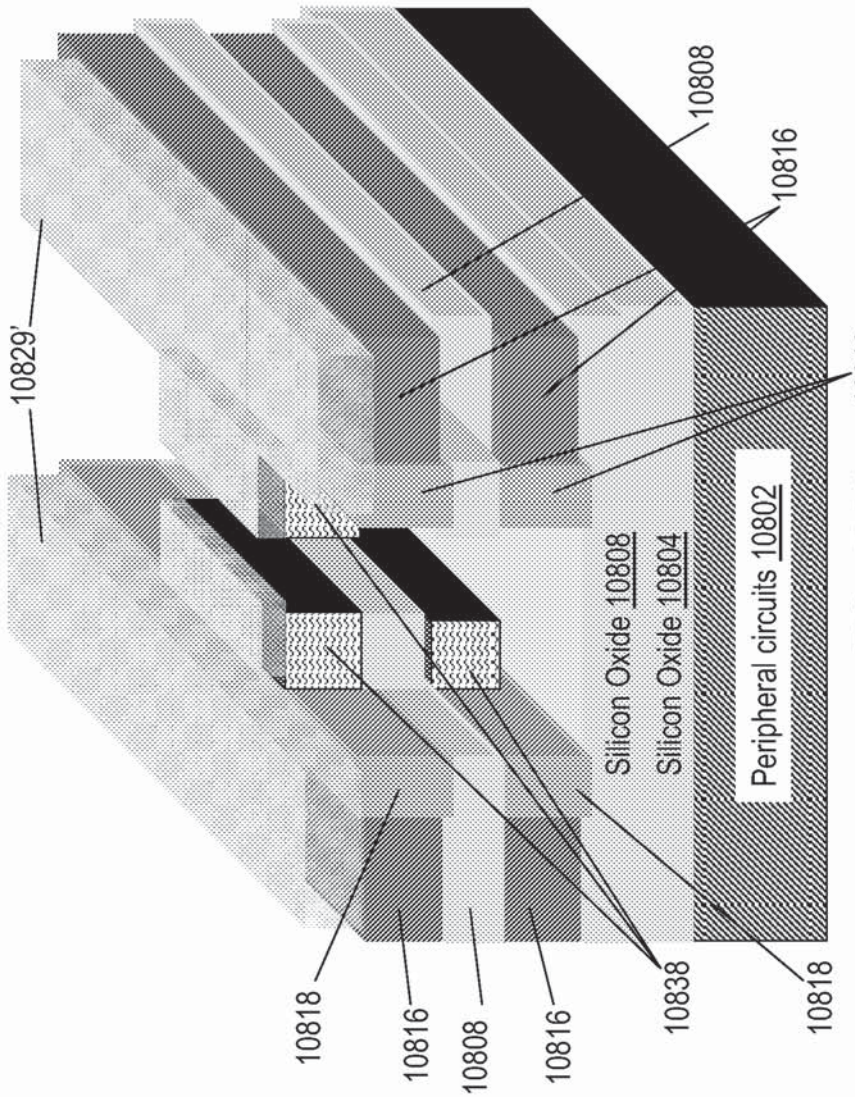

10829'
10808
10816
10818
Silicon Oxide 10808
Silicon Oxide 10804
Peripheral circuits 10802
10818
10816
10808
10816
10838
10818

FIG. 108G

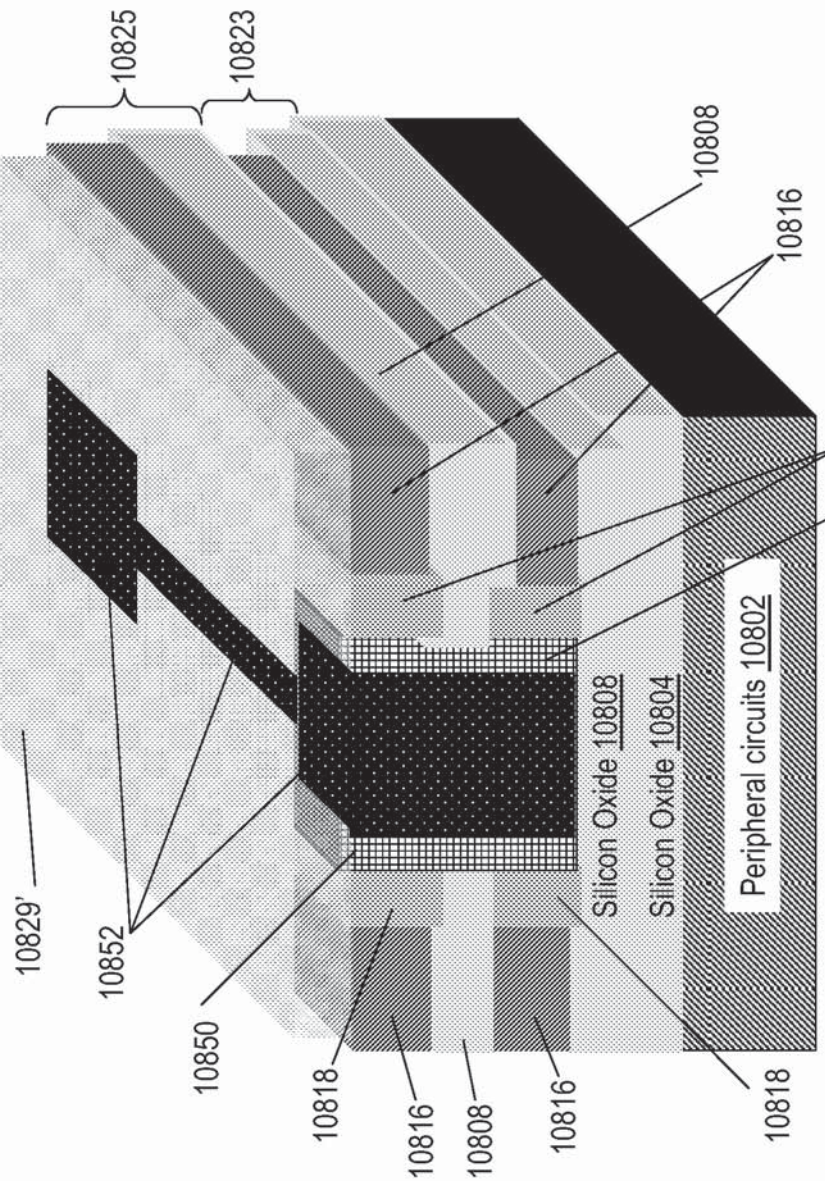

10825
10823
10808
10816
10818
10850
10852
10829'
Silicon Oxide 10808
Silicon Oxide 10804
Peripheral circuits 10802

FIG. 108H

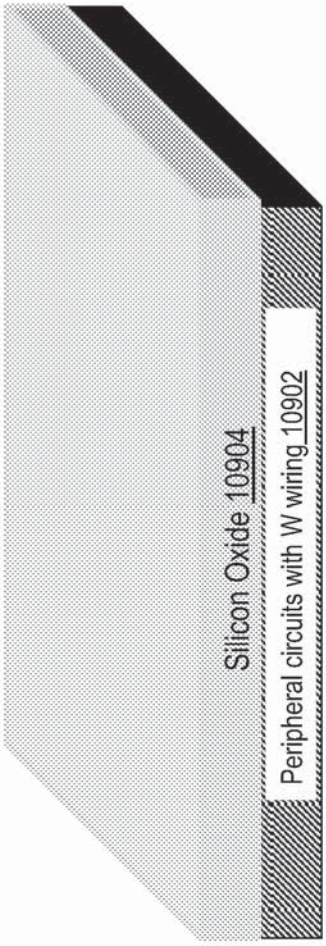

Silicon Oxide 10904
Peripheral circuits with W wiring 10902

FIG. 109A

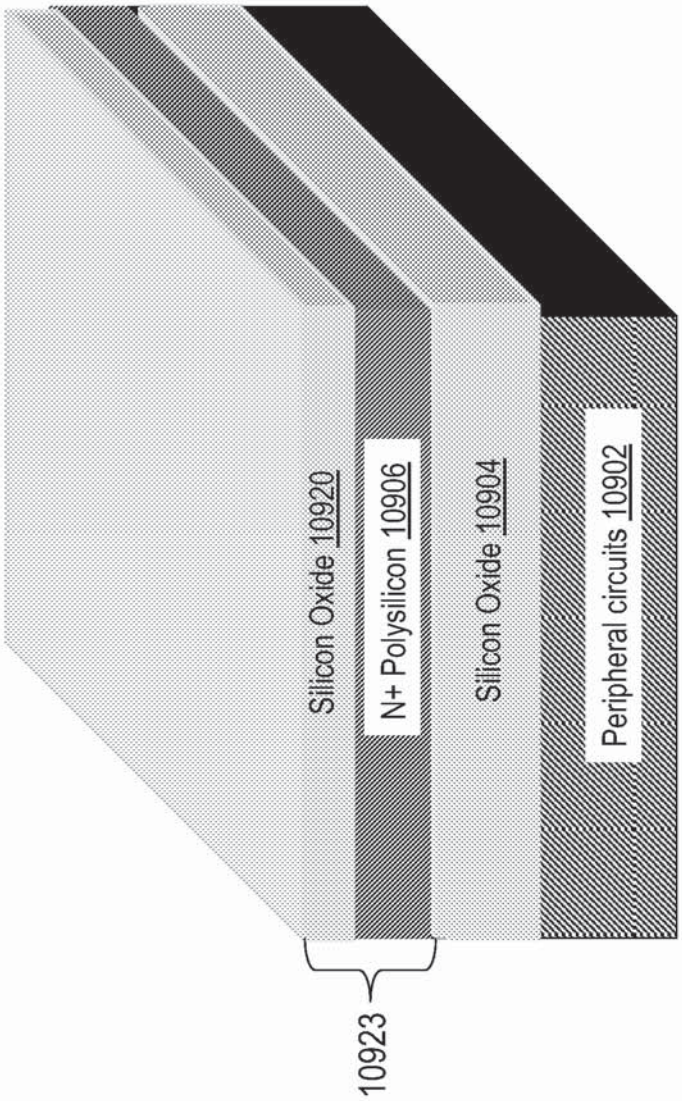

Silicon Oxide 10920
N+ Polysilicon 10906
Silicon Oxide 10904
Peripheral circuits 10902
10923

FIG. 109B

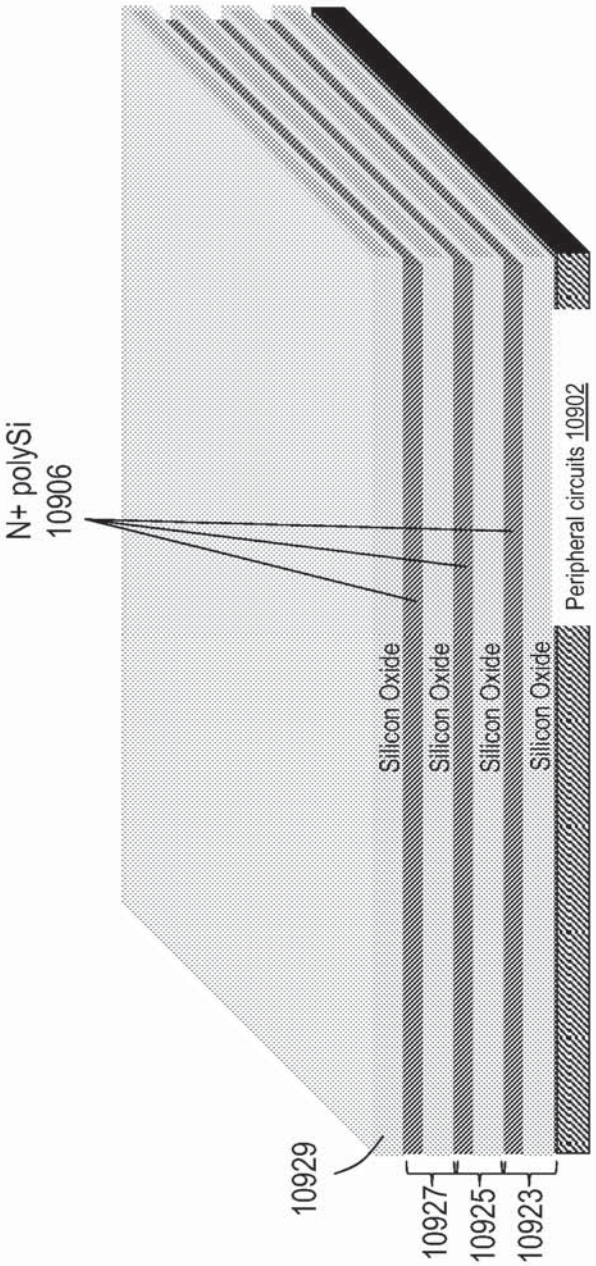

N+ polySi
10906
Silicon Oxide
Silicon Oxide
Silicon Oxide
Silicon Oxide
Peripheral circuits 10902
10929
10927
10925
10923

FIG. 109C

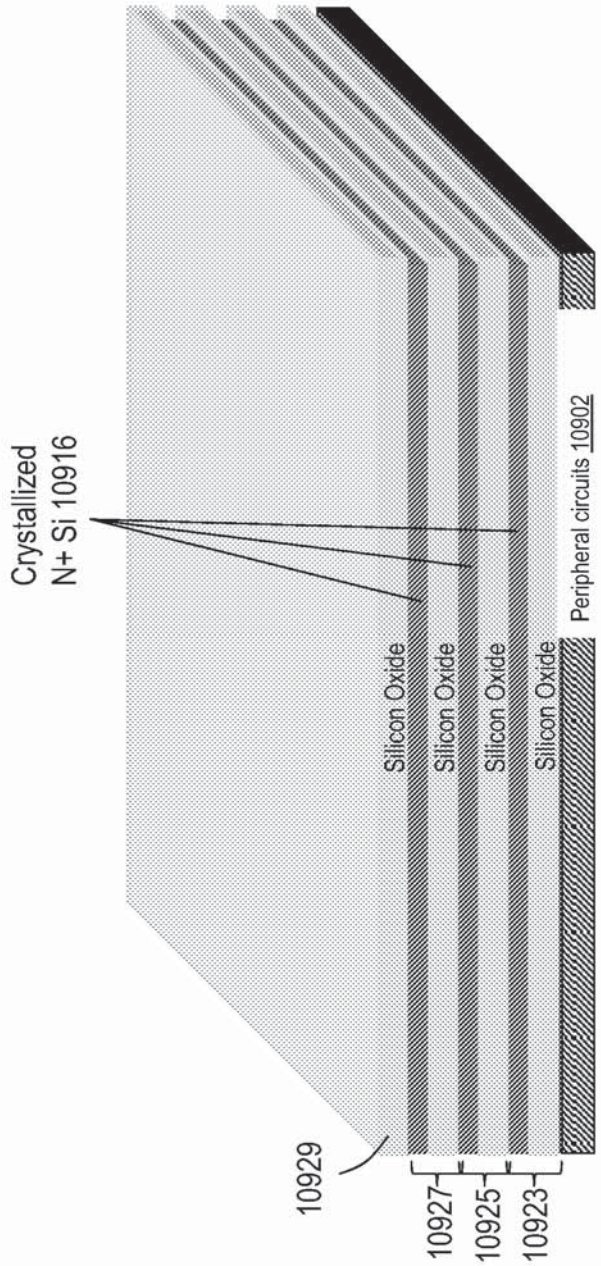

Crystallized
N+ Si 10916
Silicon Oxide
Silicon Oxide
Silicon Oxide
Silicon Oxide
Peripheral circuits 10902
10929
10927
10925
10923

FIG. 109D

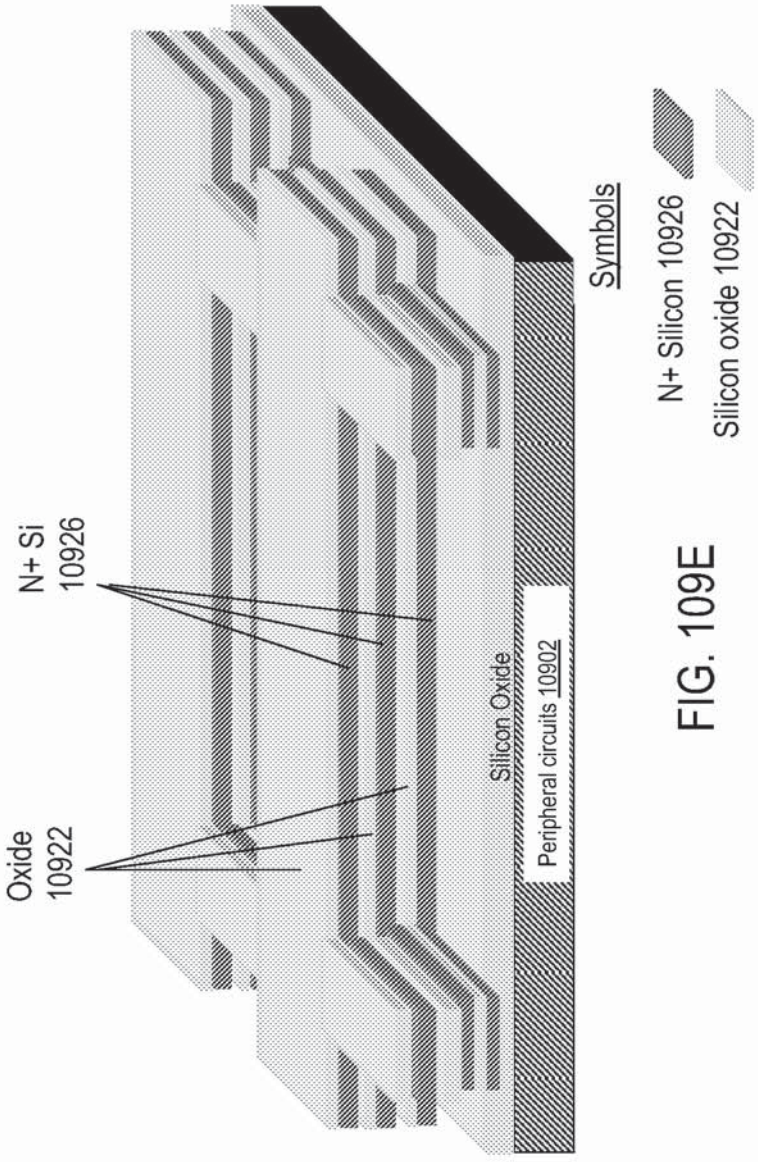

Oxide
10922
N+ Si
10926
Silicon Oxide
Peripheral circuits 10902
Symbols
N+ Silicon 10926
Silicon oxide 10922

FIG. 109E

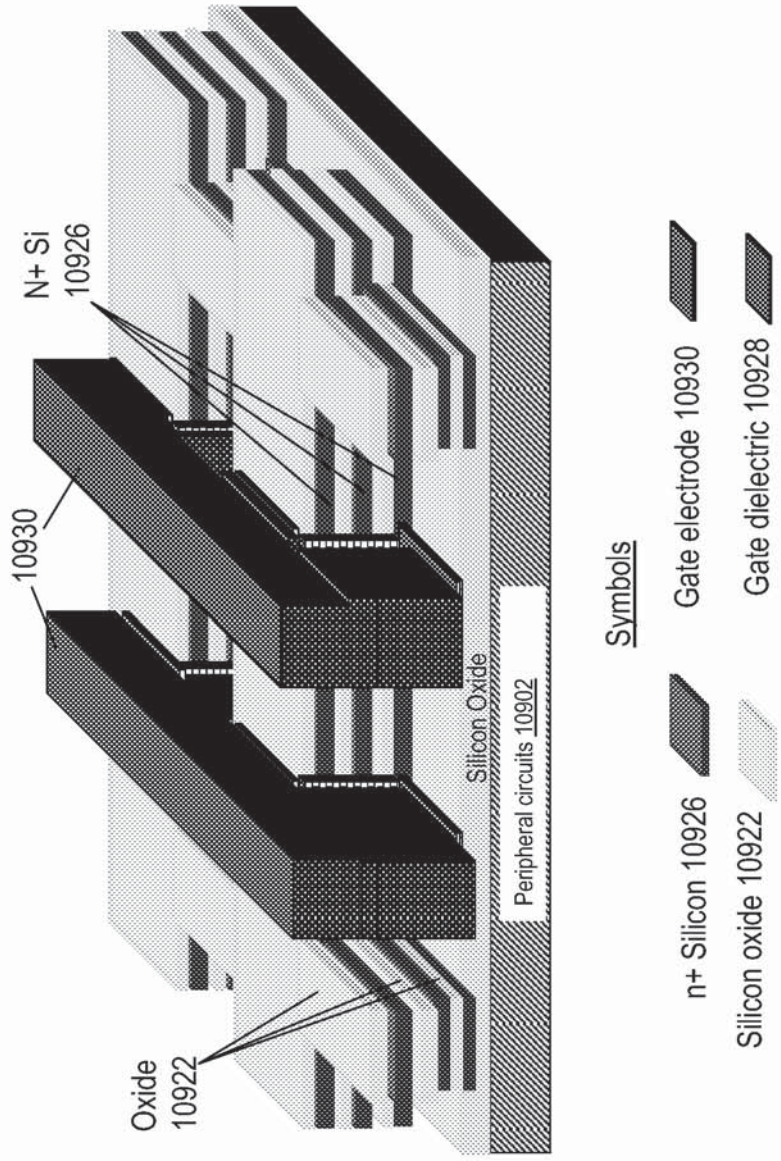

N+ Si
10926
10930
Oxide
10922
Silicon Oxide
Peripheral circuits 10902
Symbols
n+ Silicon 10926
Gate electrode 10930
Silicon oxide 10922
Gate dielectric 10928

FIG. 109F

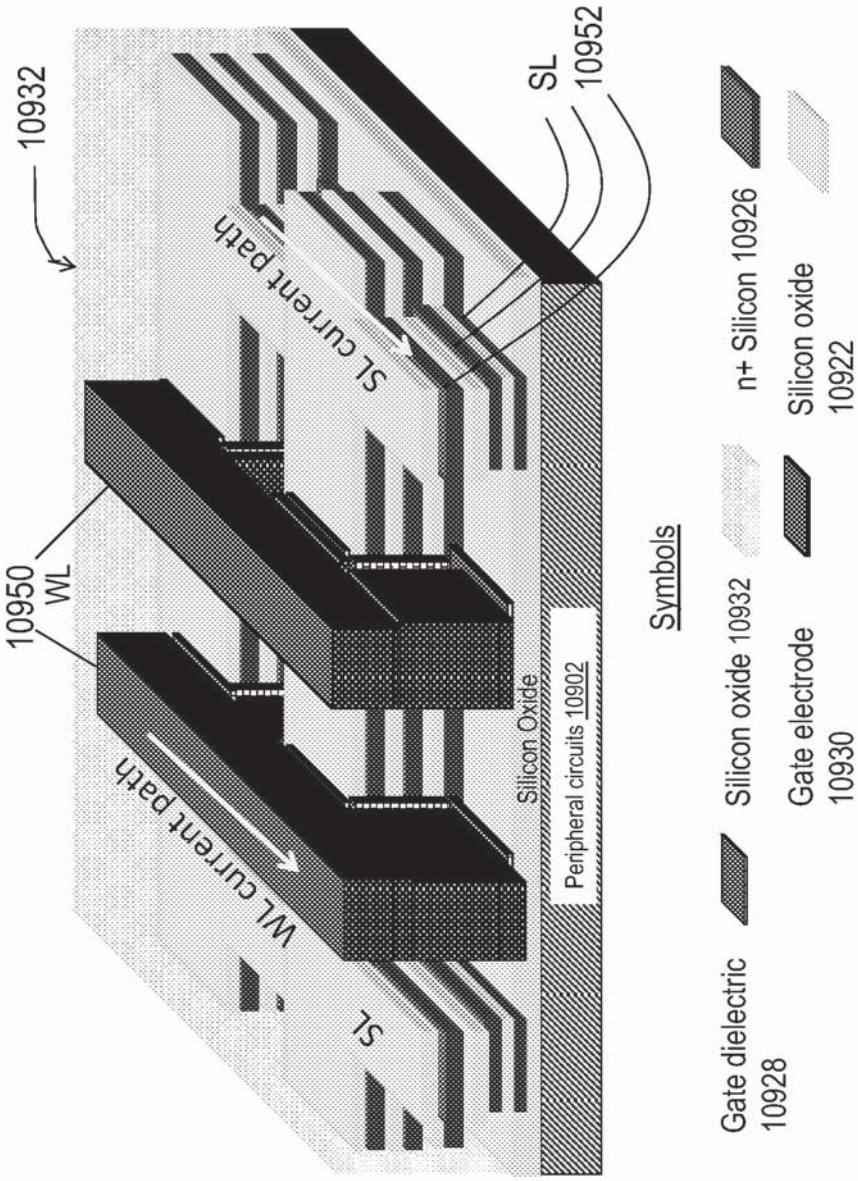

10932
SL
10952
SL current path
10950
WL
WL current path
SL
Silicon Oxide
Peripheral circuits 10902
Symbols
Gate dielectric 10928
Silicon oxide 10932
Gate electrode 10930
n+ Silicon 10926
Silicon oxide 10922

FIG. 109G

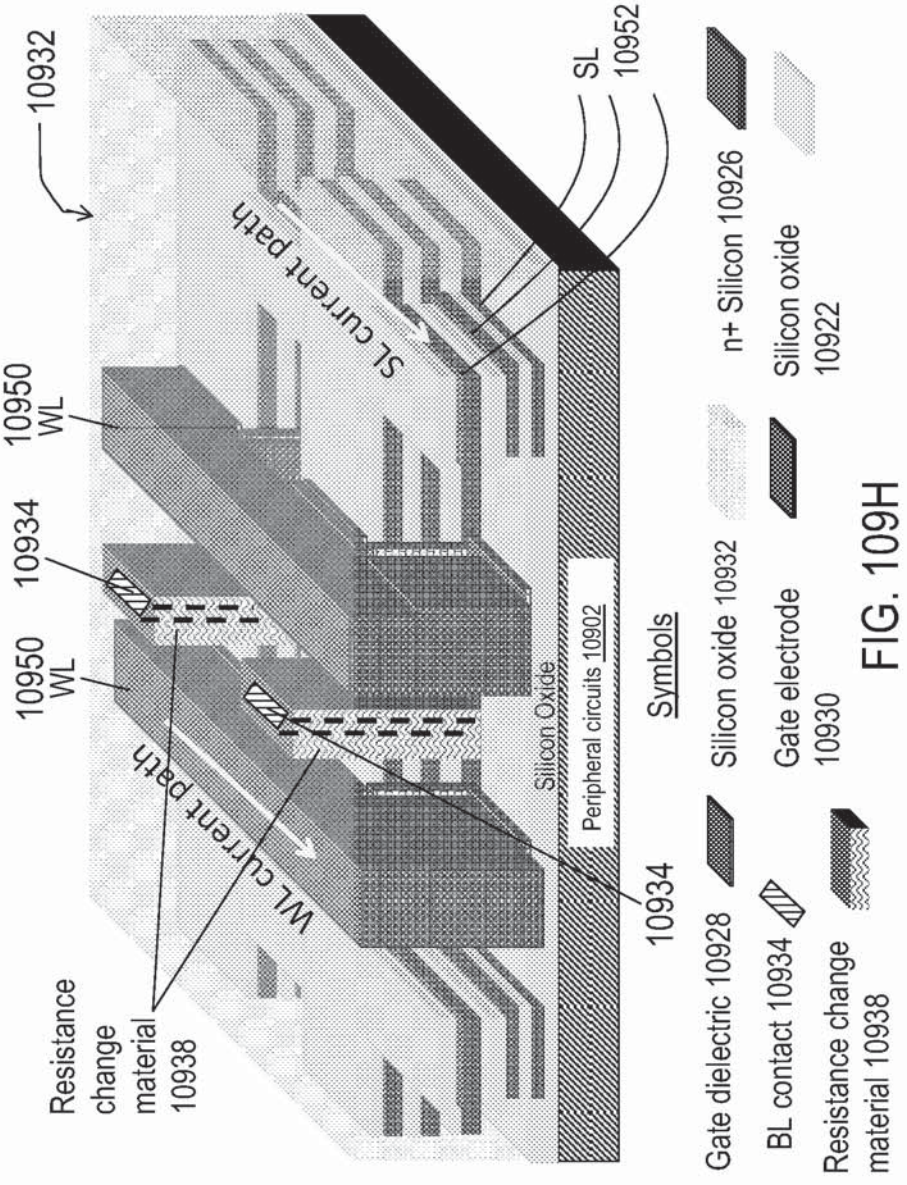

10932
SL
10952
SL current path
10950
WL
10934
10950
WL
WL current path
Resistance
change
material
10938
Silicon Oxide
Peripheral circuits 10902
10934
Symbols
Gate dielectric 10928
Silicon oxide 10932
n+ Silicon 10926
BL contact 10934
Gate electrode
10930
Silicon oxide
10922
Resistance change
material 10938

FIG. 109H

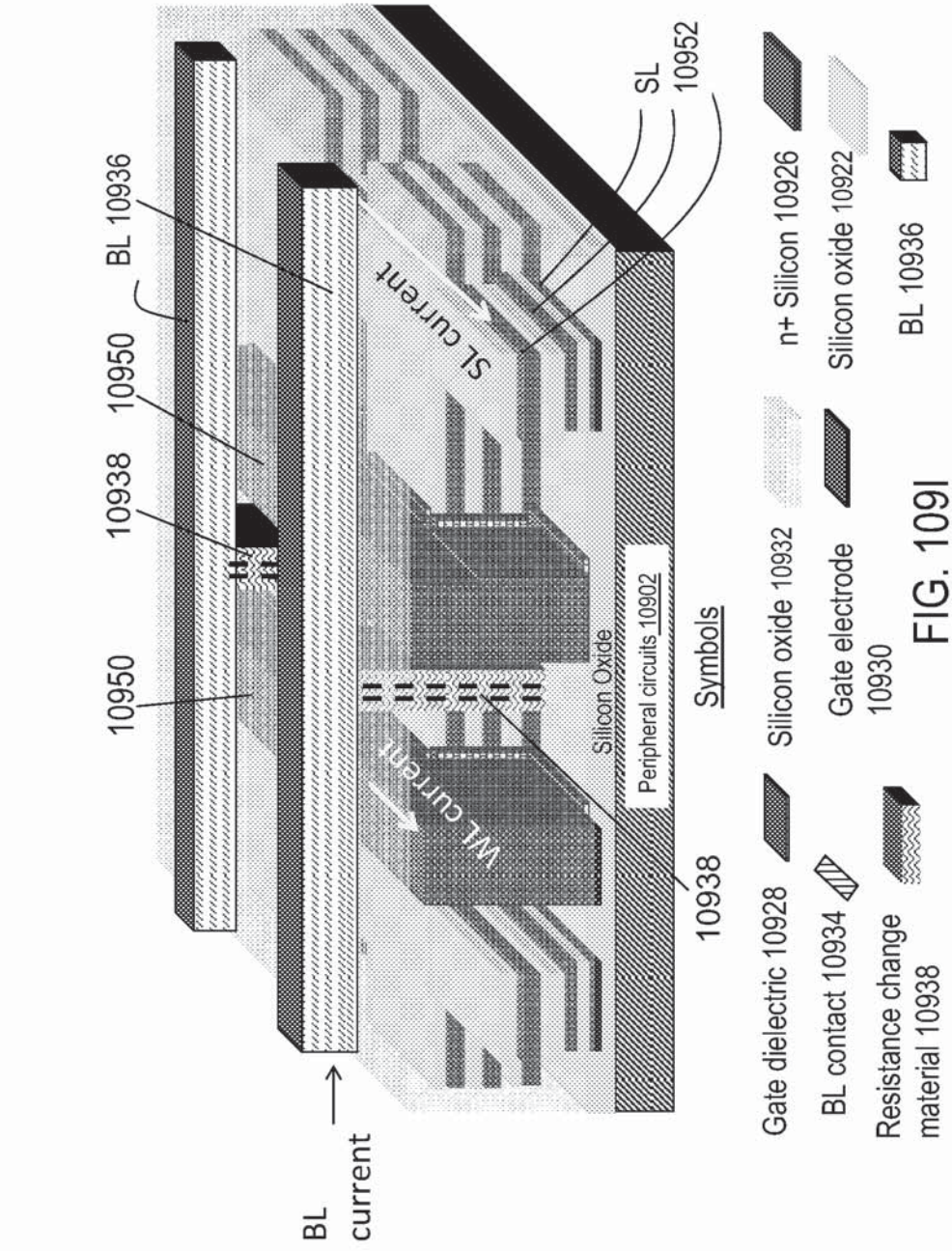

BL 10936
10950
10938
10950
SL
10952
SL current
WL current
Silicon Oxide
Peripheral circuits 10902
10938
BL current
Symbols
Gate dielectric 10928
Silicon oxide 10932
n+ Silicon 10926
BL contact 10934
Gate electrode 10930
Silicon oxide 10922
Resistance change material 10938
BL 10936

FIG. 109I

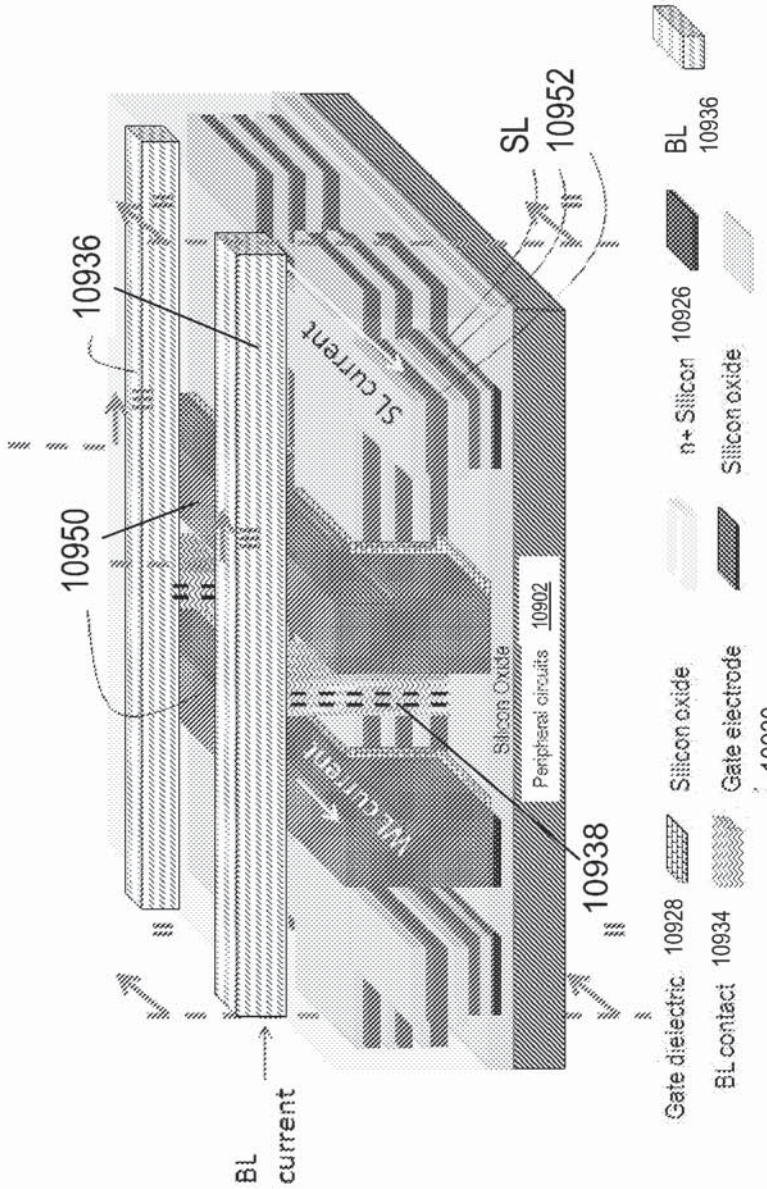

10936
10950
SL current
SL
10952
BL
10936
n+ Silicon 10926
Silicon oxide
Silicon Oxide
Peripheral circuits 10902
WL current
10938
Gate dielectric 10928
Silicon oxide
BL contact 10934
Gate electrode
10930
Resistance change material 10938
BL current

FIG. 109J

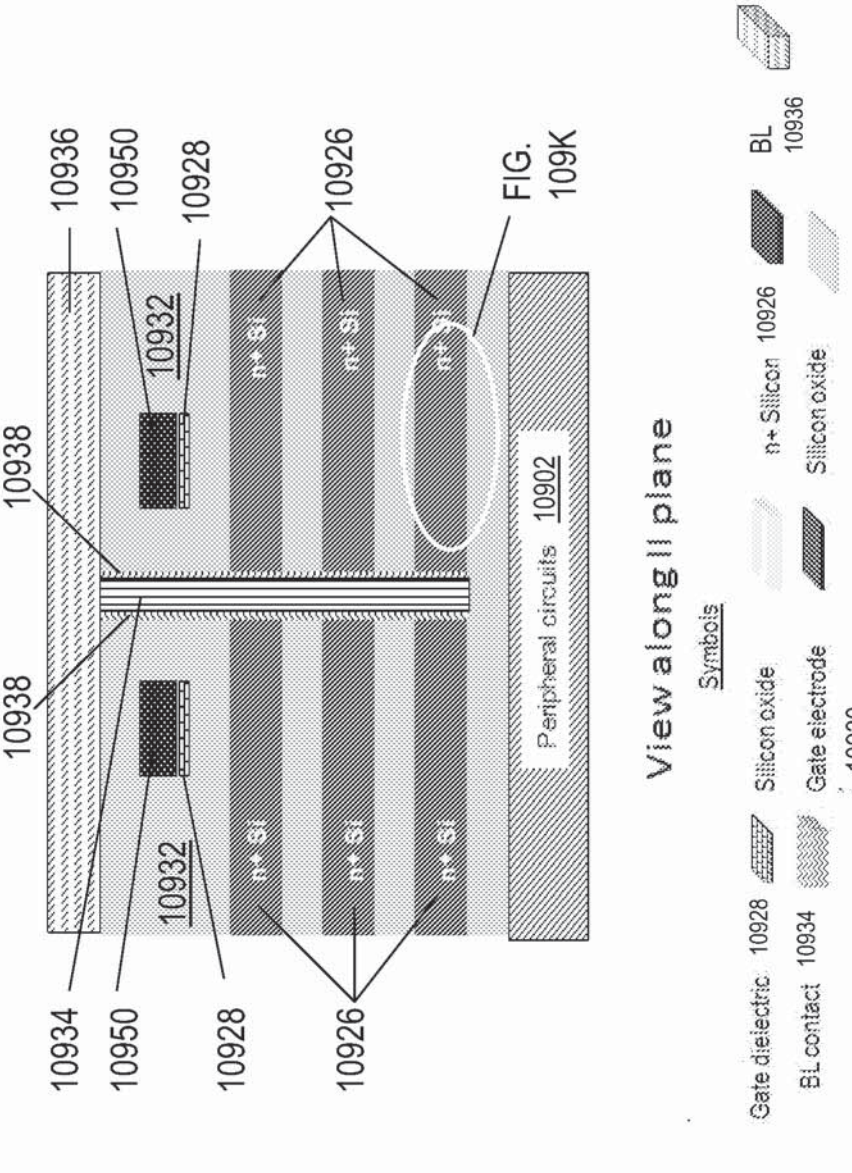

10936
10950
10928
10926
10938
10932
n+ Si
FIG. 109K
Peripheral circuits 10902
10934
10950
10928
10926
10938
10932
n+ Si
View along II plane
Symbols
Gate dielectric 10928
Silicon oxide
n+ Silicon 10926
BL 10936
Bit contact 10934
Gate electrode 10930
Silicon oxide
Resistance change material 10938

FIG. 109J1

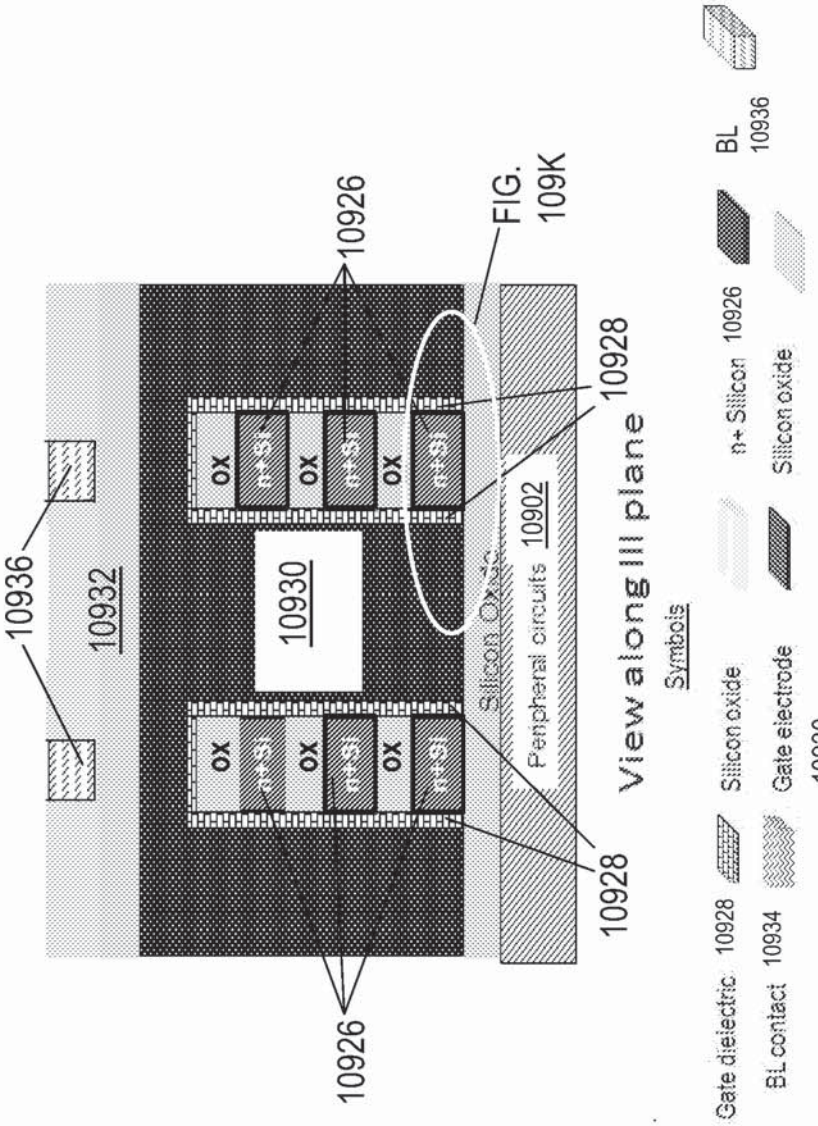

10936
10932
10926
10930
10928
FIG. 109K
View along III plane
Peripheral circuits 10902
Silicon Oxide
ox
n+Si
Symbols
Gate dielectric 10928
Bl contact 10934
Silicon oxide
Gate electrode 10930
n+ Silicon 10926
Silicon oxide
BL 10936

FIG. 109J2

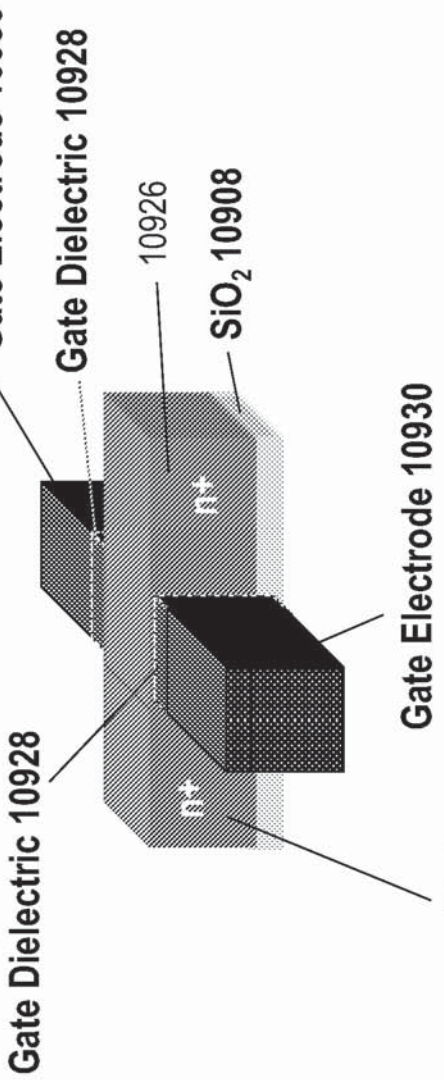

Gate Electrode 10930
Gate Dielectric 10928
10926
SiO_2 10908
n+
n+
Gate Electrode 10930
Gate Dielectric 10928
10926

FIG. 109K

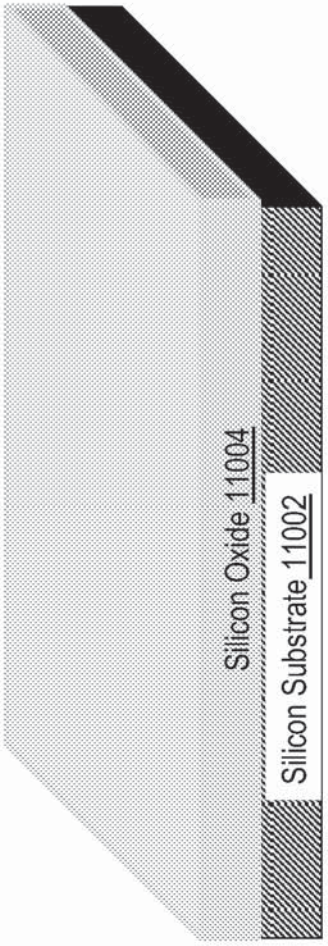


FIG. 110A

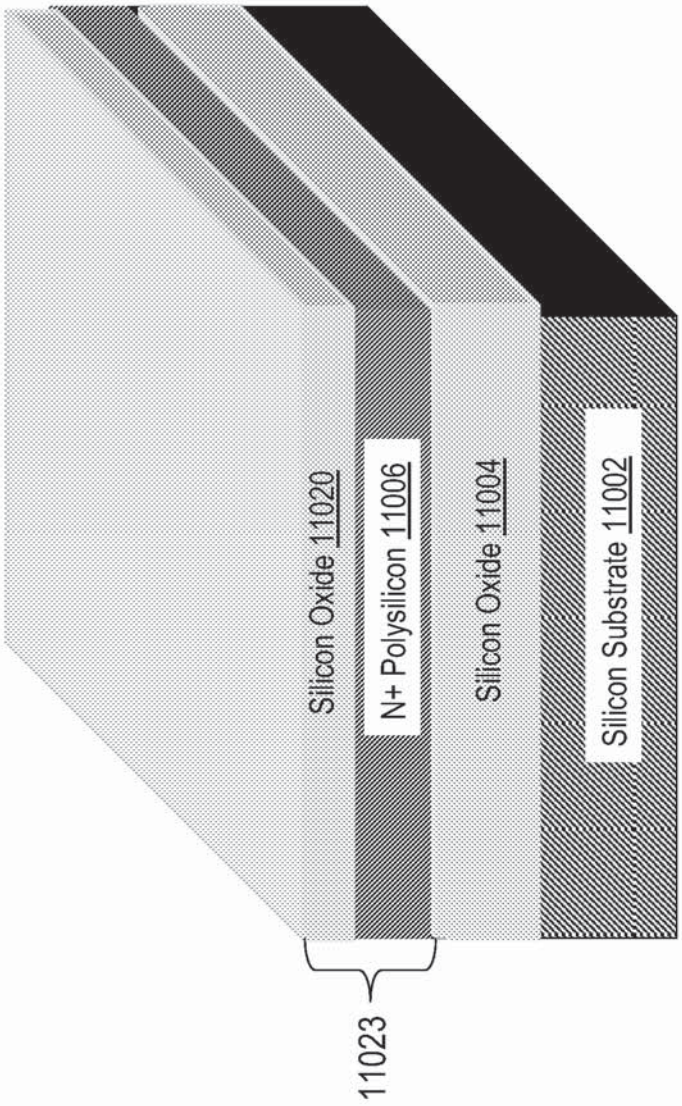

Silicon Oxide 11020
N+ Polysilicon 11006
Silicon Oxide 11004
Silicon Substrate 11002
11023

FIG. 110B

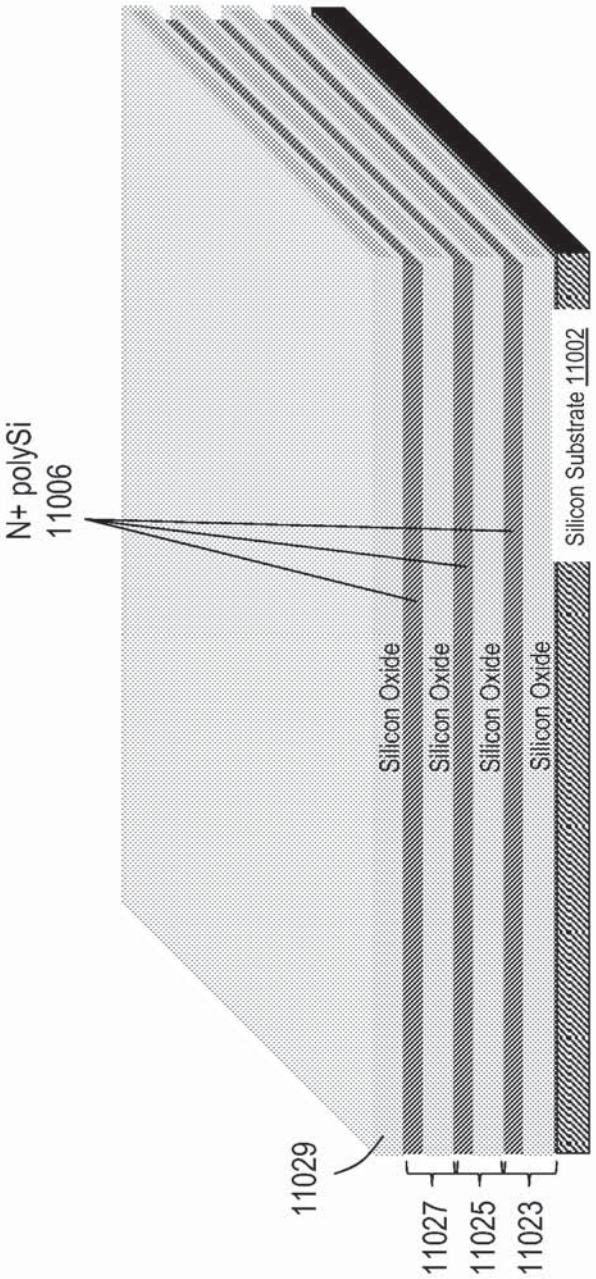

N+ polySi
11006
Silicon Oxide
Silicon Oxide
Silicon Oxide
Silicon Oxide
Silicon Substrate 11002
11029
11027
11025
11023

FIG. 110C

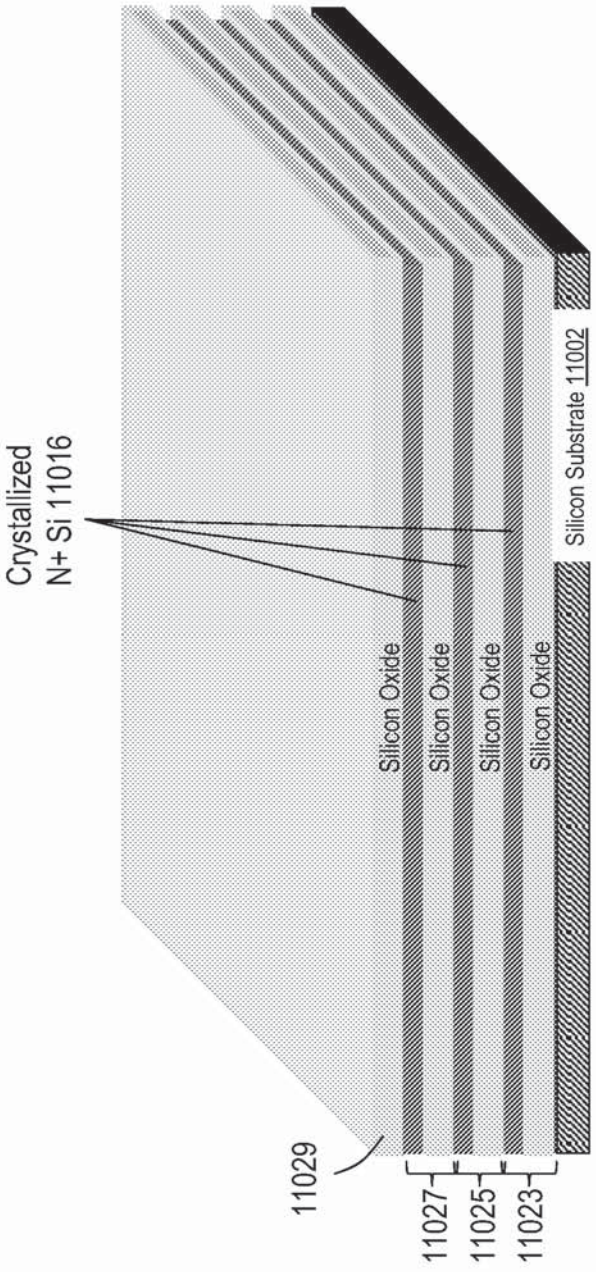

Crystallized
N+ Si 11016
Silicon Oxide
Silicon Oxide
Silicon Oxide
Silicon Oxide
Silicon Substrate 11002
11029
11027
11025
11023

FIG. 110D

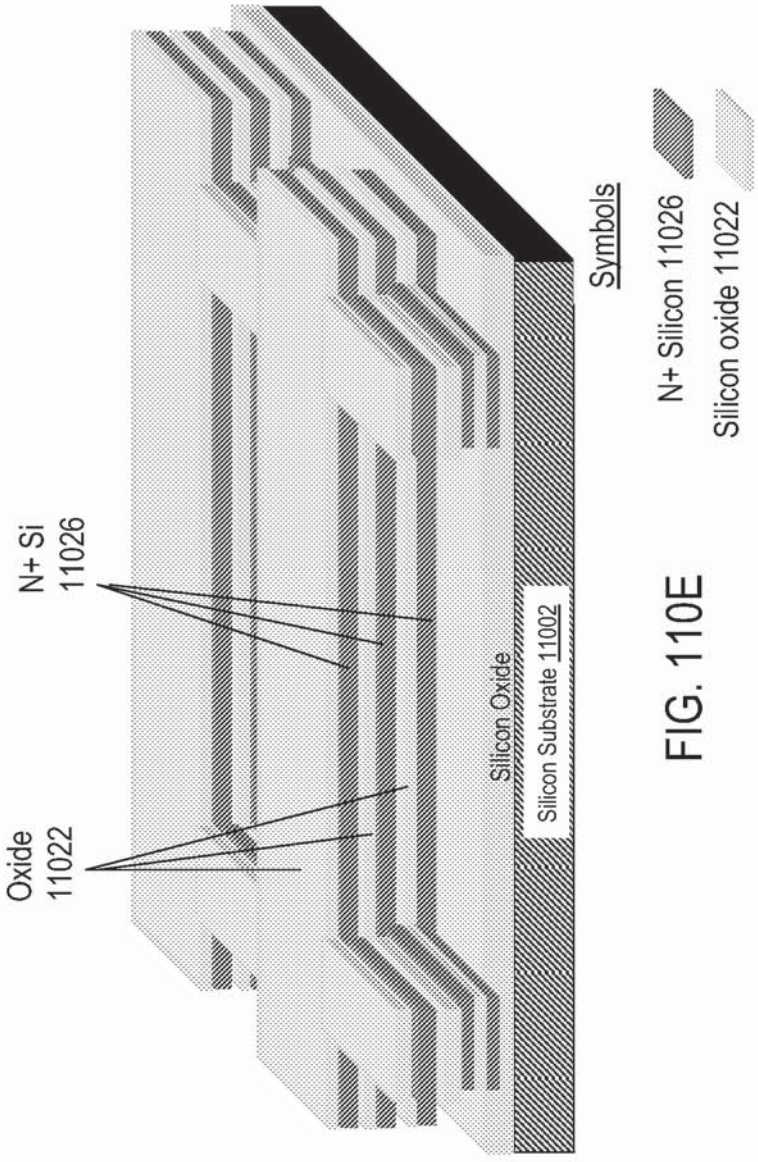

Oxide
11022
N+ Si
11026
Silicon Oxide
Silicon Substrate 11002
Symbols
N+ Silicon 11026
Silicon oxide 11022

FIG. 110E

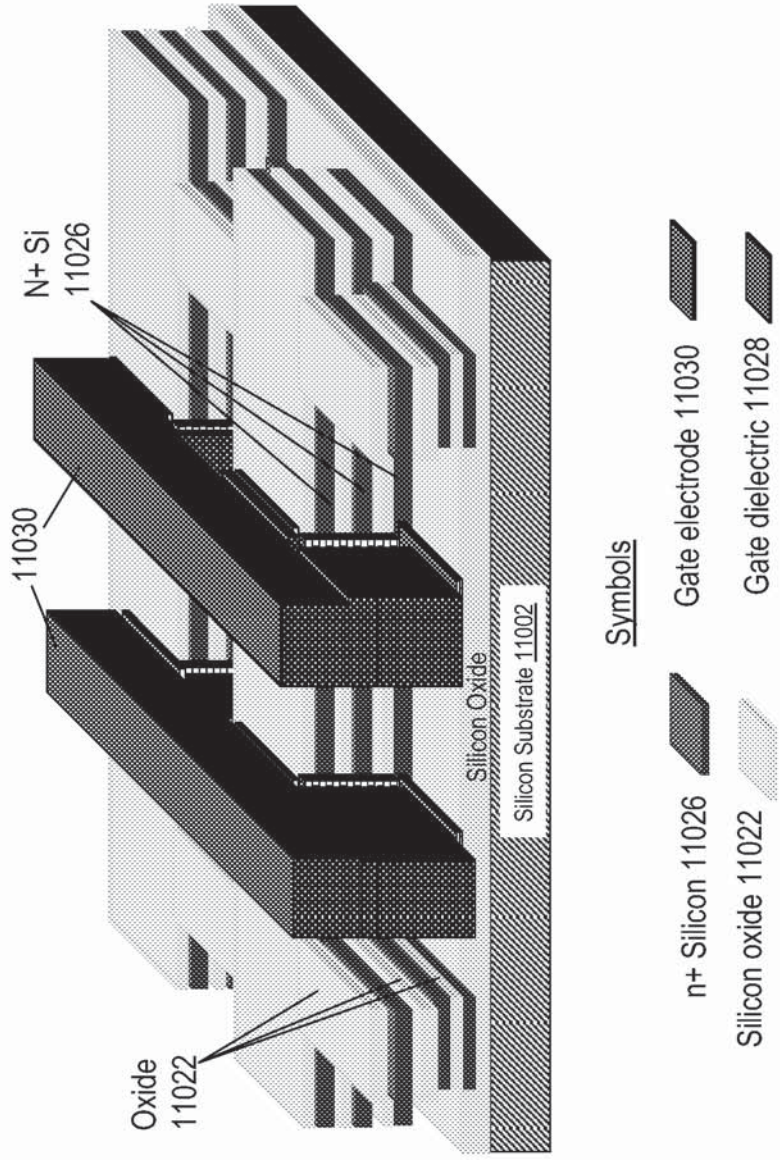

N+ Si
11026
11030
Oxide
11022
Silicon Oxide
Silicon Substrate 11002
Symbols
n+ Silicon 11026
Gate electrode 11030
Silicon oxide 11022
Gate dielectric 11028

FIG. 110F

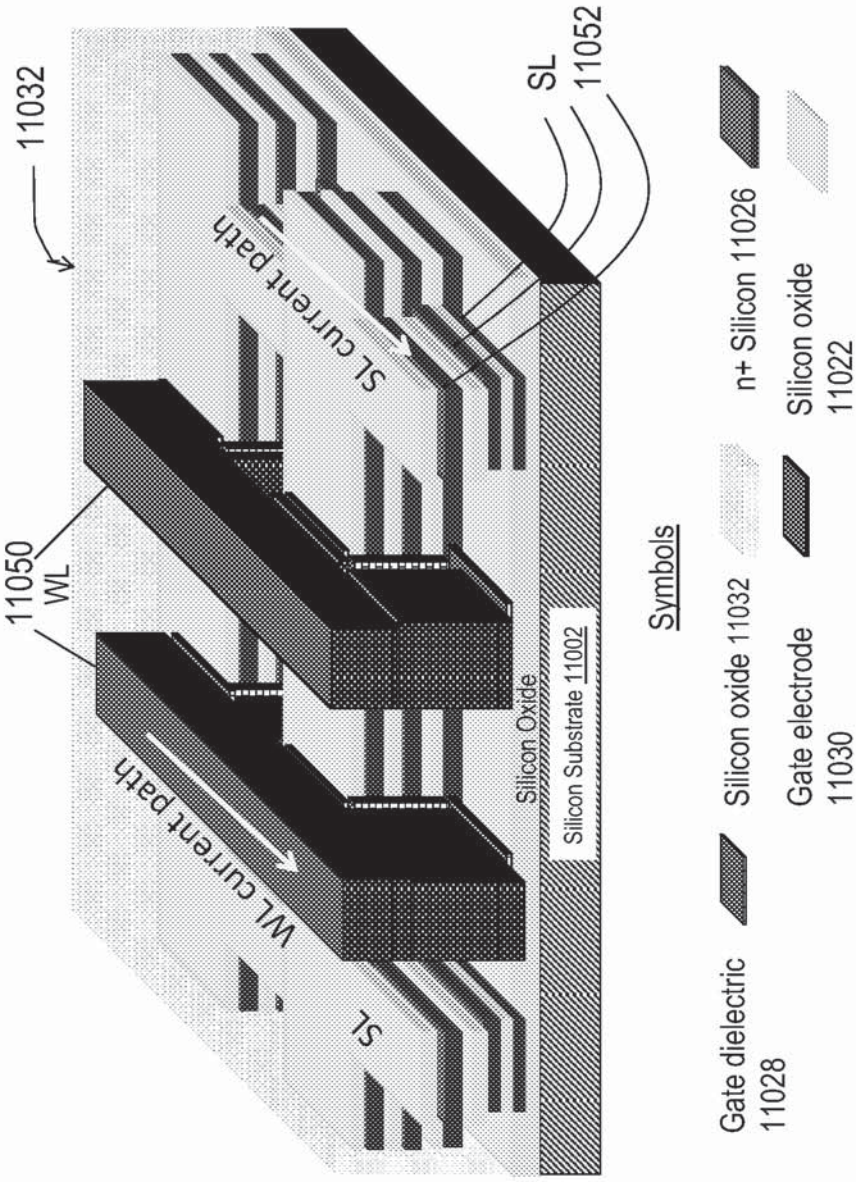

11032
SL
11052
SL current path
11050
WL
WL current path
SL
Silicon Oxide
Silicon Substrate 11002
Symbols
Gate dielectric 11028
Silicon oxide 11032
Gate electrode 11030
n+ Silicon 11026
Silicon oxide 11022

FIG. 110G

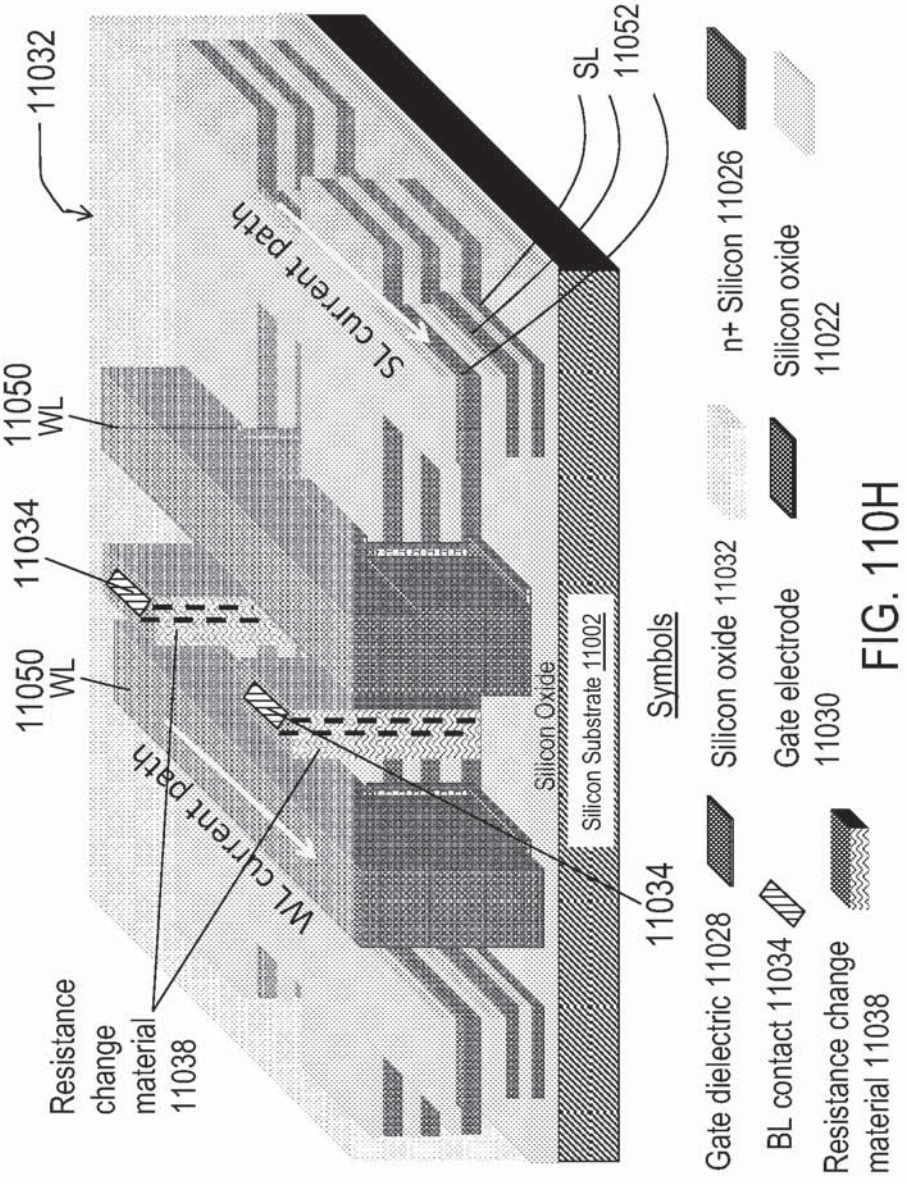

11032
SL
11052
SL current path
11050
WL
11034
11050
WL
WL current path
Resistance
change
material
11038
Silicon Oxide
Silicon Substrate 11002
11034
Symbols
Gate dielectric 11028
Silicon oxide 11032
n+ Silicon 11026
BL contact 11034
Gate electrode
11030
Silicon oxide
11022
Resistance change
material 11038

FIG. 110H

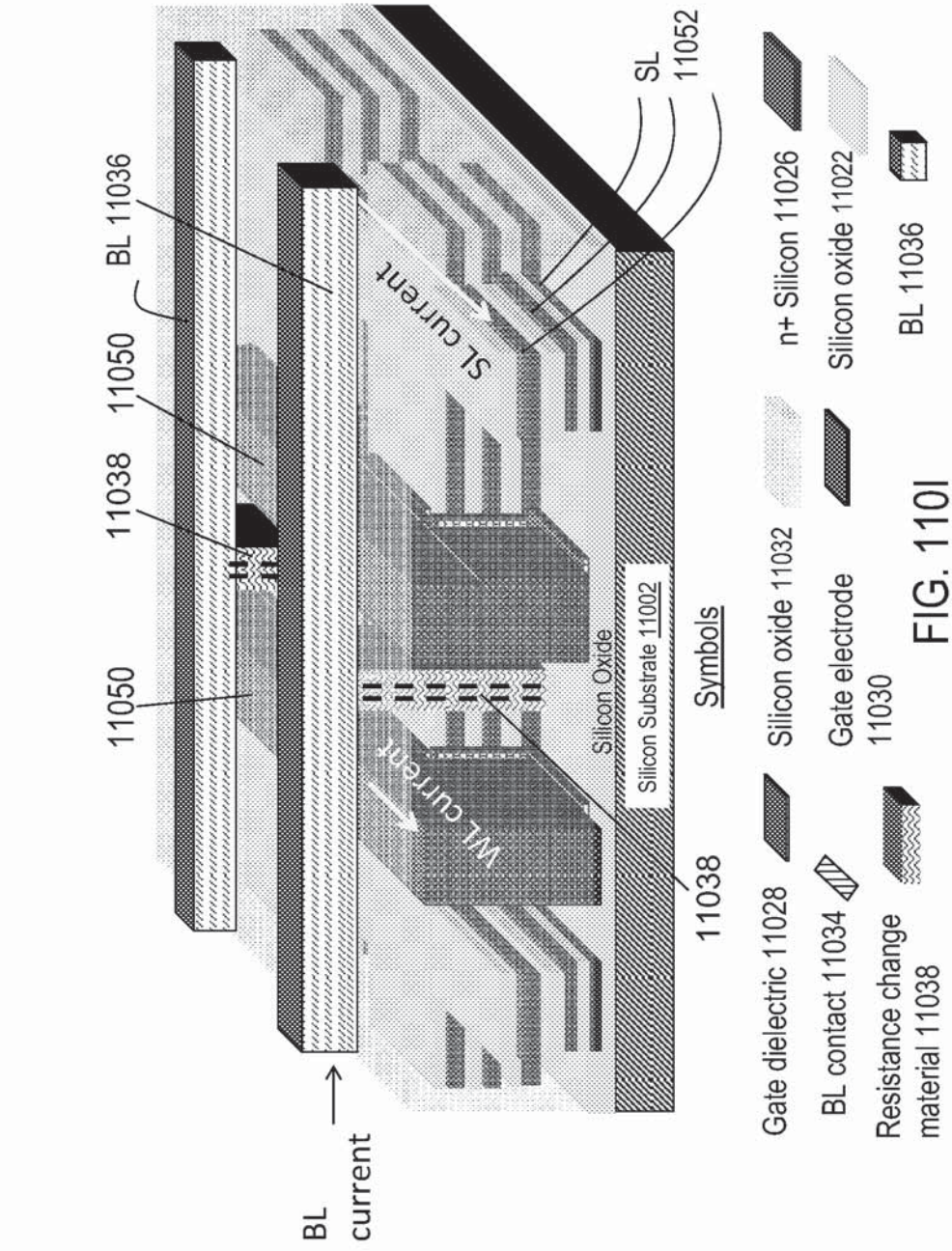

BL 11036
11050
11038
11050
SL
11052
SL current
WL current
Silicon Oxide
Silicon Substrate 11002
11038
BL current
Symbols
Gate dielectric 11028
Silicon oxide 11032
n+ Silicon 11026
BL contact 11034
Gate electrode 11030
Silicon oxide 11022
Resistance change material 11038
BL 11036

FIG. 110I

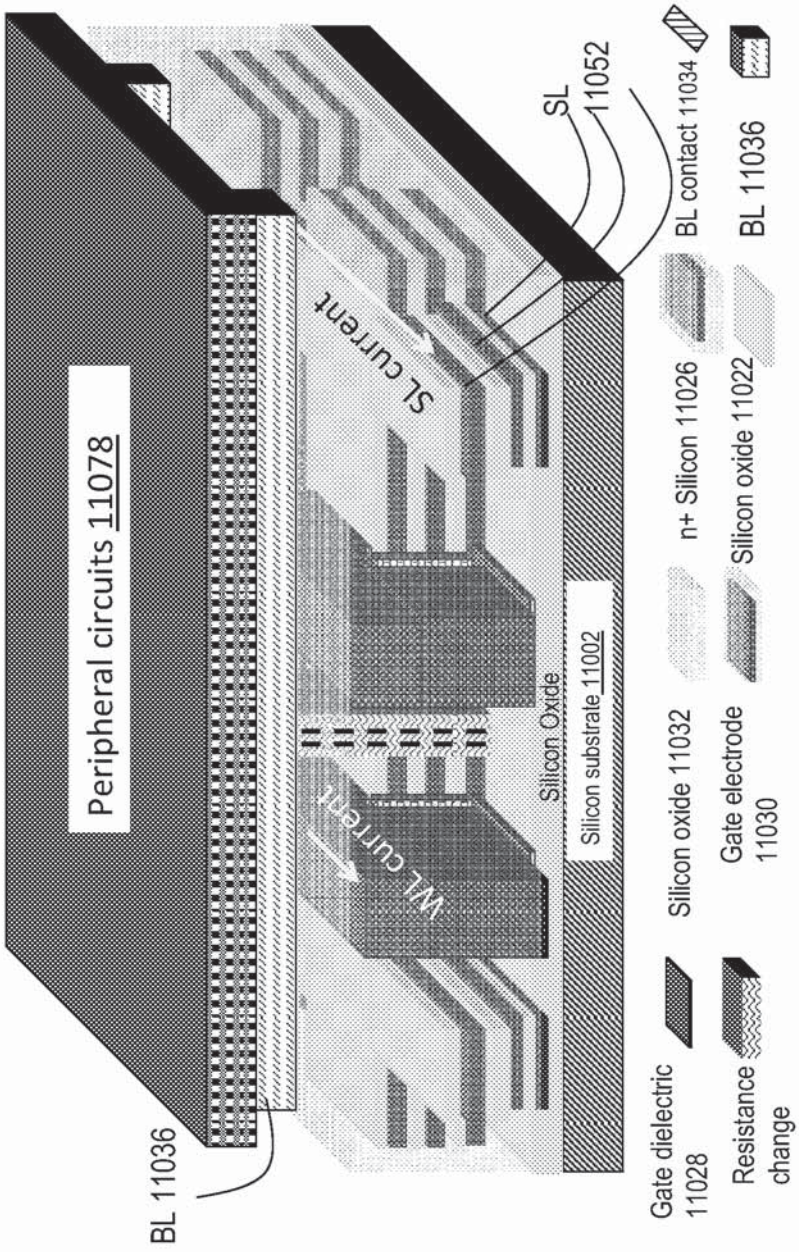

Peripheral circuits 11078
BL 11036
WL current
SL current
Silicon Oxide
Silicon substrate 11002
SL 11052
BL contact 11034
BL 11036
Gate dielectric 11028
Silicon oxide 11032
n+ Silicon 11026
Silicon oxide 11022
Resistance change memory 11038
Gate electrode 11030

Fig. 110J

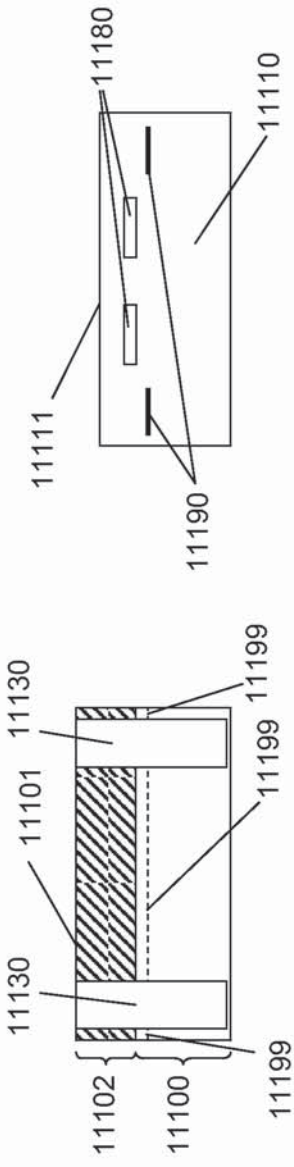

11180
11110
11111
11190
11130
11199
11199
11101
11130
11199
11102
11100

FIG. 111A

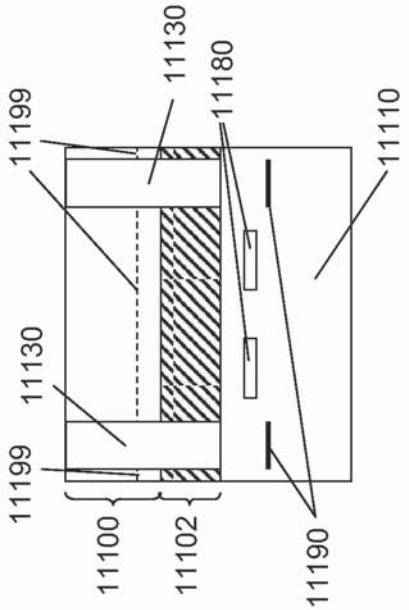


FIG. 111B

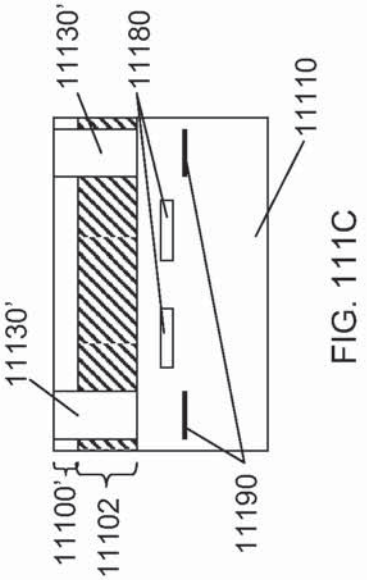


FIG. 111C

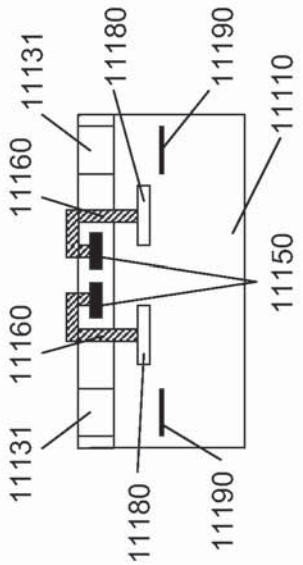

11131
11180
11190
11110
11160
11150
11160
11131
11180
11190

FIG. 111D

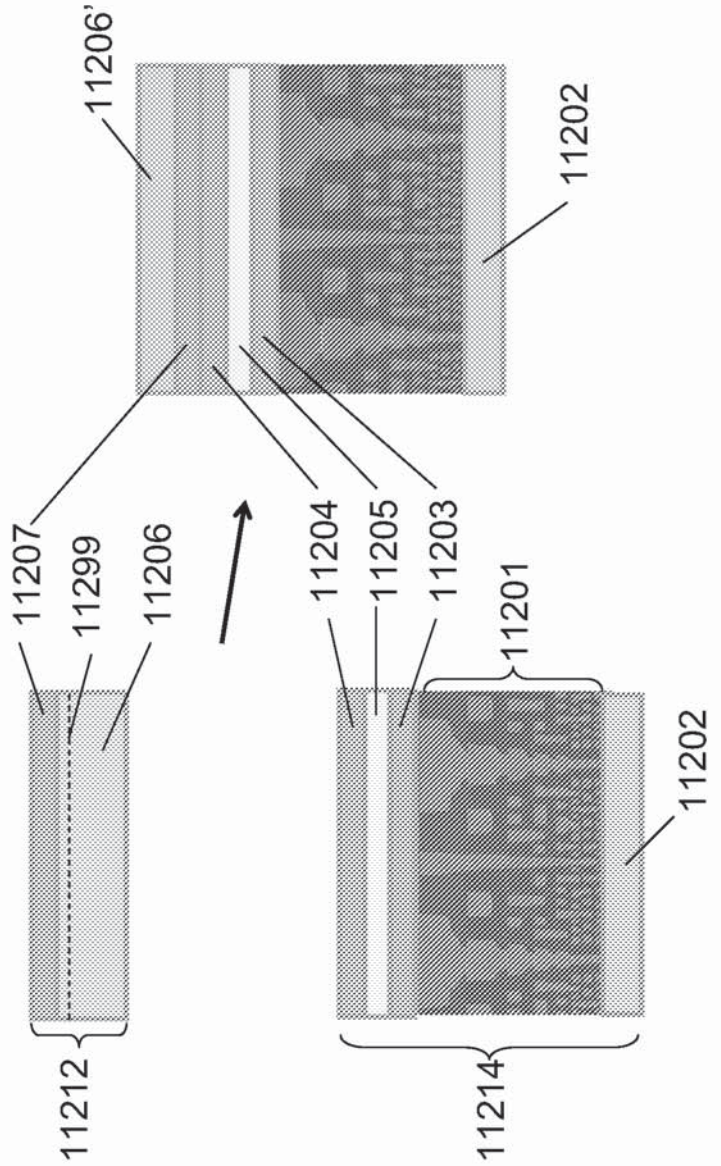

11206'
11202
11207
11299
11206
11204
11205
11203
11201
11202
11212
11214

FIG. 112

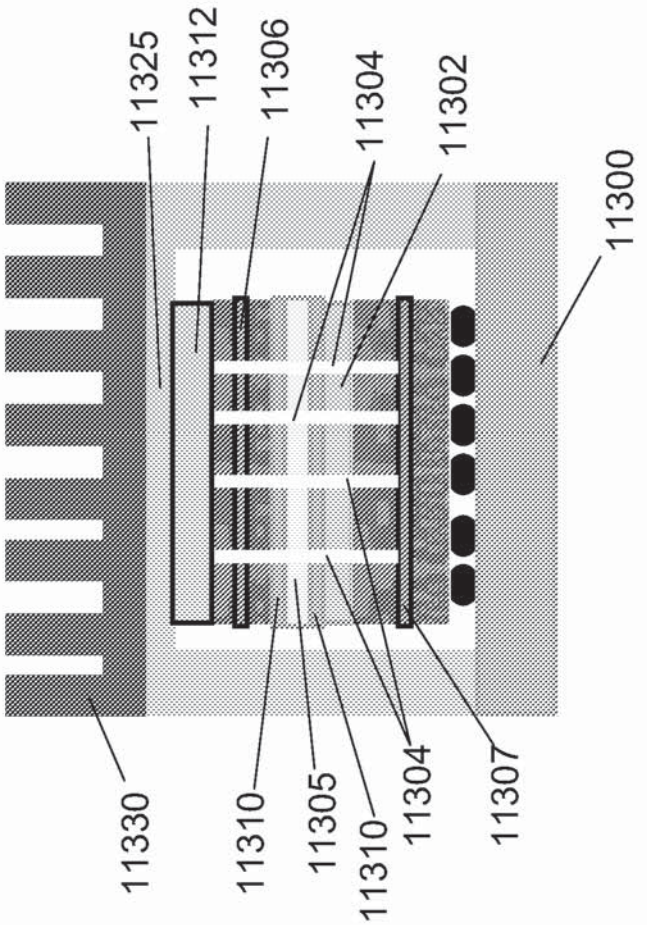

11325
11312
11306
11304
11302
11300
11330
11310
11305
11310
11304
11307

FIG. 113A

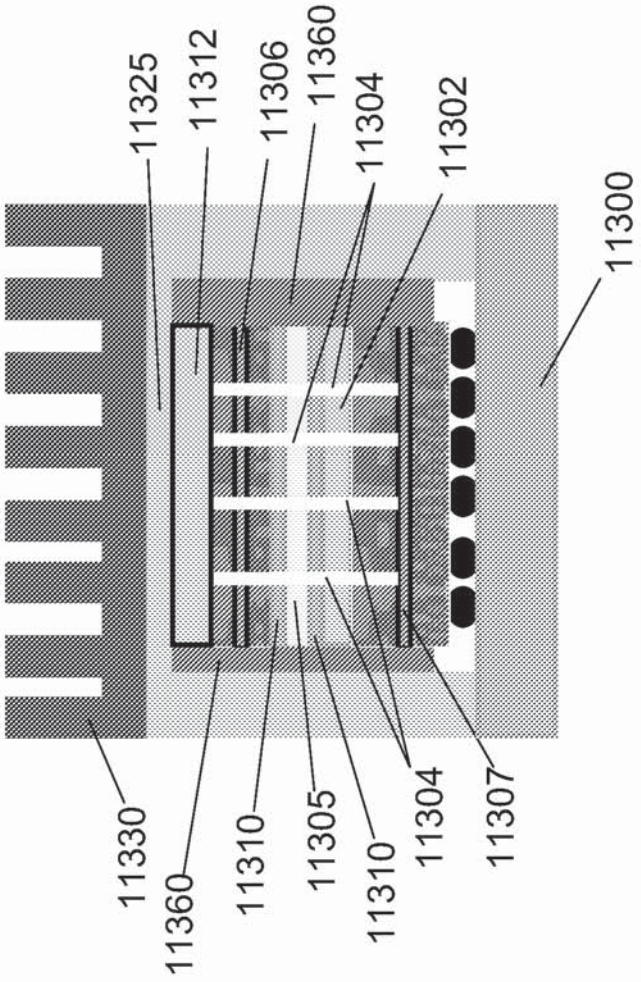

11325
11312
11306
11360
11304
11302
11300
11330
11360
11310
11305
11310
11304
11307

FIG. 113B

Figure 114

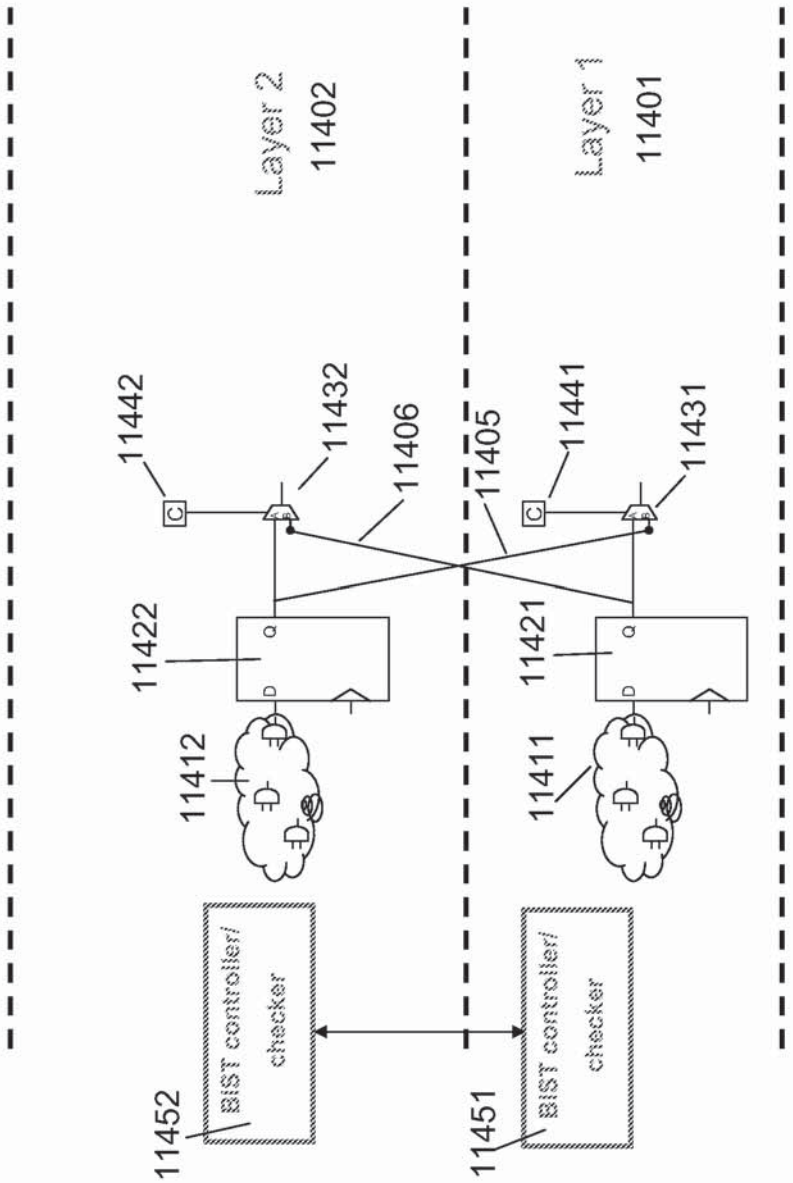
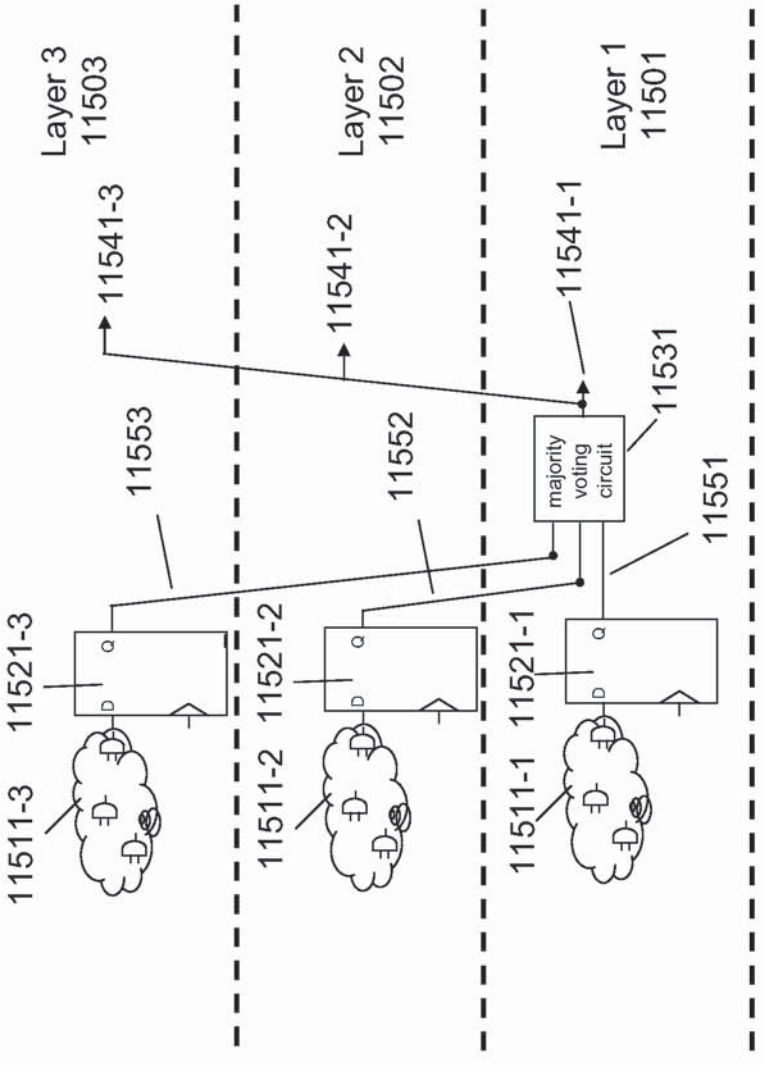

Layer 2
11402
Layer 1
11401
11442
11432
11406
11405
11441
11431
11422
11421
11412
11411
BIST controller/ checker
BIST controller/ checker
11452
11451

Figure 115


Layer 3
11503
Layer 2
11502
Layer 1
11501
11541-3
11541-2
11541-1
11531
majority
voting
circuit
11553
11552
11551
11521-3
11521-2
11521-1
11511-3
11511-2
11511-1
D
Q

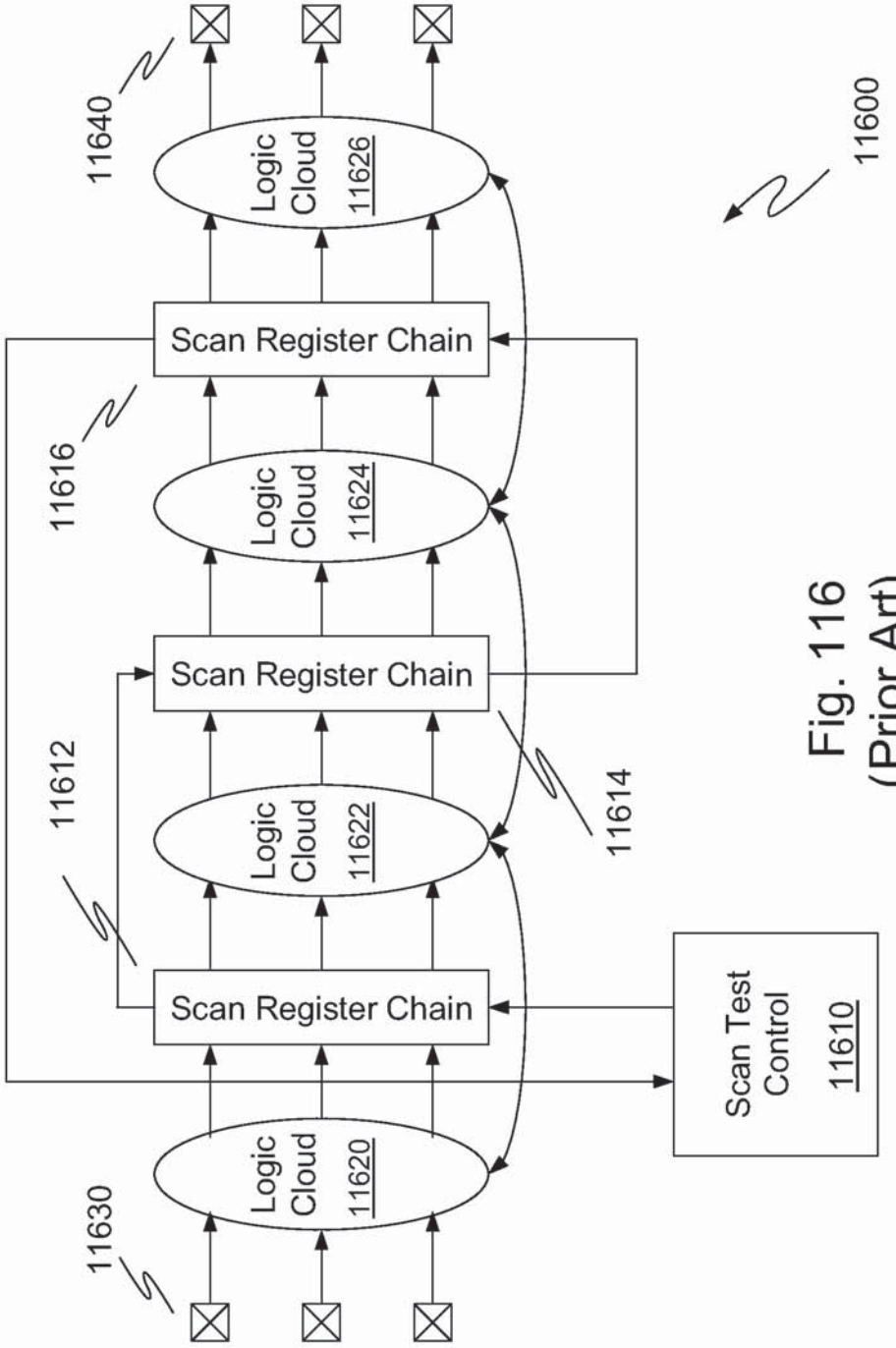


Fig. 116
(Prior Art)

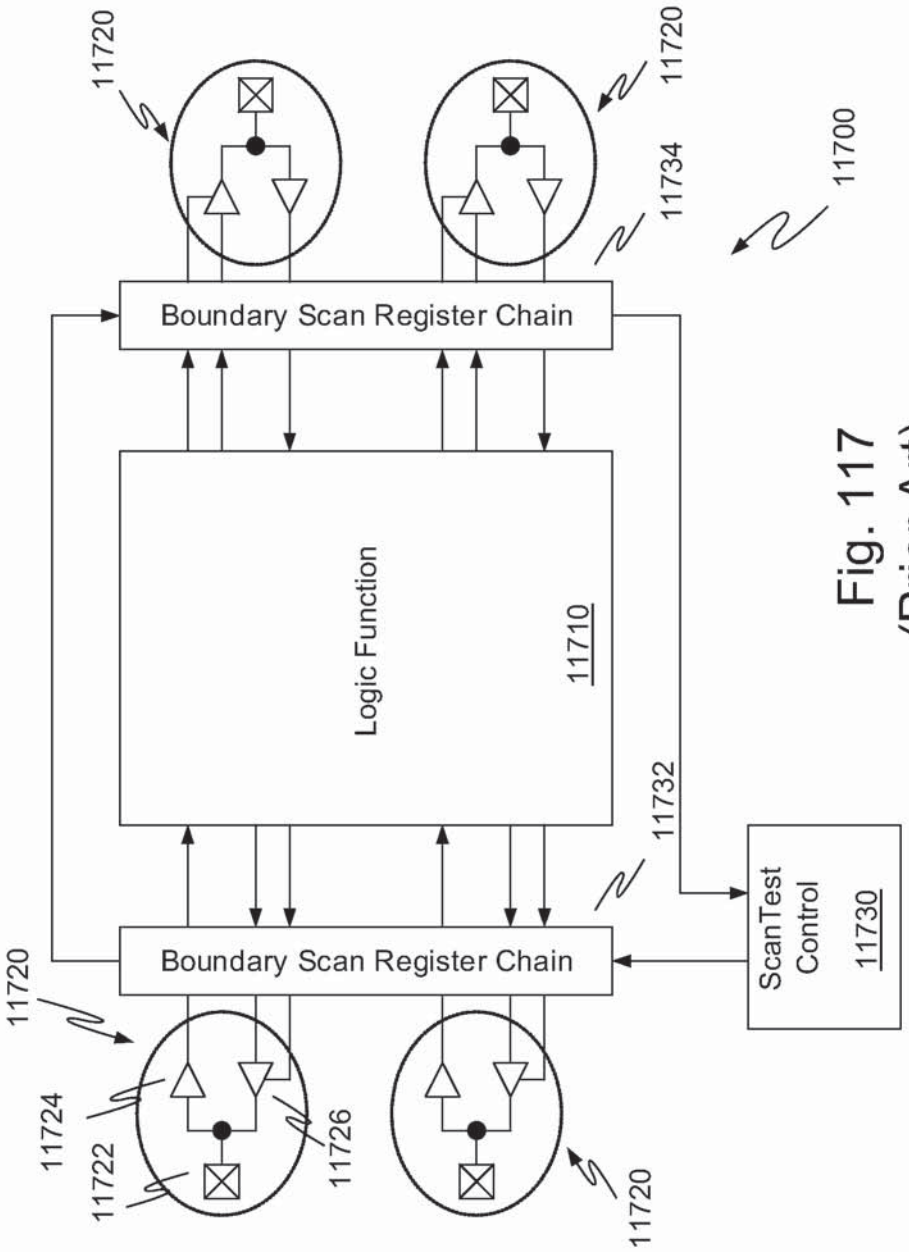


Fig. 117
(Prior Art)

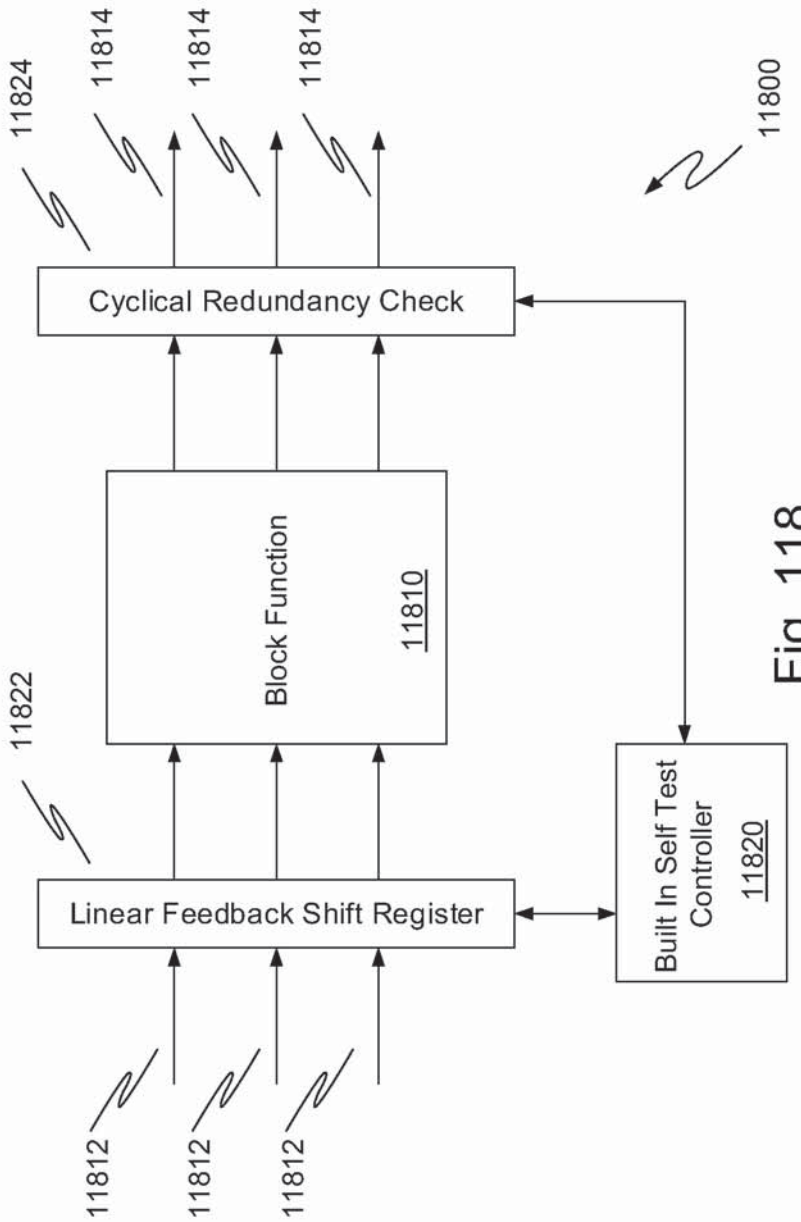


Fig. 118
(Prior Art)

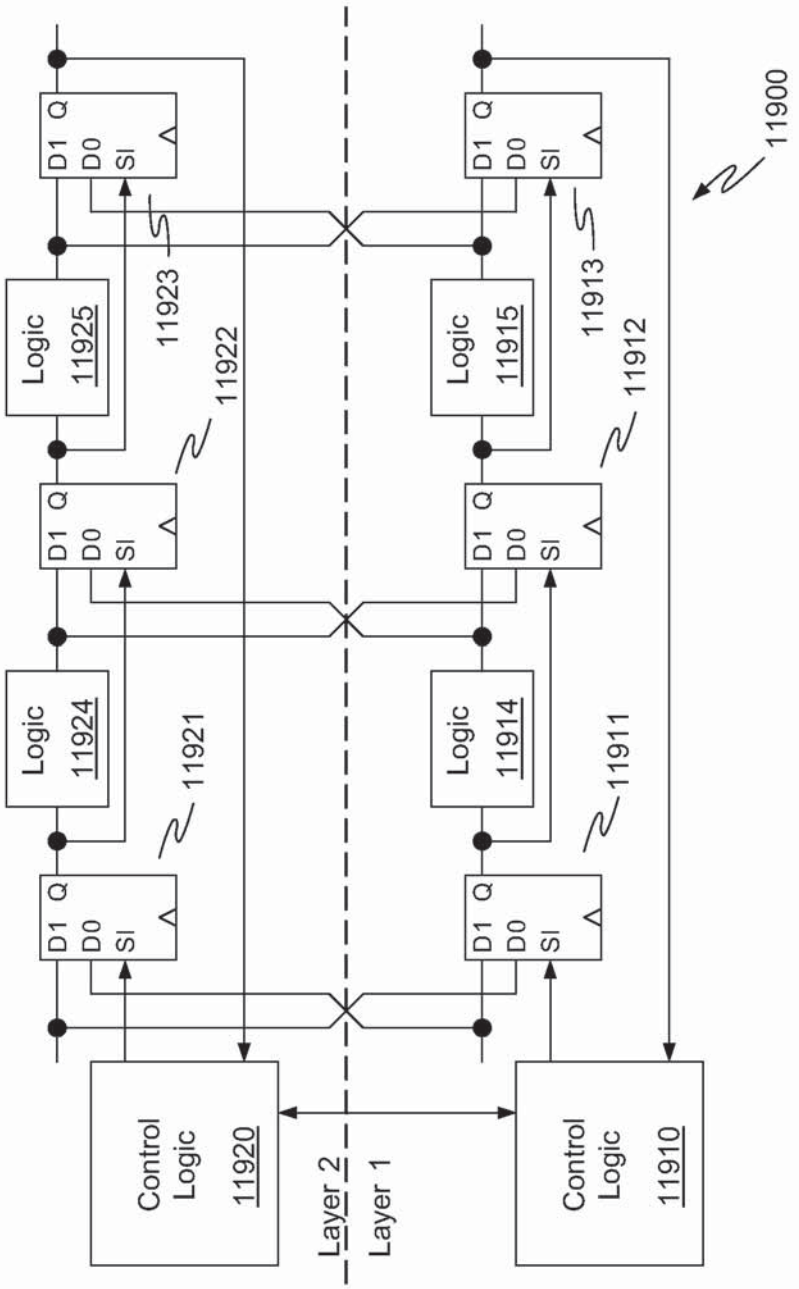

11900
11923
11922
11913
11912
11921
11911
Logic 11925
Logic 11924
Logic 11915
Logic 11914
D1 Q
D0
SI
Control Logic 11920
Control Logic 11910
Layer 2
Layer 1

Fig. 119

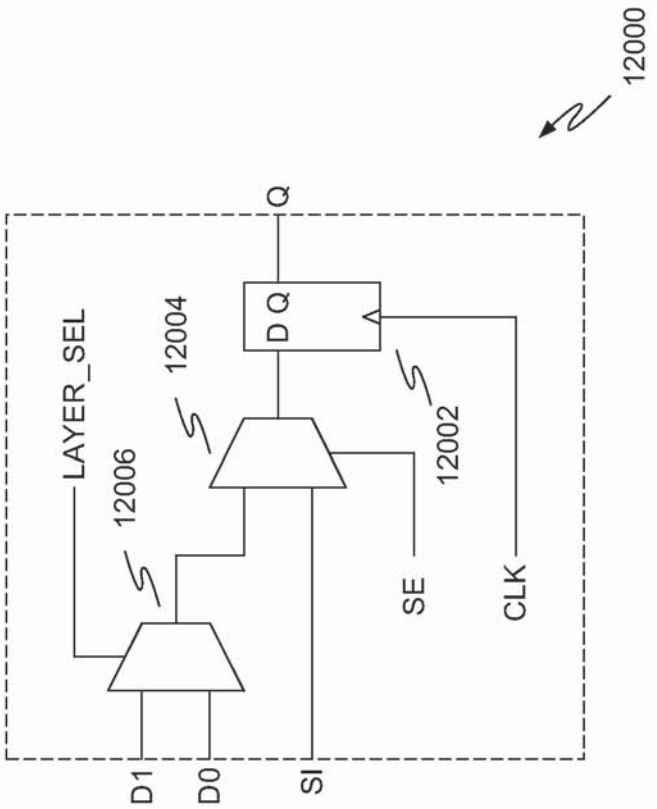


Fig. 120

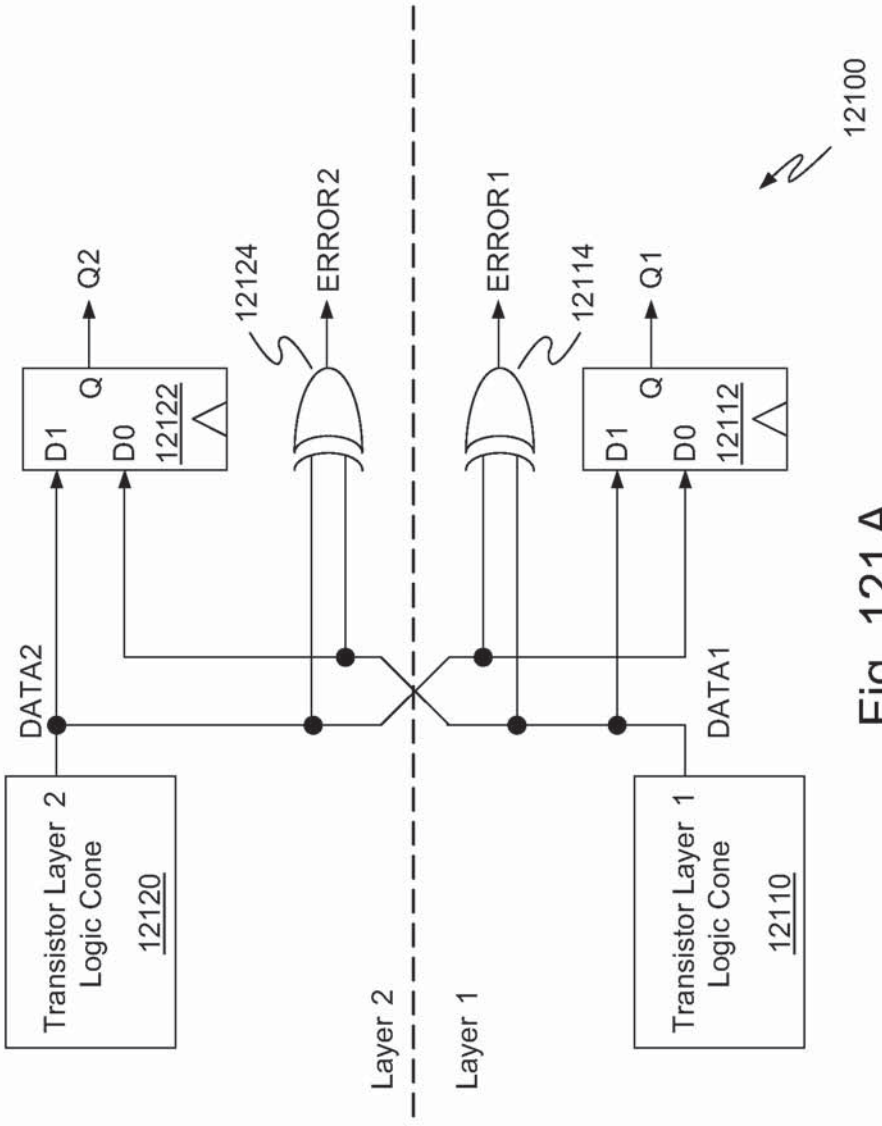

12100
Transistor Layer 2
Logic Cone
12120
Transistor Layer 1
Logic Cone
12110
DATA2
DATA1
Layer 2
Layer 1
D1
D0
Q
12122
12112
Q2
Q1
12124
12114
ERROR2
ERROR1

Fig. 121 A

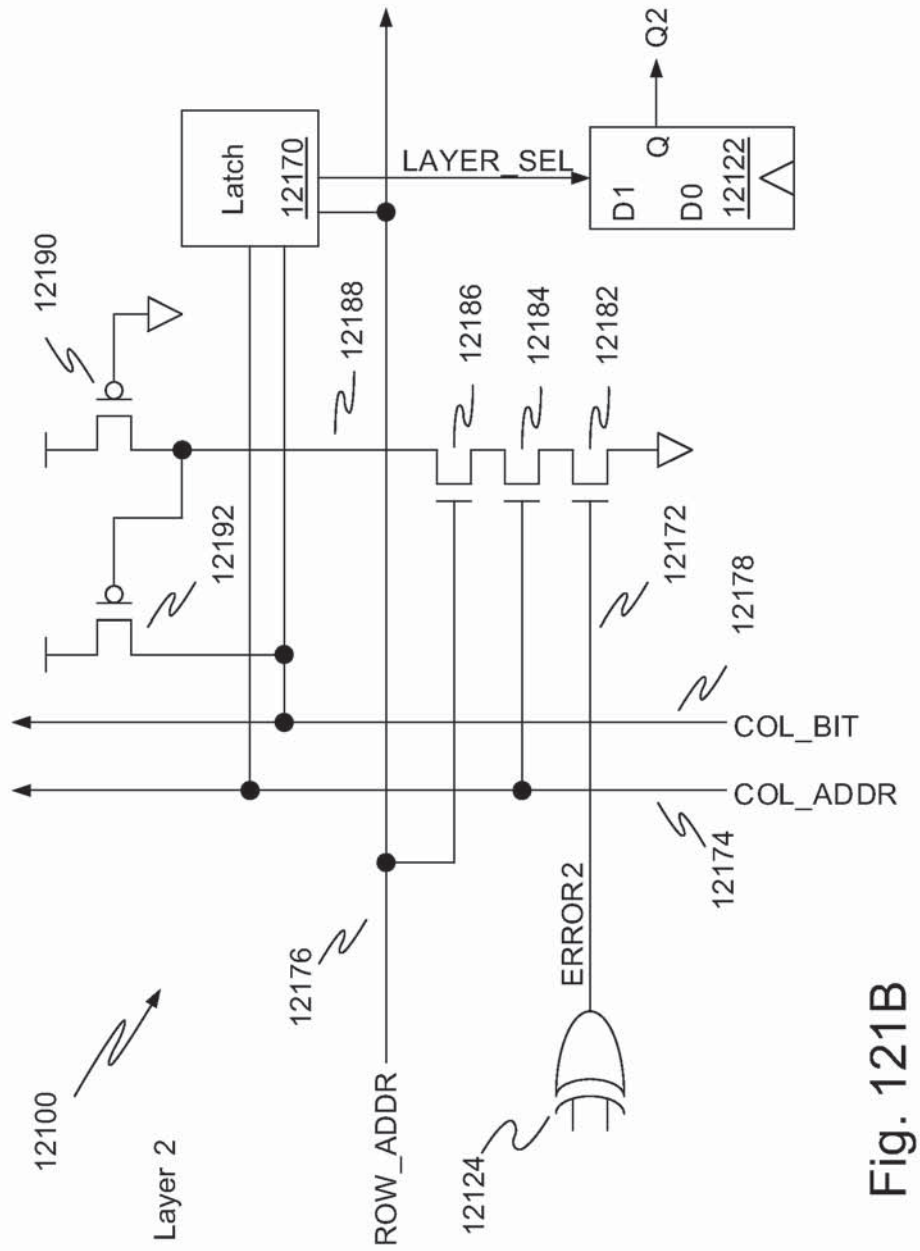

12100
Layer 2
12190
12192
12188
12186
12184
12182
12172
12178
12176
12174
12124
Latch
12170
LAYER_SEL
D1
Q
D0
12122
Q2
ROW_ADDR
COL_BIT
COL_ADDR
ERROR2

Fig. 121B

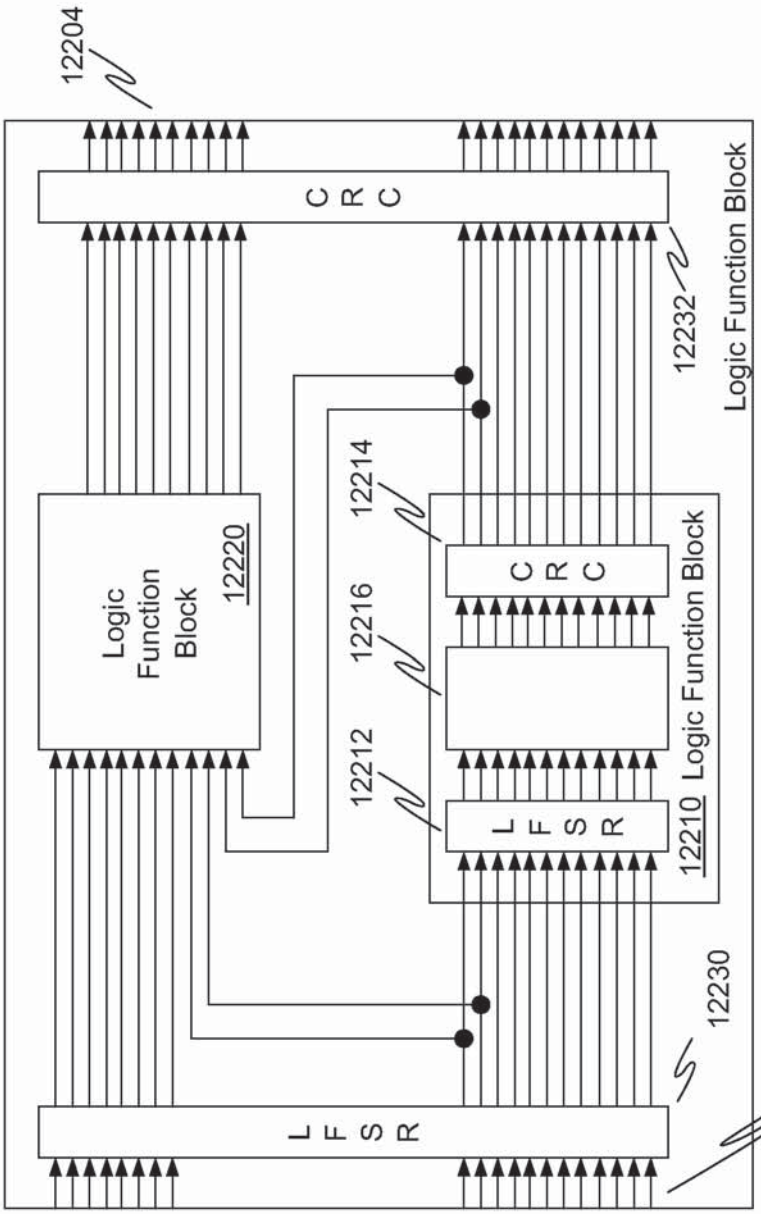

12204
C R C
12232
Logic Function Block
12200
Logic Function Block 12220
12214
12216
12212
C R C
L F S R
12210 Logic Function Block
12230
12202
L F S R

Fig. 122

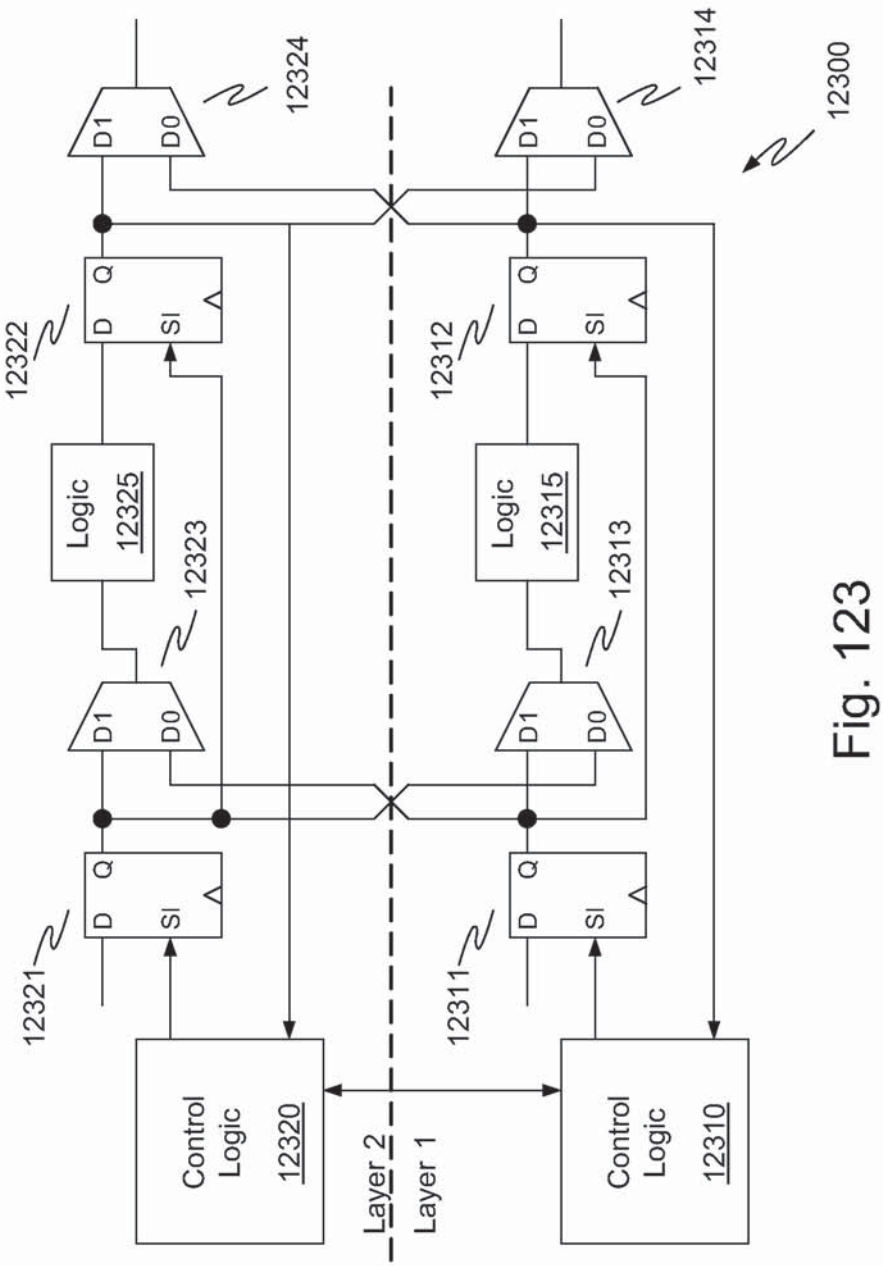

12300
12324
12314
12322
12312
12323
12313
12321
12311
Logic 12325
Logic 12315
Control Logic 12320
Control Logic 12310
Layer 2
Layer 1
D1
D0
D
Q
SI

Fig. 123

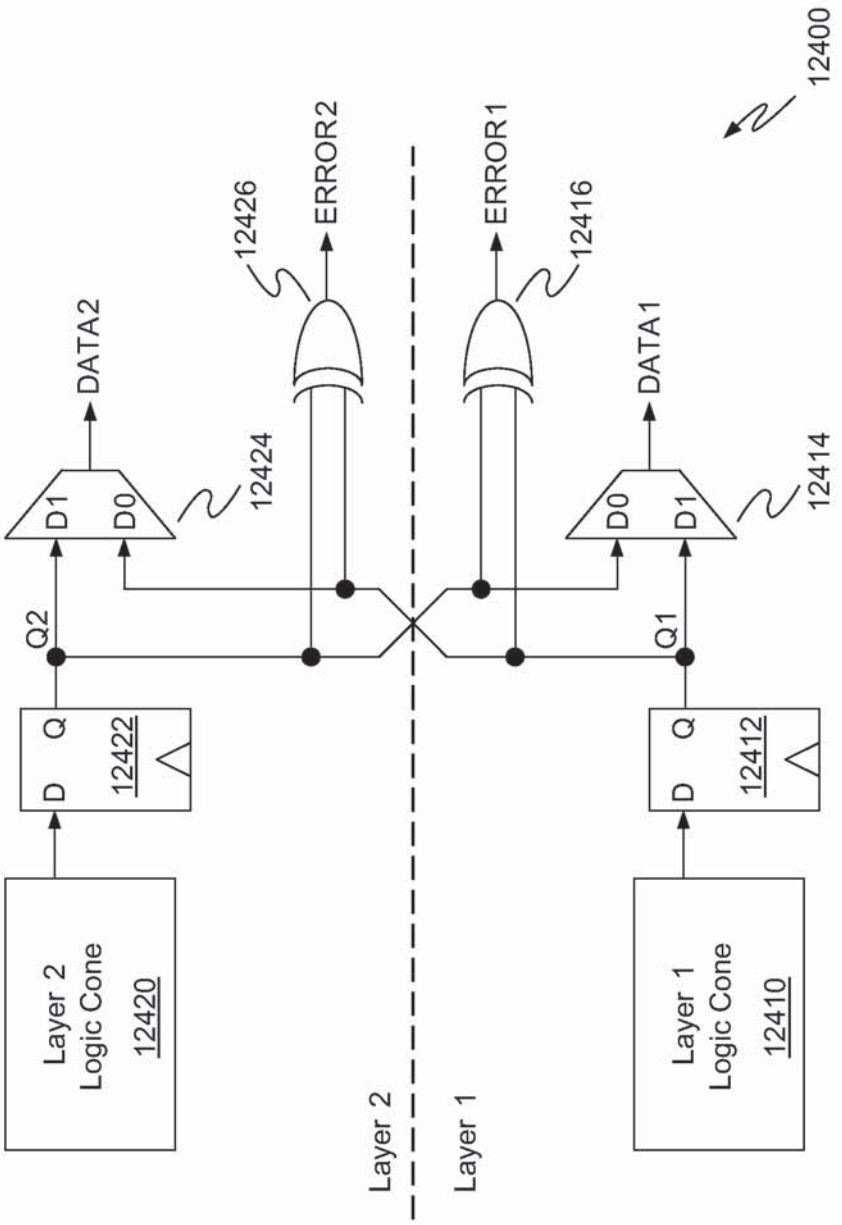

12400
ERROR2
ERROR1
12426
12416
DATA2
DATA1
12424
12414
D1
D0
D0
D1
Q2
Q1
D
Q
12422
D
Q
12412
Layer 2
Logic Cone
12420
Layer 1
Logic Cone
12410
Layer 2
Layer 1

Fig. 124

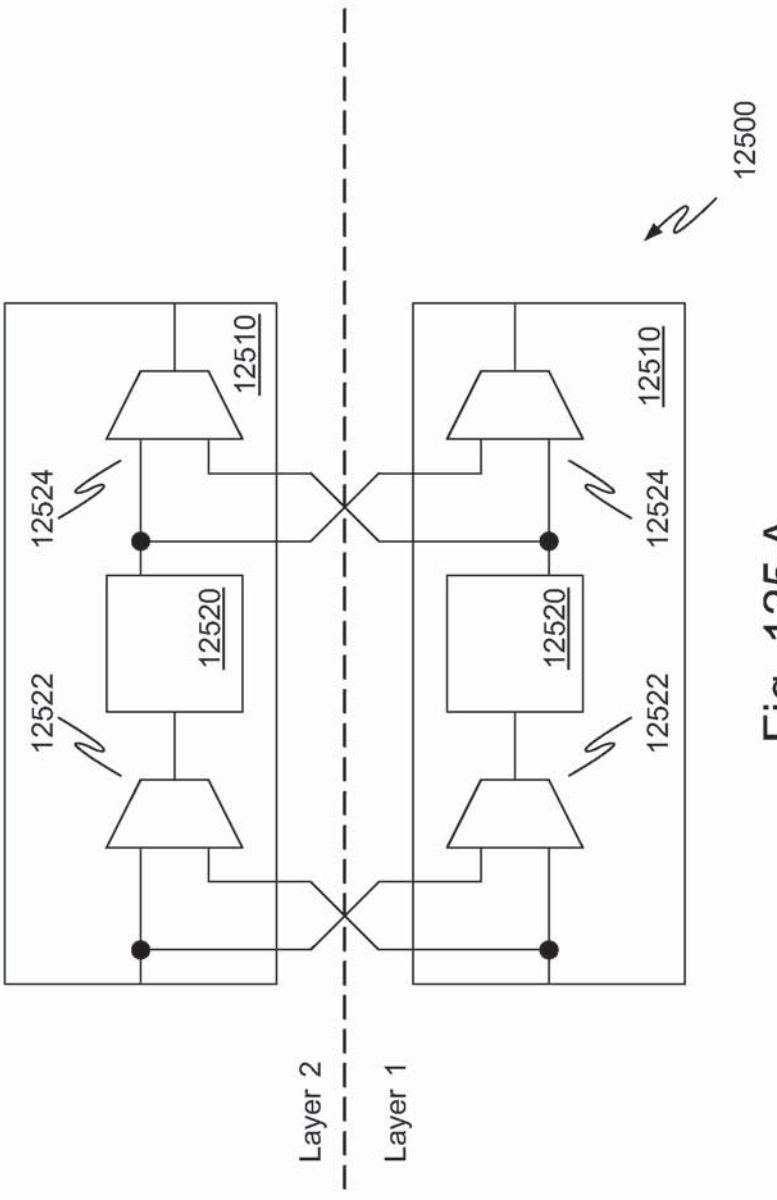

12500
12510
12524
12520
12522
12522
12520
12524
12510
Layer 2
Layer 1

Fig. 125A

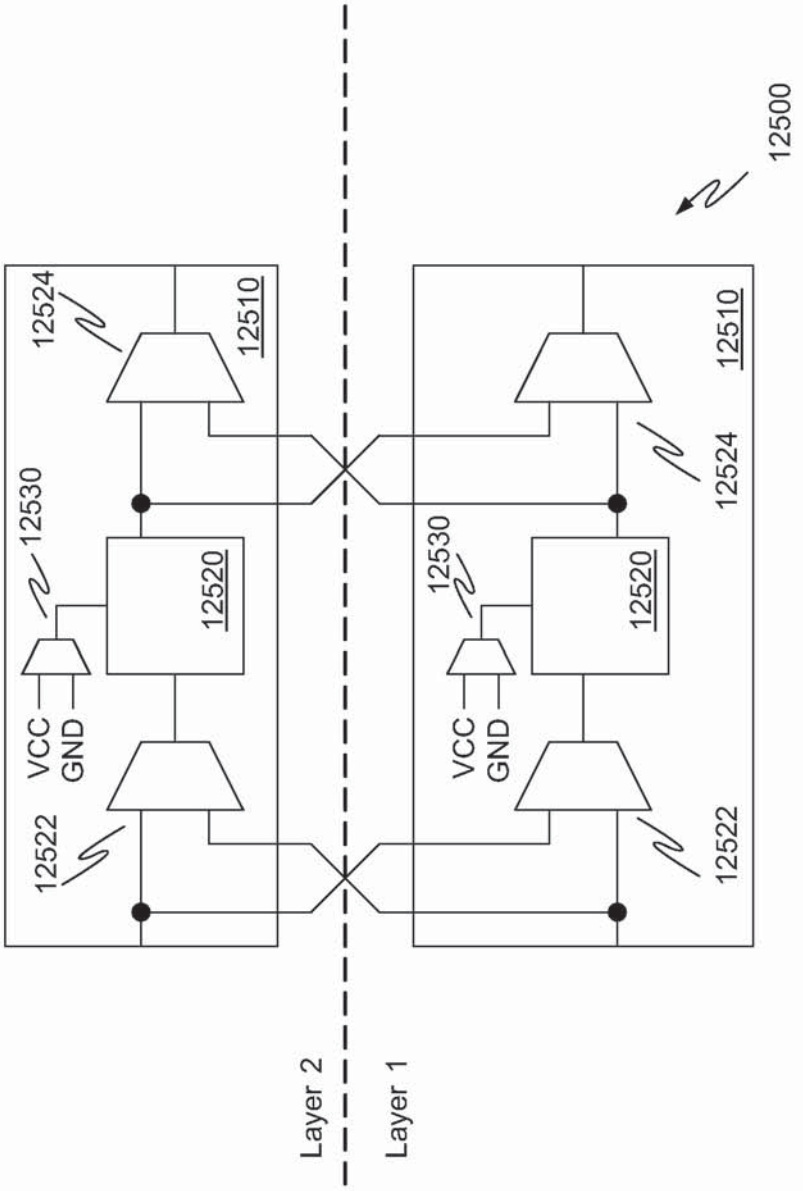


Fig. 125B

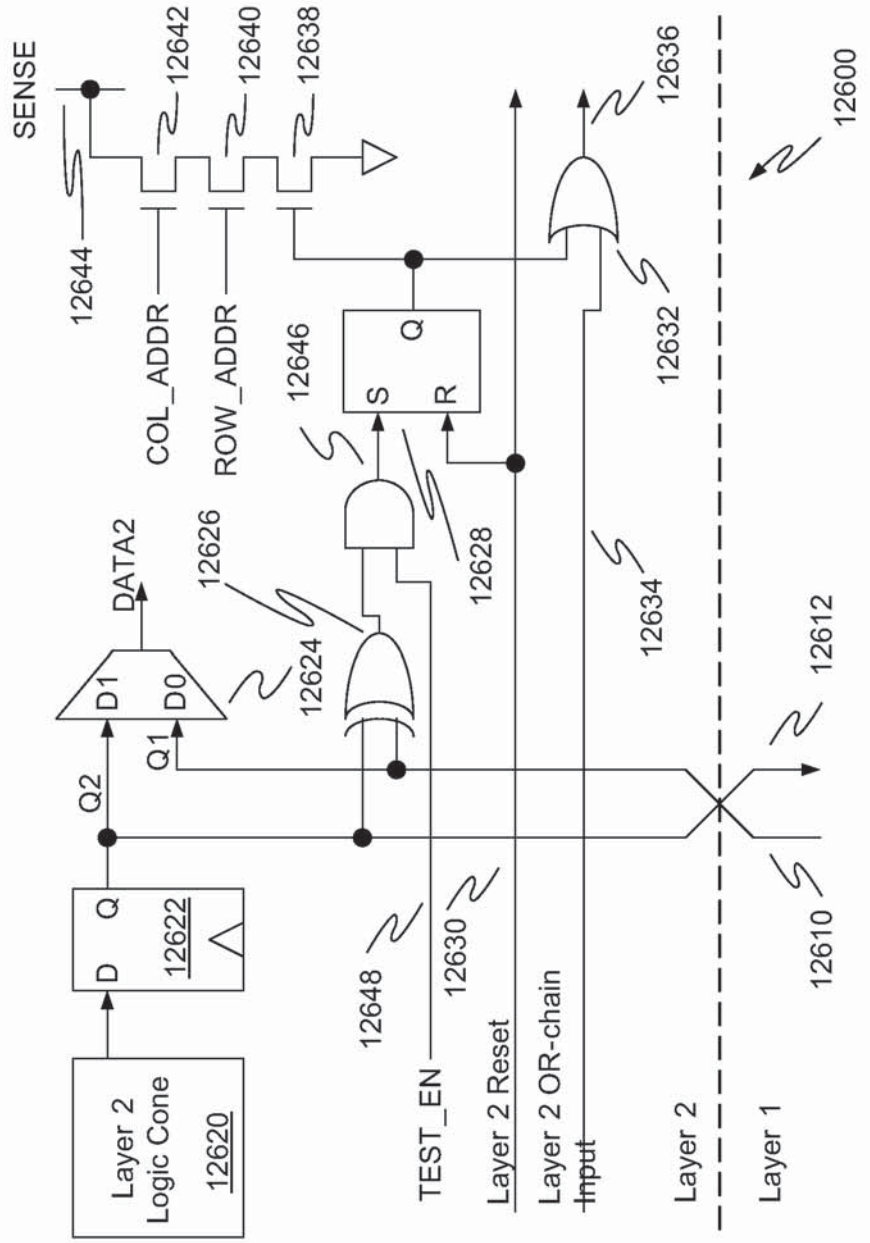

SENSE
12644
12642
12640
12638
COL_ADDR
ROW_ADDR
12646
S
R
Q
12636
12600
12632
12626
12624
12628
12634
DATA2
D1
D0
Q1
Q2
12612
Layer 2
Logic Cone
12620
D
Q
12622
12648
12630
12610
TEST_EN
Layer 2 Reset
Layer 2 OR-chain
Input
Layer 2
Layer 1

Fig. 126

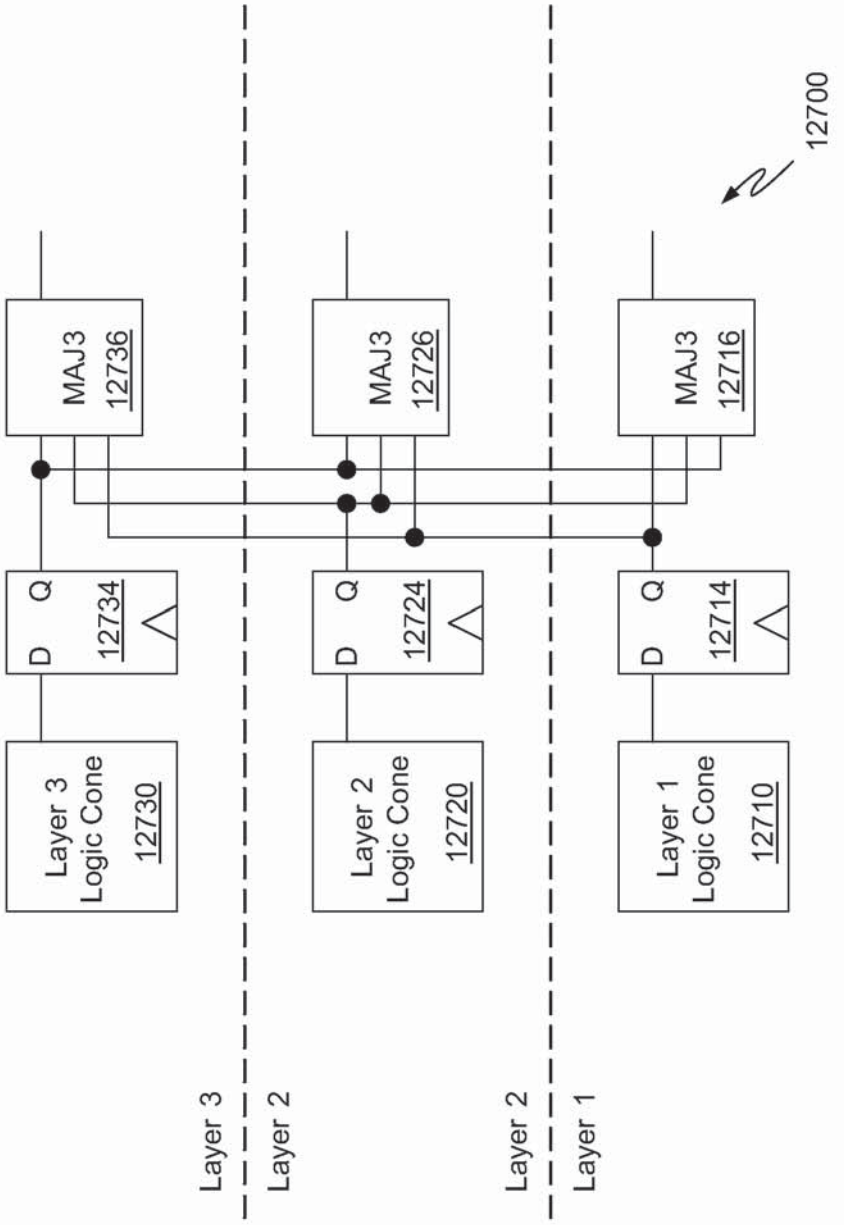

12700
MAJ3
12736
MAJ3
12726
MAJ3
12716
D
Q
12734
D
Q
12724
D
Q
12714
Layer 3
Logic Cone
12730
Layer 2
Logic Cone
12720
Layer 1
Logic Cone
12710
Layer 3
Layer 2
Layer 2
Layer 1

Fig. 127

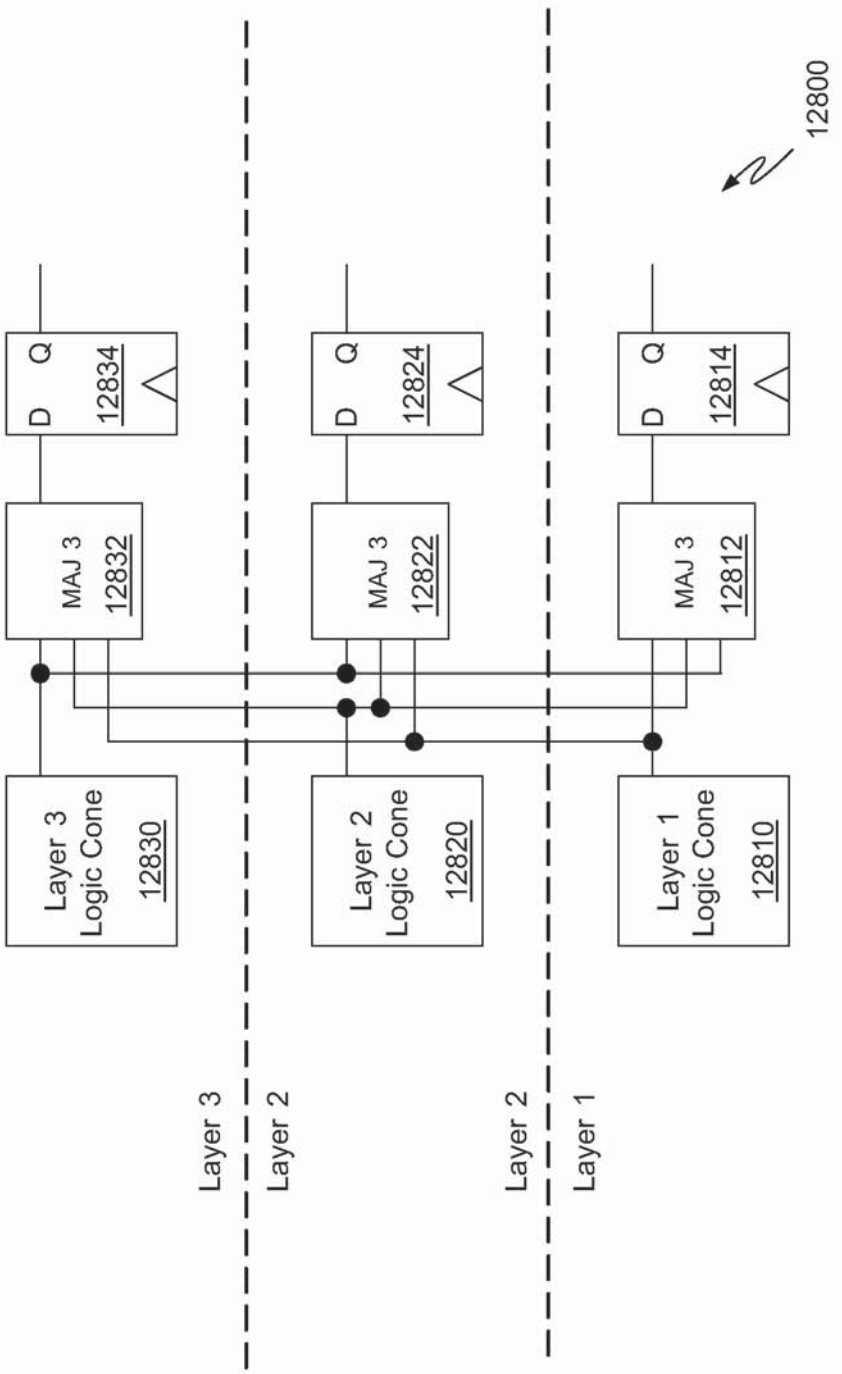

12800
Layer 3
Layer 2
Layer 2
Layer 1
Layer 3 Logic Cone 12830
Layer 2 Logic Cone 12820
Layer 1 Logic Cone 12810
MAJ 3 12832
MAJ 3 12822
MAJ 3 12812
D Q 12834
D Q 12824
D Q 12814

Fig. 128

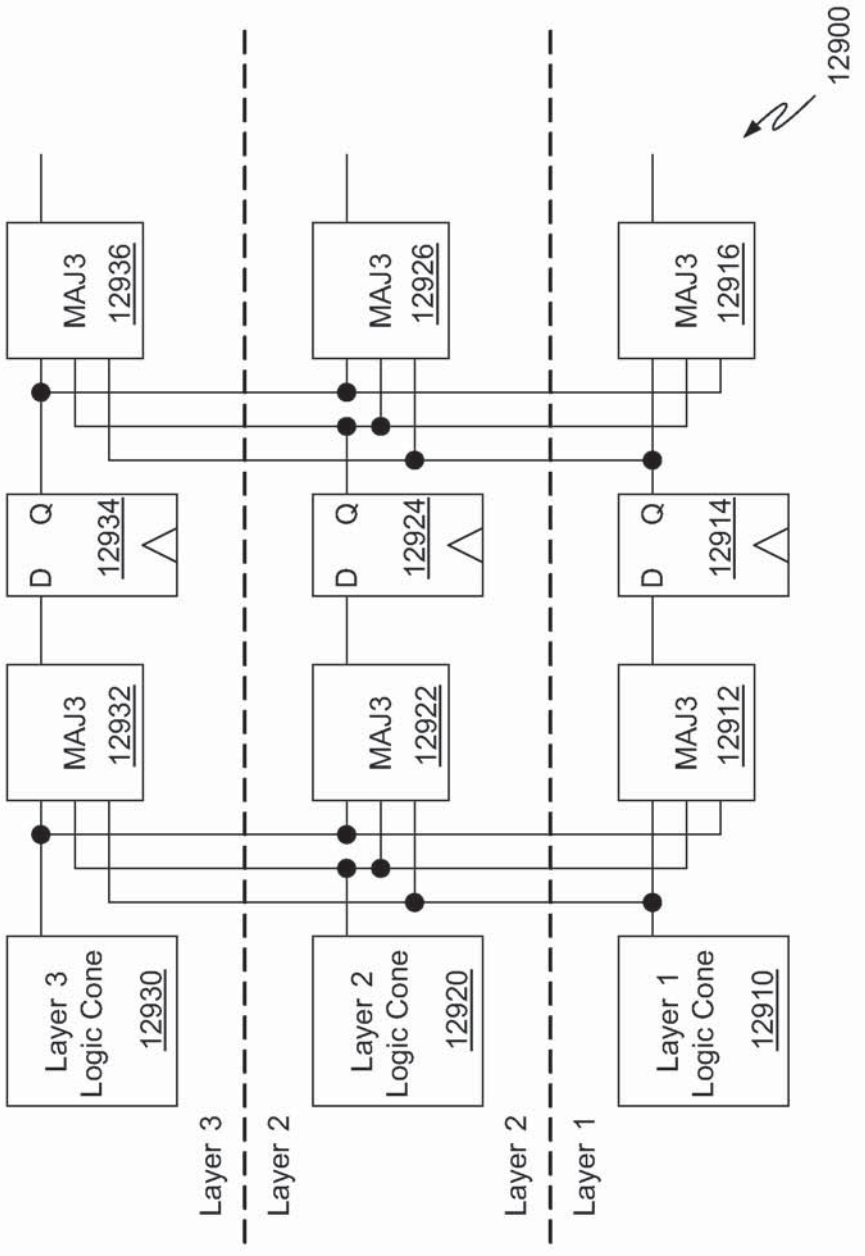

12900
MAJ3
12936
MAJ3
12926
MAJ3
12916
D Q
12934
D Q
12924
D Q
12914
MAJ3
12932
MAJ3
12922
MAJ3
12912
Layer 3
Logic Cone
12930
Layer 2
Logic Cone
12920
Layer 1
Logic Cone
12910
Layer 3
Layer 2
Layer 2
Layer 1

Fig. 129

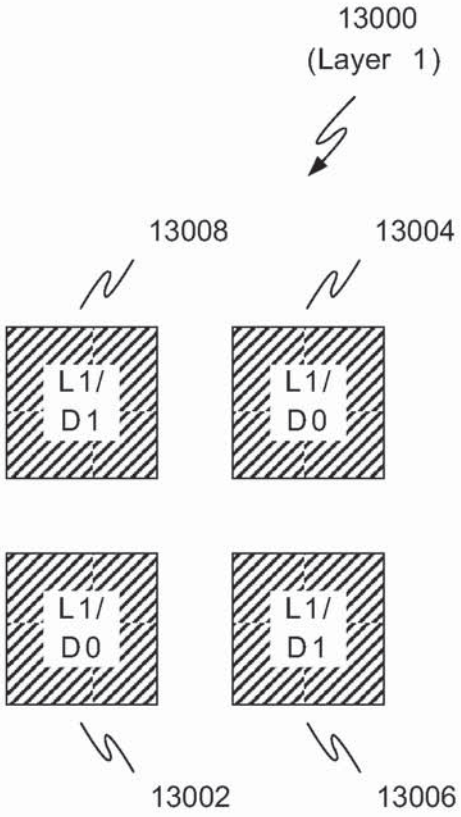


Fig. 130A

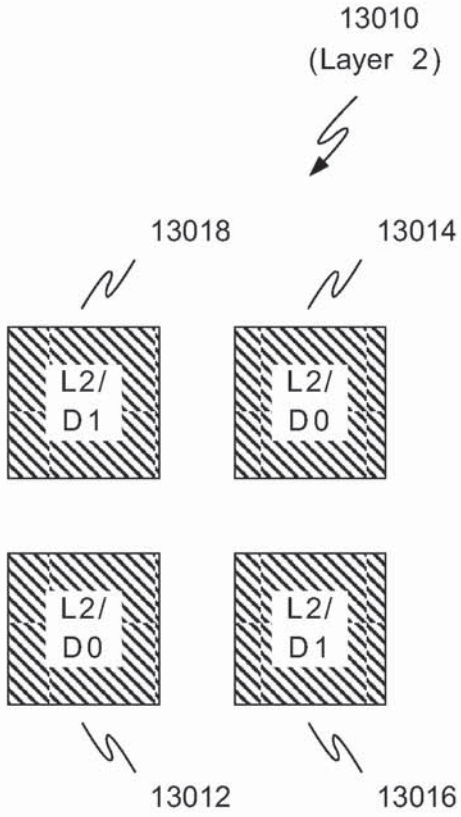


Fig. 130B

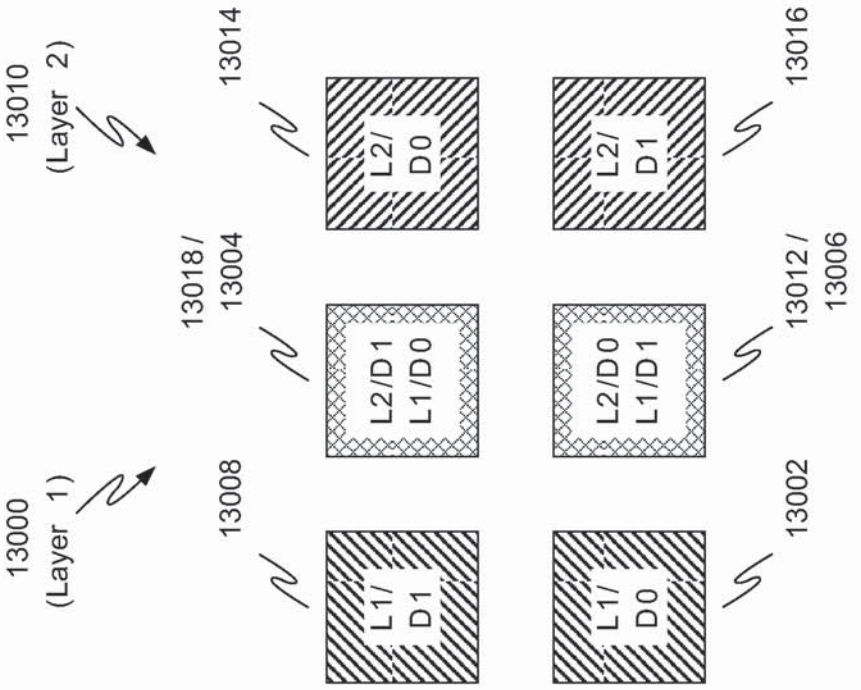

13000
(Layer 1)
13010
(Layer 2)
13008
13018 /
13004
13014
13002
13012 /
13006
13016
L1/
D1
L2/D1
L1/D0
L2/
D0
L1/
D0
L2/D0
L1/D1
L2/
D1

Fig. 130C

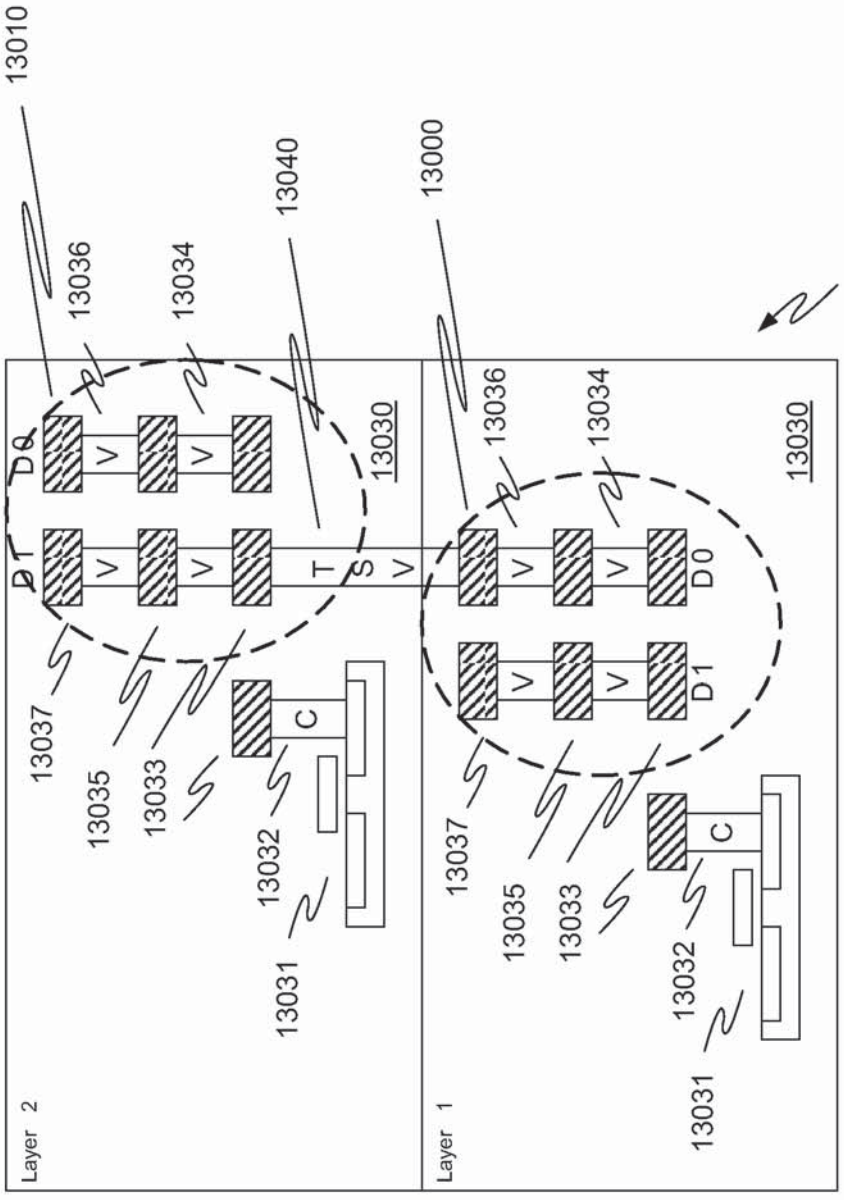

13010
13036
13034
13040
13000
13020
13030
DT
DQ
V
T
S
C
D0
D1
13037
13035
13033
13032
13031
Layer 2
Layer 1

Fig. 130D

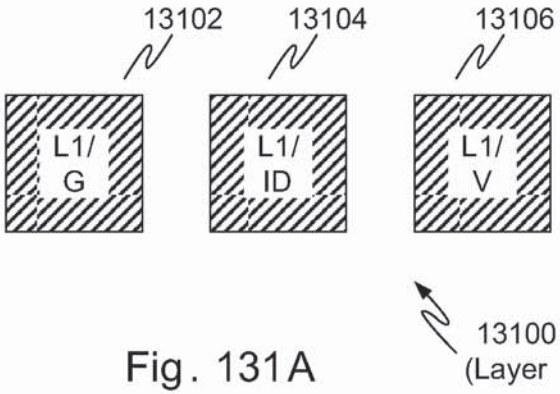


Fig. 131A

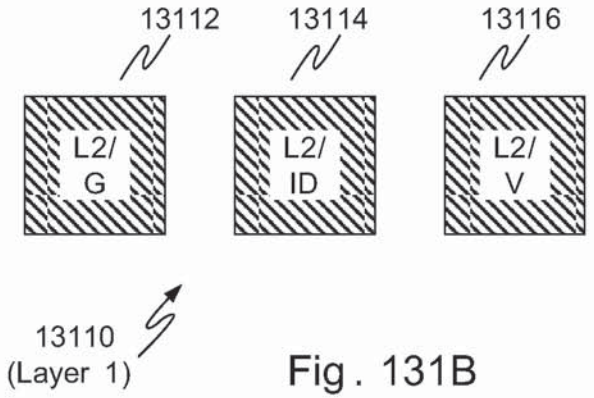


Fig. 131B

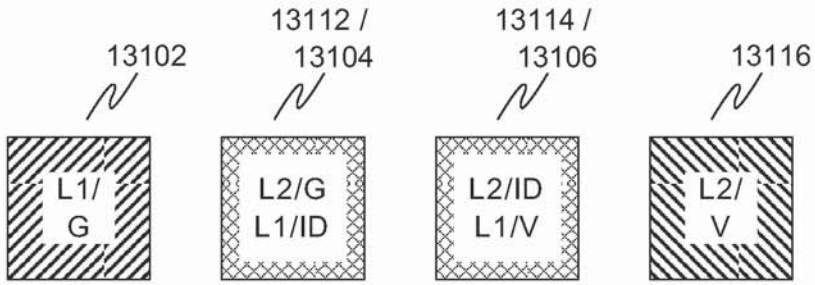


Fig. 131C

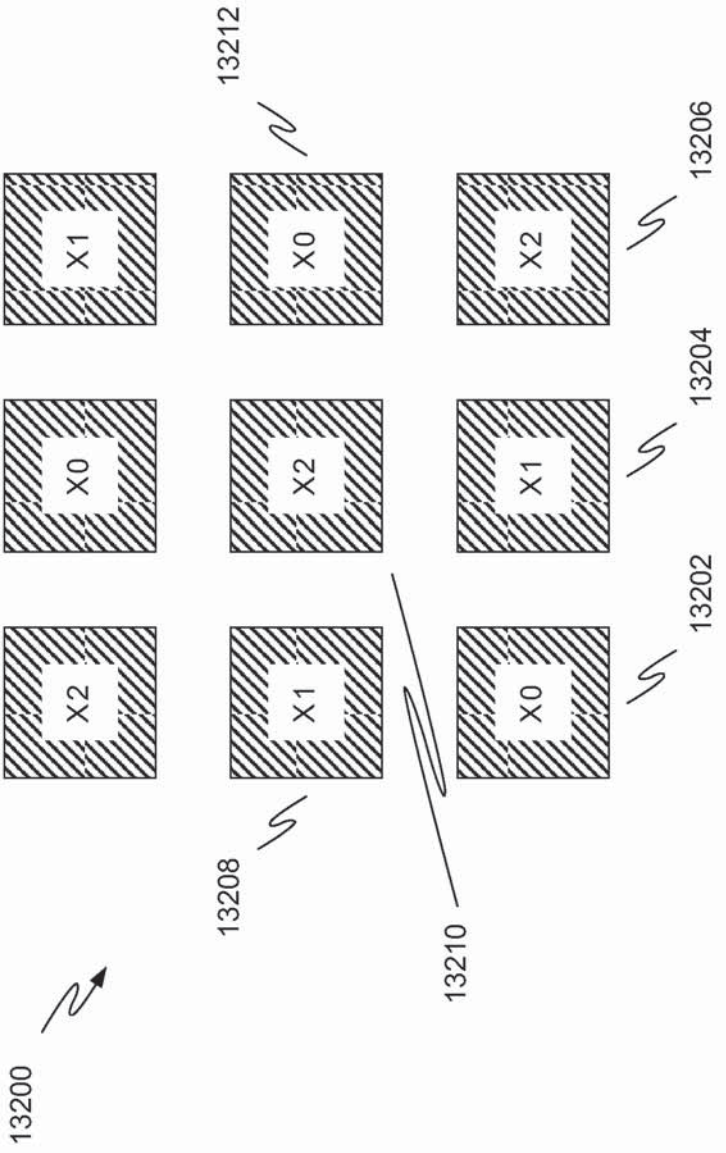

13200
13202
13204
13206
13208
13210
13212
13214
13216
13218
X0
X1
X2

Fig. 132A

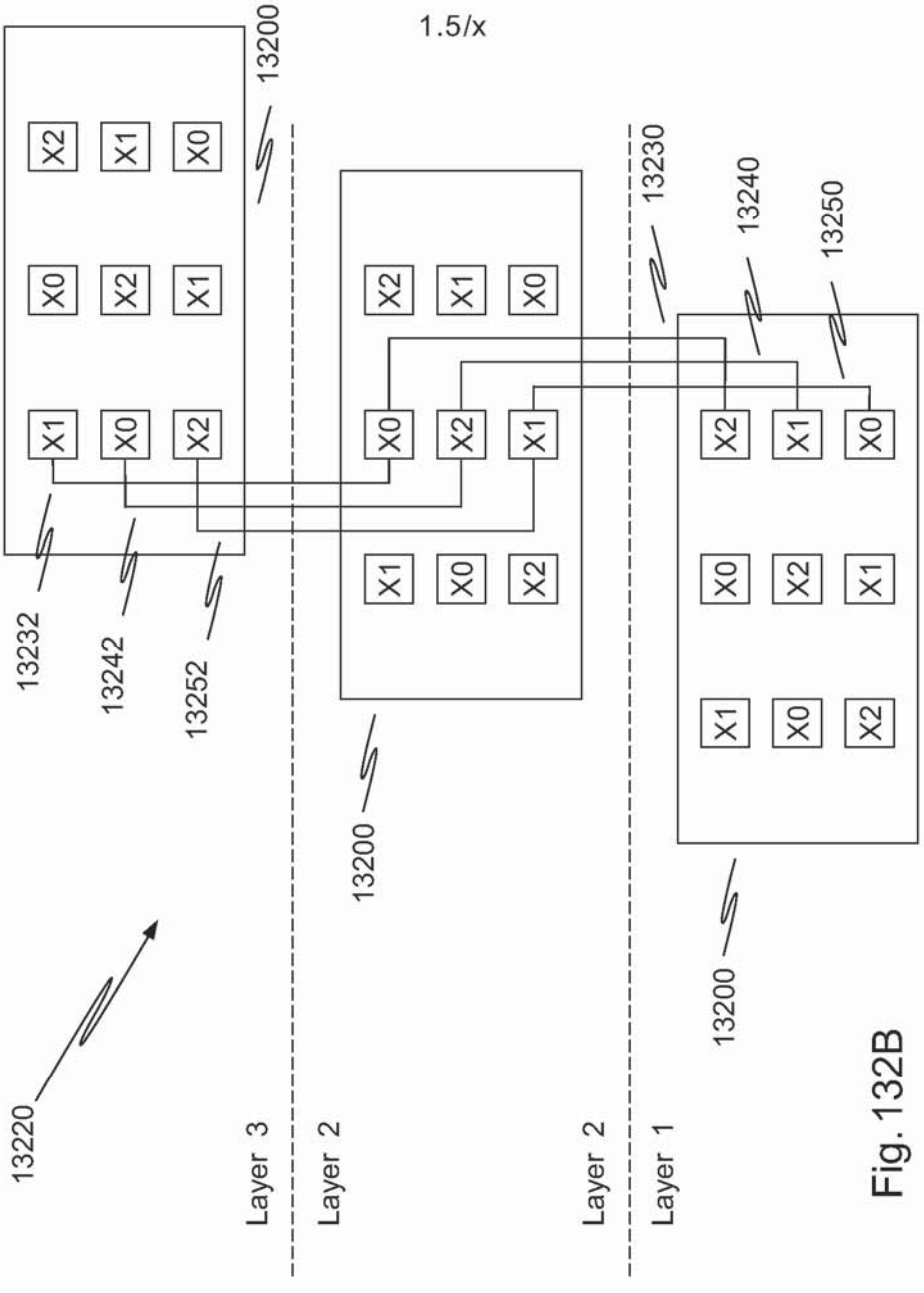

1.5/x
13200
13230
13240
13250
X2
X1
X0
13232
13242
13252
13220
Layer 3
Layer 2
Layer 2
Layer 1

Fig. 132B

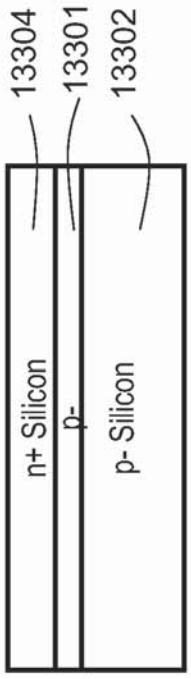


FIG. 133A

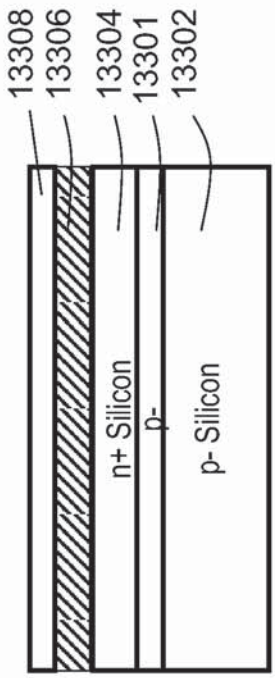


FIG. 133B

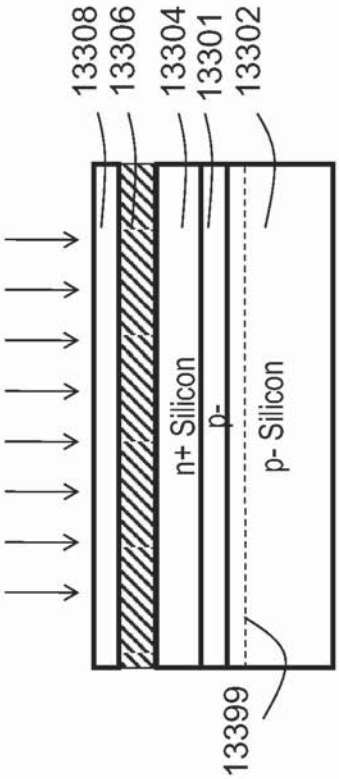


FIG. 133C

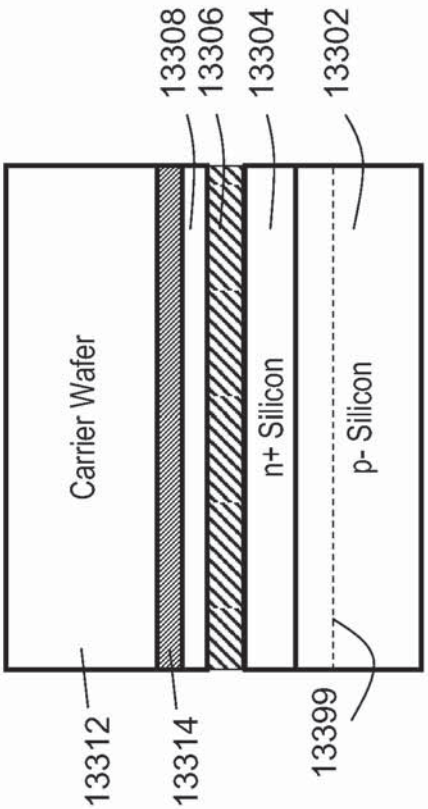

13308
13306
13304
13302
Carrier Wafer
n+ Silicon
p- Silicon
13312
13314
13399

FIG. 133D

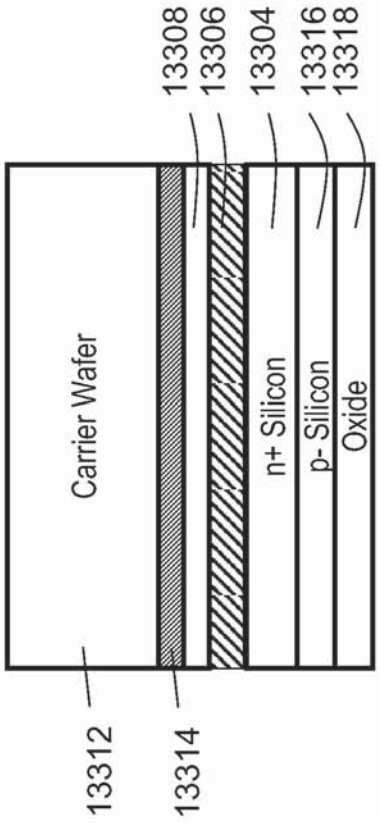

13308
13306
13304
13316
13318
Carrier Wafer
n+ Silicon
p- Silicon
Oxide
13312
13314

FIG. 133E

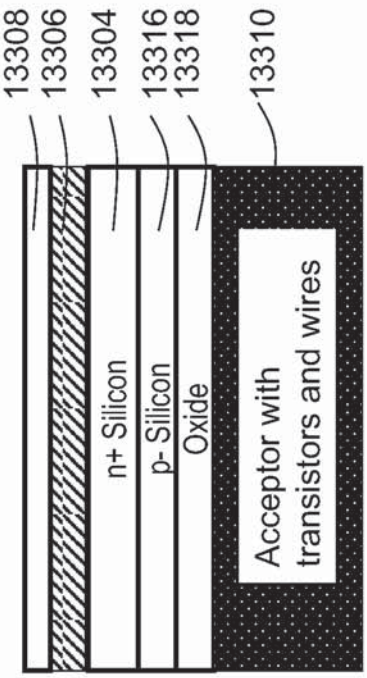

13308
13306
13304
13316
13318
13310
n+ Silicon
p- Silicon
Oxide
Acceptor with
transistors and wires

FIG. 133F

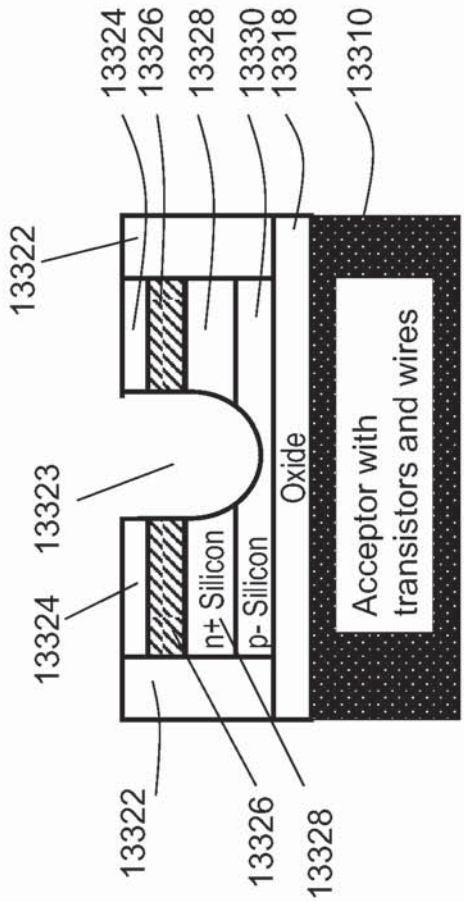

13324
13326
13328
13330
13318
13310
13322
13323
13324
n± Silicon
p- Silicon
Oxide
Acceptor with transistors and wires
13322
13326
13328

FIG. 133G

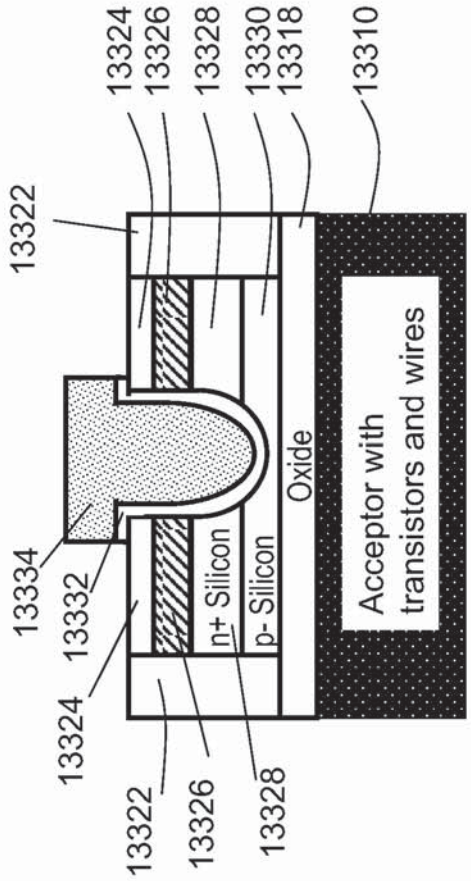

13324
13326
13328
13330
13318
13310
13322
Oxide
Acceptor with
transistors and wires
13334
13332
n+ Silicon
p- Silicon
13324
13322
13326
13328

FIG. 133H

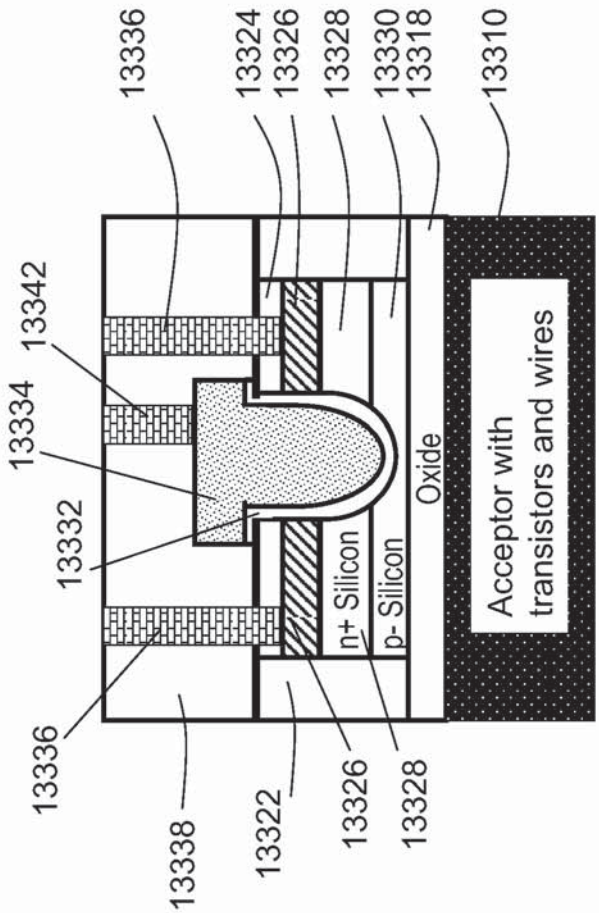

13336
13324
13326
13328
13330
13318
13310
13342
13334
13332
13336
13338
13322
13326
13328
n+ Silicon
p- Silicon
Oxide
Acceptor with
transistors and wires

FIG. 133I



FIG. 134A

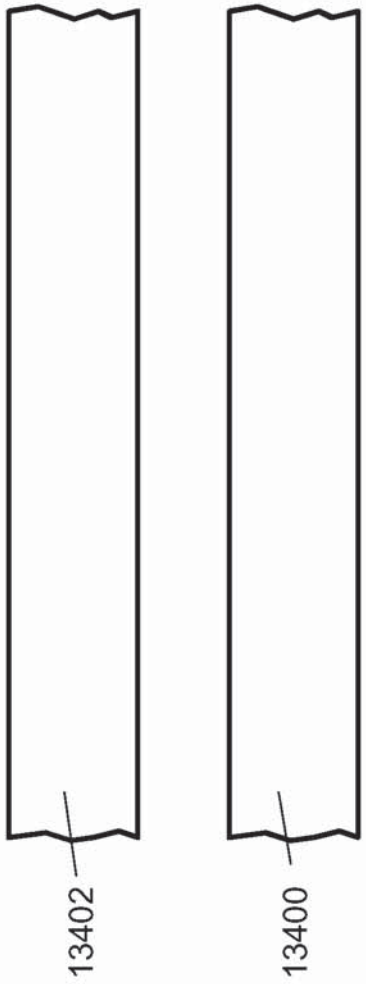


FIG. 134B

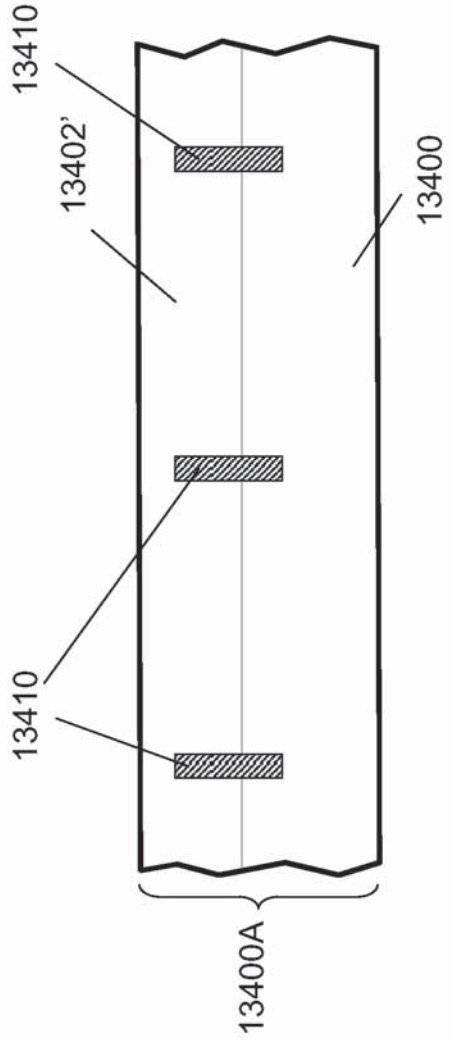


FIG. 134C

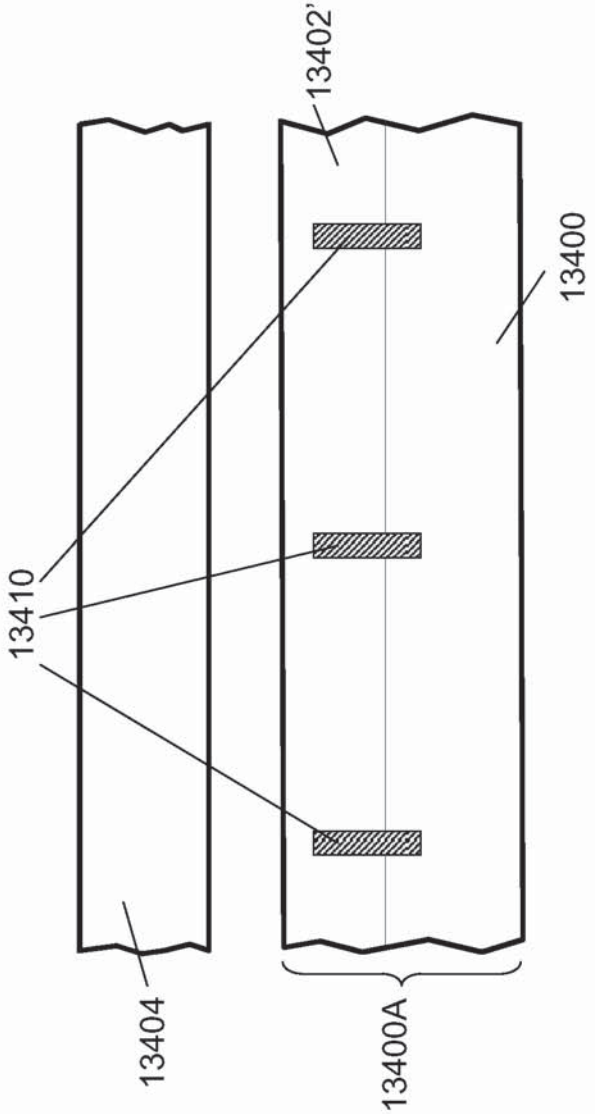


FIG. 134D

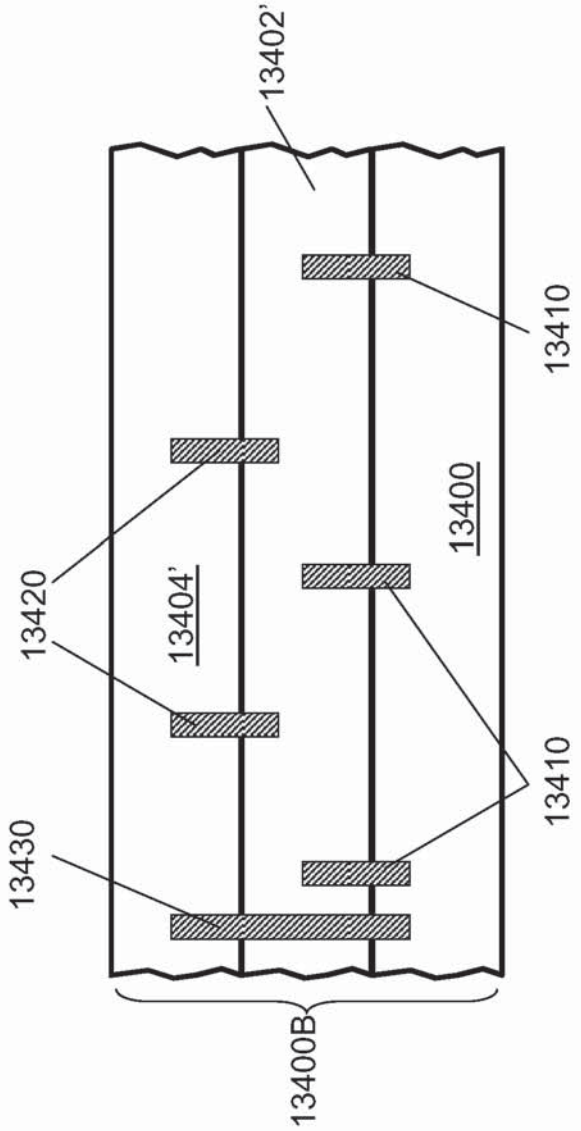


FIG. 134E

FIG. 134F

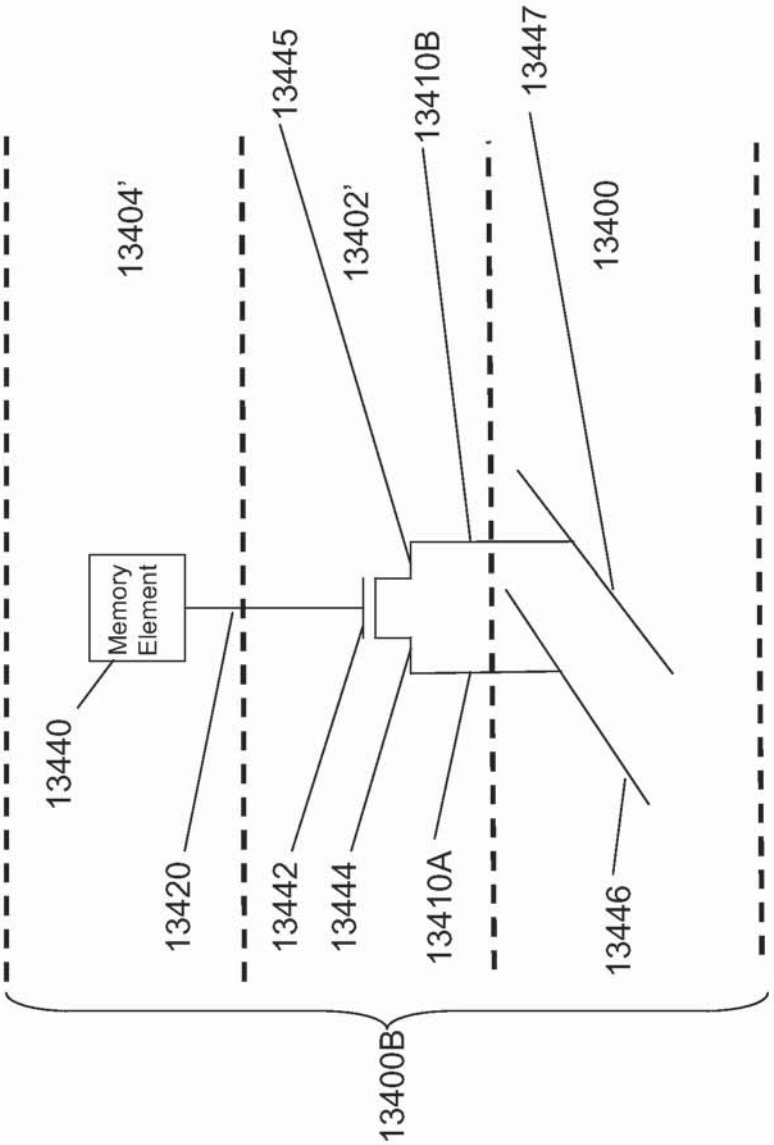

13400B
13440
Memory Element
13420
13442
13444
13410A
13446
13400
13402'
13404'
13445
13410B
13447



FIG. 135A

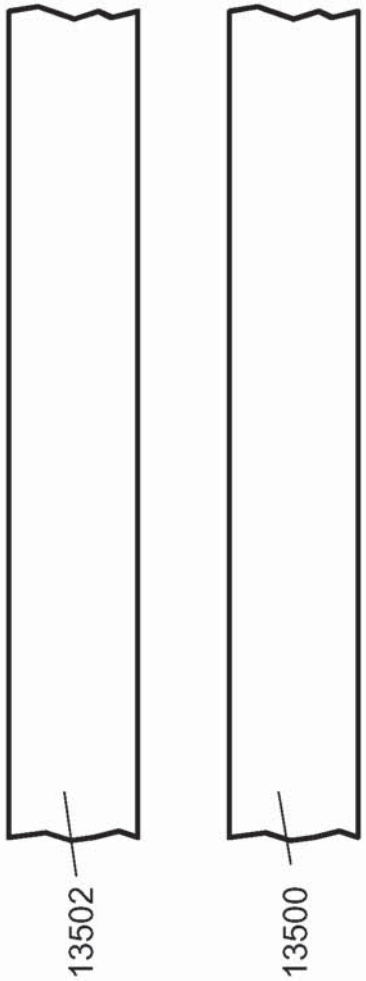


FIG. 135B

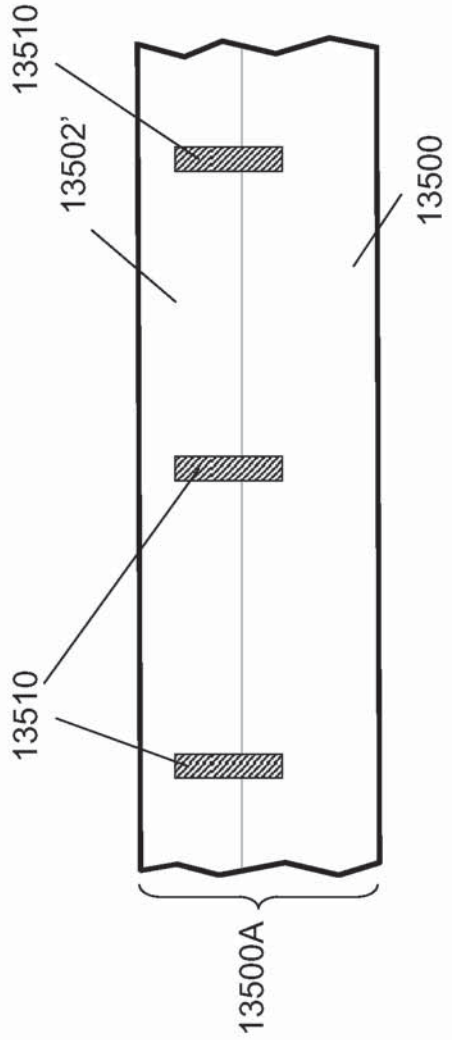
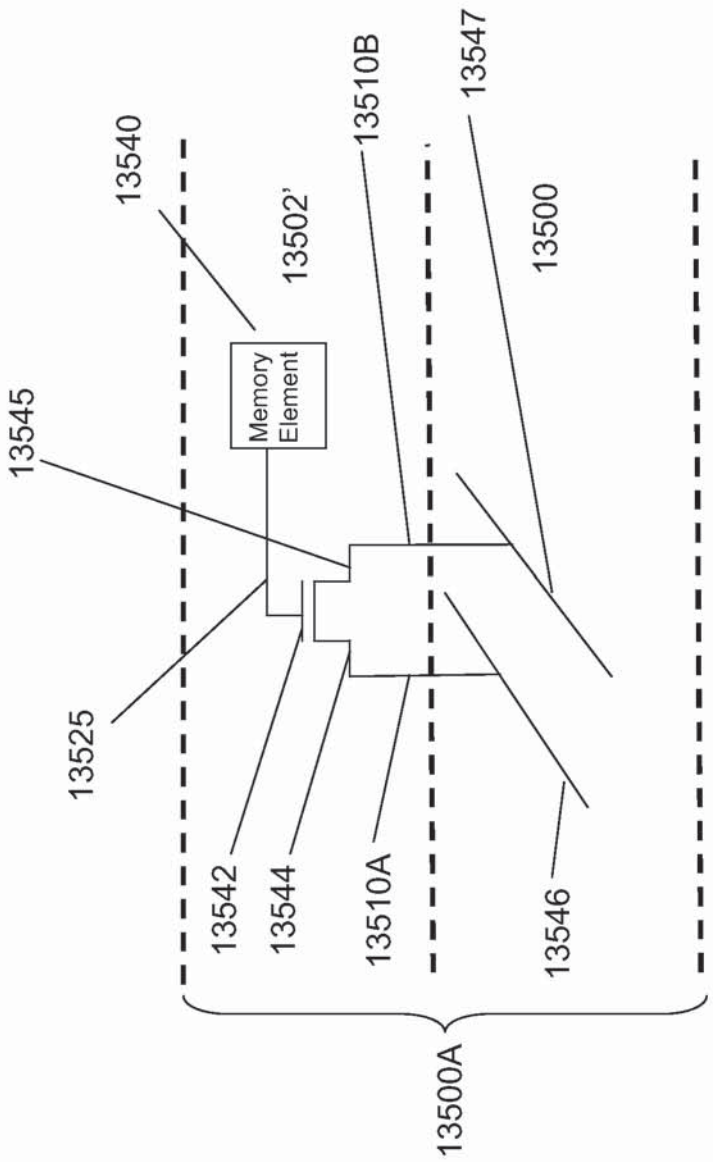


FIG. 135C

FIG. 135D


13545
13540
13502'
13510B
13547
13500
Memory Element
13525
13542
13544
13510A
13546
13500A

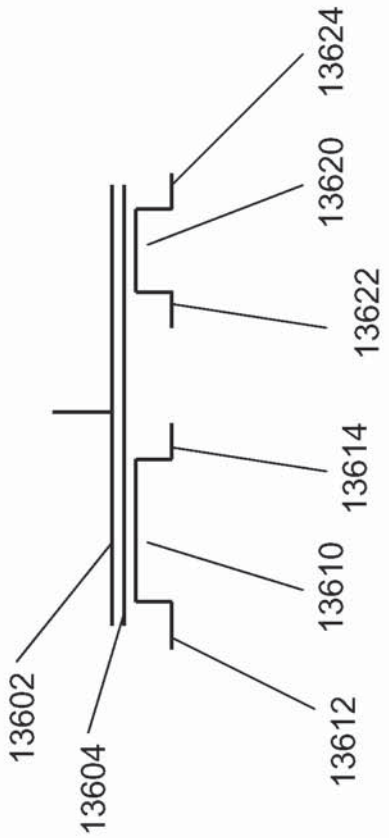


FIG. 136

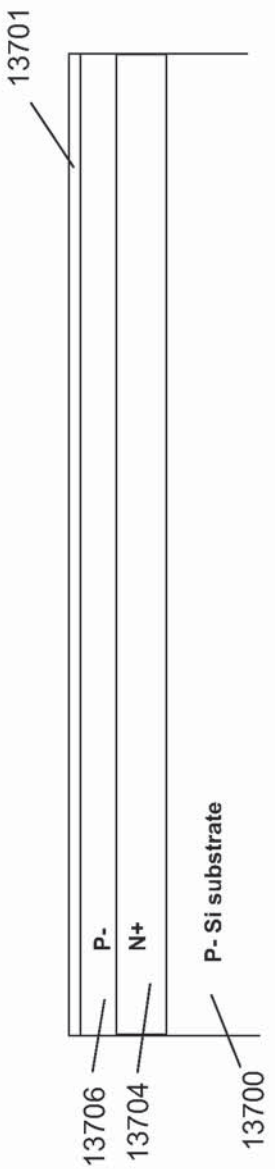


FIG. 137A

13707

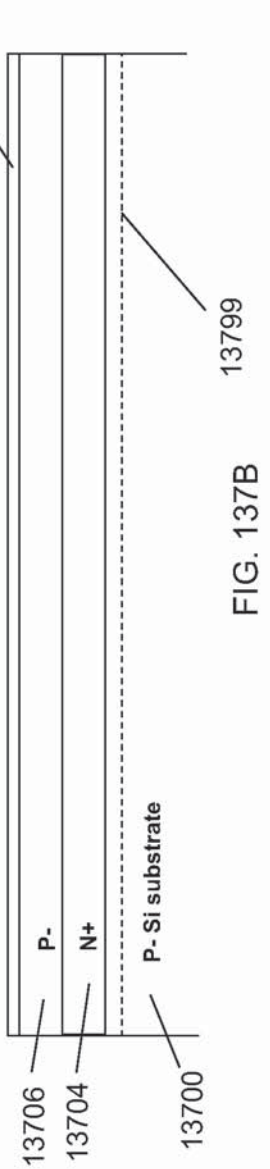


FIG. 137B

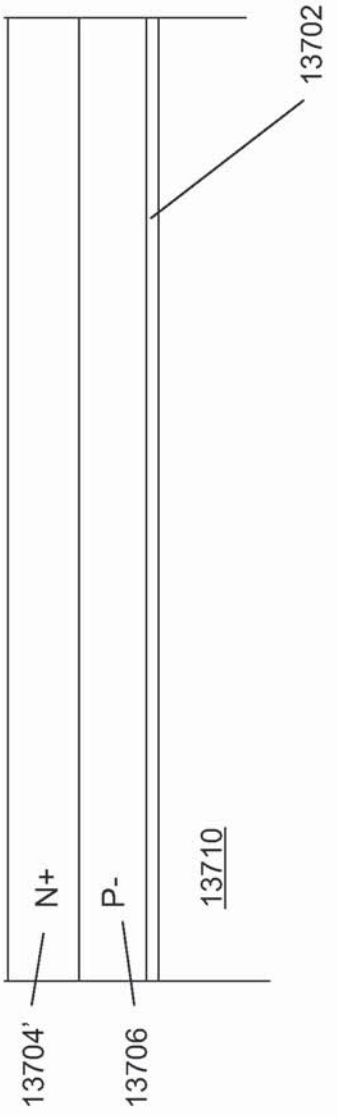


FIG. 137C

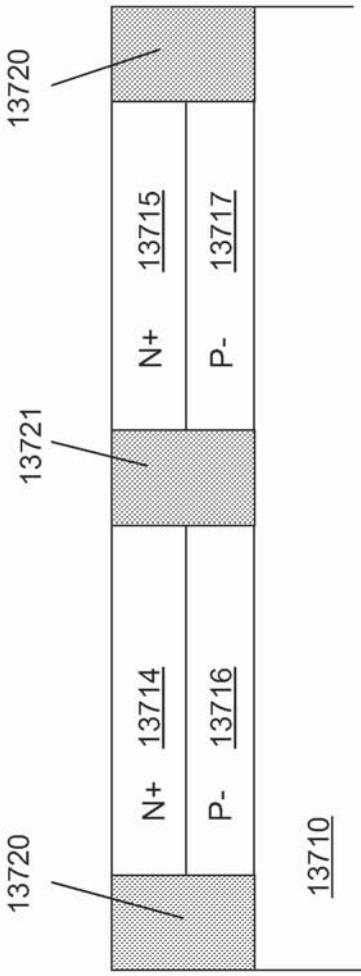


FIG. 137D

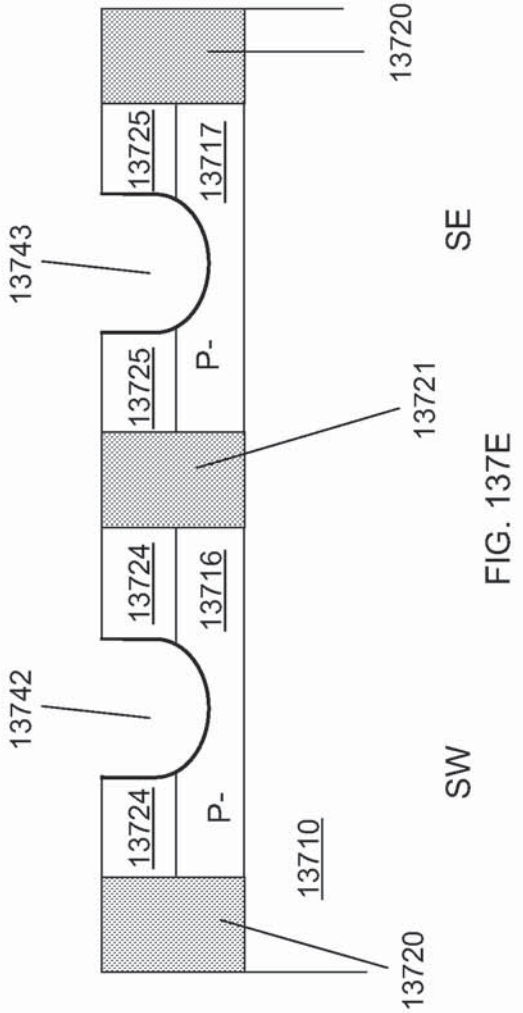

13720
13725
13717
13743
SE
13725
P-
13721
13724
13716
13742
13724
P-
SW
13710
13720

FIG. 137E

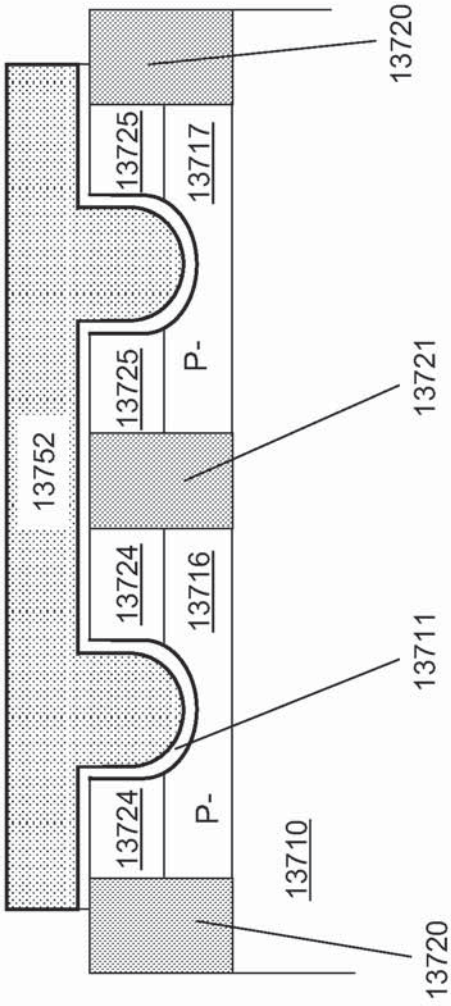

13720
13725
13717
13752
13725
P-
13721
13724
13716
13711
13724
P-
13710
13720
SW
SE

FIG. 137F

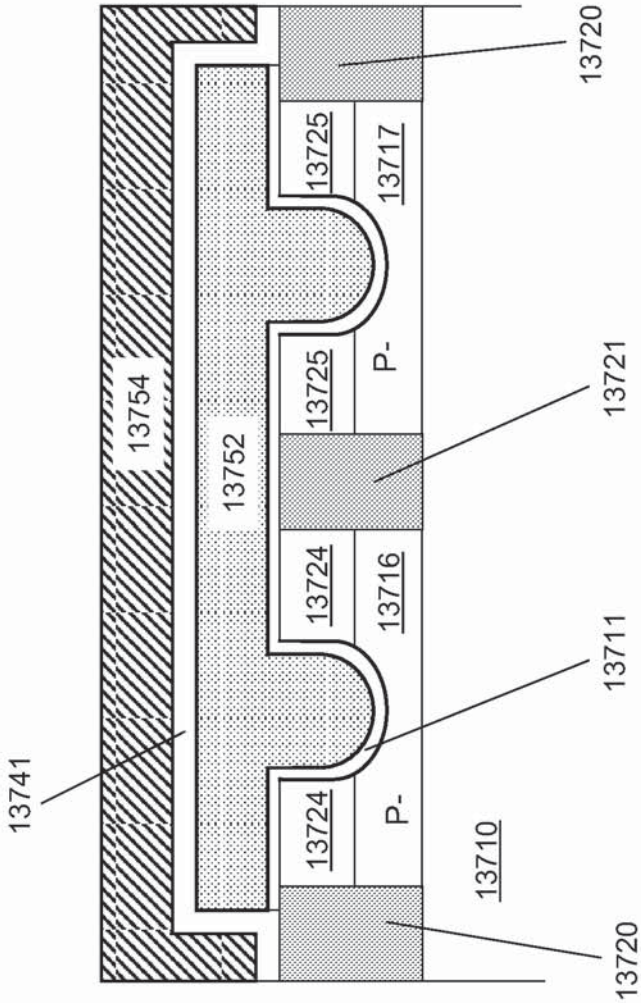

13741
13754
13752
13724
13724
13725
13725
13716
13717
P-
P-
13710
13711
13721
13720
13720
SW
SE

FIG. 137G