

Description

This invention concerns a clamping circuit for restoring the DC component of a video signal in a video signal processing and display system such as a television receiver including an image displaying kinescope. In particular, this invention concerns a circuit for clamping the video output signal of a wide bandwidth display driver amplifier.

A conventional television receiver for processing broadcast television signals, e.g., according to NTSC broadcast standards as used in the United States, is intended to process video signal with a bandwidth limited to approximately 4.2 MHz at the high frequency extreme. A display driver amplifier for an image displaying kinescope in such a system must exhibit a corresponding bandwidth capability. Also in such a system, the DC bias for the signal input electrode of the kinescope is often related to the output DC bias condition of the driver amplifier. The output DC bias may vary in accordance with the setting of an image brightness control of the system.

Recent trends toward high definition video signal display systems with significantly increased picture resolution capability, including high resolution television receivers and data display monitors, dictate the need for a video signal processing system with significantly wider signal bandwidth capability compared to conventional systems, and wide bandwidth display driver amplifiers in particular.

In a wideband display driver amplifier it is desirable to maintain a substantially fixed output DC bias condition for various reasons. Output bias variations such as produced in response to adjustment of bias controls including an image brightness control require a display driver operating supply voltage large enough to accommodate output DC level shifts associated with such adjustments. Large supply voltages are undesirable in a wideband display driver because of the resulting increased power consumption and dissipation which would result for a wideband driver which is often already operating at increased DC current levels. In addition, wideband driver transistors sometimes exhibit low voltage ratings which do not permit the use of a larger supply voltage required to accommodate DC output voltage shifts. Bias voltage variations also influence the capacitance parameters of the driver transistors, undesirably causing operating bandwidth variations with shifts in transistor DC bias. The driver transistor operating bandwidth capability also varies with the current gain of the transistor, which is a function of transistor bias current.

Consequently, wideband kinescope drivers often do not permit DC bias shifts such as would

otherwise be required for brightness control, for example, and often employ capacitor (AC) coupling between the output of the kinescope driver stage and the kinescope. Such capacitor coupling requires a circuit for DC restoration and brightness control at the signal input electrode (e.g., the cathode electrode) of the kinescope. One type of video output DC restoration circuit employing a keyed clamping diode is disclosed for example in US-A-4,285,008. Another example of such a DC restoration circuit is disclosed in US-A-4,178,610 utilising in one form of such circuit, a single transistor switch by which to couple the inputs of three chrominance amplifiers to respective clamping diodes during the horizontal retrace period.

Video output DC restoration circuits which employ a clamping diode exhibit one or more disadvantages. During active picture information intervals of the video signal the clamping diode is reverse biased. It exhibits a capacitance which can adversely affect the high frequency response of the video output signal path particularly in the case of a wideband system depending on the diode type and the magnitude of the reverse bias voltage across the diode. Diode clamping circuits are also subject to introducing a clamping error which is signal dependent. This error is related to an offset voltage produced by signal dependent clamping current flowing through an impedance in series with the clamping diode.

In GB-A-2,149,610 (having the same inventors as the present application) a DC restoration circuit is disclosed in which there is no clamping diode; instead, an amplifier with a feedback path has a tapping point in that path directly coupled to a coupling capacitor in the video signal path. The present invention, as set forth in Claim 1, provides a DC restoration circuit which also includes an amplifier with a tapped feedback path. However, the feedback tap is coupled to the video coupling capacitor through a diode, the feedback path is closed during the horizontal blanking interval so that the diode is conductive only during that interval, and resistors in the circuit effectively decouple the parasitic capacitance of the diode from the amplifier while the feedback path is open during image intervals.

In accordance with a preferred embodiment, the brightness of a displayed image can be adjusted by varying the level of current conducted by the feedback path when closed, such as in response to voltage derived from a viewer adjustable source of brightness potential, in a manner which does not contribute to the development of signal dependent clamping errors.

The sole FIGURE of the drawing illustrates a portion of a wideband video signal processing and display system, including a video output DC res-

toration clamping circuit in accordance with the principles of the present invention.

A video signal from a source 10 is applied to a wideband (e.g., 100MHz) video output kinescope driver amplifier 12, which provides a high level output video signal suitable for driving the cathode intensity control electrode 14 of an image displaying kinescope 15. The video output signal is conveyed from the output of display driver 12 to cathode 14 via an AC coupling capacitor 18 and a current limiting resistor 19. Display driver amplifier 12 may, for example, comprise a cascode amplifier with an input common emitter amplifier stage and an output common base amplifier stage, as known.

A DC restoration clamping network 20 for restoring the DC level of the video output signal which is AC coupled via capacitor 18, in accordance with the present invention, is coupled to capacitor 18 at a node A in a kinescope cathode signal coupling path including resistor 19. Network 20 includes a keyed clamping diode 22 with an anode electrode coupled to node A in the video output signal path. A source of positive bias potential VB is applied to the junction of series connected resistors 23 and 24 which are connected between the anode and cathode electrodes of diode 22 for providing bias thereto.

Network 20 also includes cascade connected, opposite conductivity type switching transistors 30 and 31. A base input electrode of transistor 30 receives fixed bias via a resistor 32 and a source of bias voltage (-12v.), a variable bias via a resistor 33 and a source of variable bias potential 34, and a keying signal VA including positive pulse keying components coupled via a diode 35. Transistor 30 normally exhibits a saturated conductive state whereby transistor 31 is rendered nonconductive. During clamping intervals, transistor 30 is caused to operate in a linear conduction region in response to the positive pulse components of signal VA, thereby rendering transistor 31 conductive.

In this example source 34 is a source of viewer adjustable brightness control potential for varying the brightness of a displayed image by varying the conduction of transistors 30 and 31 during clamping intervals when transistor 31 is rendered conductive in response to the positive pulse components of signal VA. Each positive pulse component of signal VA occurs during a clamping interval which in this case is the so-called "back porch" interval following the synchronizing pulse interval within each horizontal line blanking interval.

An emitter circuit of emitter follower transistor 30 includes a resistor 36. A collector output circuit of transistor 31 includes a decoupling resistor 37 which connects the collector output of transistor 31 to an output terminal B at the junction of resistor 24 and the cathode electrode of clamping diode 22. A

feedback resistor 38 coupled from terminal B to the base input of transistor 30 comprises a negative feedback loop also including transistors 30, 31 and decoupling resistor 37.

During clamping intervals when the positive pulse components of signal VA appear, normally conductive diode 35 is rendered nonconductive, transistor 30 changes from its normally saturated conductive condition to its linear conductive condition, resulting in normally nonconductive transistor 31 being rendered conductive. At this time a pulse component VC appears at the collector of transistor 31 and at terminal B. The magnitude of such pulse component may be on the order of +20 volts to +80 volts for example, as determined by the values of resistors 32, 33 and 38 and by the magnitude of the voltage from brightness control source 34. The setting of the brightness control in source 34 controls the conduction level of transistors 30 and 31. This in turn determines the magnitude of pulse component VC and the conduction level of clamp diode 22, for determining an image brightness related DC bias condition of the kinescope cathode signal path. Normally nonconductive clamping diode 22 is rendered conductive in response to clamping interval pulse VC such that the charge developed on capacitor 18 at node A is modified in accordance with the magnitude of clamping pulse VC. Thus the brightness related DC level of the cathode video signal path is clamped to a value in accordance with the value of the brightness control voltage from source 34.

Outside of the clamping intervals, i.e., during image trace intervals, diode 35 is forward biased into conduction by signal VA, and transistor 30 is in its normal saturated condition. At this time a voltage substantially equal to VB (+100 volts) appears at terminal B, thereby reverse biasing clamping diode 22. The bias provided to the cathode of clamping diode 22 during non-clamping intervals is chosen to be large enough to assure that clamp diode 22 remains reverse biased (cut-off) for any video signal conditions expected to appear at node A in the video signal path.

Such sufficient biasing of diode 22 outside of the clamping intervals avoids the need for special provisions in video circuits preceding display driver stage 12. Such provisions can include clipping circuits, to keep amplitude excursions of the video signal from extending too far in the blacker-than-black direction, which would otherwise tend to render clamp diode 22 conductive. The keying of network 20 assists to assure that clamping action occurs only during the clamping intervals. Keyed clamping also assists to prevent the clamp from being activated during non-clamping intervals such as in response to noise pulses which may occur during image trace intervals.

Loading of the video output cathode signal coupling path by parasitic capacitance CP of reverse biased clamping diode 22 is virtually eliminated during image information display (trace) intervals. At such times transistor 31 is nonconductive and the cathode electrode of clamp diode 22 is coupled to a high resistance, substantially non-capacitive source comprising resistor 24 and voltage source VB.

Specifically, at such times the feedback loop including transistors 30 and 31 and resistors 37 and 38 is open. The impedance at terminal B in the collector circuit of nonconductive transistor 31 is essentially determined by the value of resistor 24. The parasitic capacitance of clamp diode 22 is no longer coupled via a low impedance to an AC ground point. Instead it is connected to relatively high value decoupling resistor 24. This renders the parasitic capacitance of diode 22 ineffective with respect to the video signal path. Thus the high frequency characteristics of the video output signal is preserved. The value of resistor 24 should be larger than the impedance exhibited by parasitic capacitance CP at the highest video frequency of interest.

It is noted that resistor 37 serves to isolate, or decouple, a collector-to-base parasitic capacitance CP1 of transistor 31, and a collector-to-ground parasitic capacitance CP2 of transistor 31, from terminal B and clamp diode 22. In the absence of resistor 37, i.e., if the collector of transistor 31 were connected directly to terminal B, the video signal path would be loaded by the series combination of the collector capacitances of transistor 31 and the parasitic capacitance of diode 22. The value of resistor 37 should be larger than the impedance exhibited by parasitic capacitances CP1 and CP2 at the highest video frequencies of interest.

During clamping intervals when transistors 30 and 31 conduct and the feedback loop is closed, the cathode electrode of clamp diode 22 is coupled to a low impedance source at terminal B. This eliminates signal dependent clamping (offset) errors which would otherwise be developed due to signal dependent clamping current flowing through clamp diode 22 and any impedance in series with diode 22. Such low impedance at terminal B is approximately ten ohms or less and is produced by the feedback loop including transistors 30 and 31.

Decoupling resistor 37 is not "seen" by the clamping circuit including diode 22 and capacitor 18 during clamping intervals and does not contribute to the production of signal dependent clamping errors because resistor 37 is within the feedback loop also including elements 30, 31 and 38. The cathode of diode 22 sees only a low impedance. The desirable low impedance developed at terminal B during clamping intervals advantageous-

ly is not compromised as the brightness control in source 34, e.g., a potentiometer, is adjusted. The impedance at point B should be as low as possible. In this example the voltage at node B should be much smaller than 1.0 volt, as determined by the impedance at node B times the clamping current through diode 22.

Claims

1. A video signal DC restoration circuit, comprising:

a video driver amplifier having an input for receiving a video input signal having image and blanking intervals and having an output coupled to a first plate of a capacitor having a second plate coupled to a kinescope; a DC restoration amplifier to which blanking and brightness control signals are applied and having a feedback path including first and second resistors connected in series between output and input terminals of said amplifier; and a circuit path connected between a junction of said resistors and said second plate of said capacitor, characterized in that:

said DC restoration amplifier (30,31) includes an output transistor (31) having a first operating mode responsive to the presence of said blanking signal in which said feedback path is closed for providing an output signal proportional to said brightness control signal and having a second operating mode responsive to the absence of said blanking signal for operating in a non-conductive state in which said feedback path is opened;

said circuit path includes a diode (22) having an anode coupled to said second plate (A) of said capacitor (18) and having a cathode coupled to said junction (B), said diode having a parasitic capacitance (CP) associated therewith;

said junction (B) of said first (37) and second (38) resistors is coupled via a third resistor to a source of bias potential (VB); and

said diode being rendered conductive during said blanking interval in response to closure of said feedback path for applying a DC restoration voltage to said capacitor proportional to said brightness control voltage provided by said amplifier, said diode being rendered non-conductive during said image interval in response to opening of said feedback path, said parasitic capacitance being effectively decoupled from said amplifier by said first and second resistors and being effectively decoupled from said source of bias potential by said

Loading of the video output cathode signal coupling path by parasitic capacitance CP of reverse biased clamping diode 22 is virtually eliminated during image information display (trace) intervals. At such times transistor 31 is nonconductive and the cathode electrode of clamp diode 22 is coupled to a high resistance, substantially non-capacitive source comprising resistor 24 and voltage source VB.

Specifically, at such times the feedback loop including transistors 30 and 31 and resistors 37 and 38 is open. The impedance at terminal B in the collector circuit of nonconductive transistor 31 is essentially determined by the value of resistor 24. The parasitic capacitance of clamp diode 22 is no longer coupled via a low impedance to an AC ground point. Instead it is connected to relatively high value decoupling resistor 24. This renders the parasitic capacitance of diode 22 ineffective with respect to the video signal path. Thus the high frequency characteristics of the video output signal is preserved. The value of resistor 24 should be larger than the impedance exhibited by parasitic capacitance CP at the highest video frequency of interest.

It is noted that resistor 37 serves to isolate, or decouple, a collector-to-base parasitic capacitance CP1 of transistor 31, and a collector-to-ground parasitic capacitance CP2 of transistor 31, from terminal B and clamp diode 22. In the absence of resistor 37, i.e., if the collector of transistor 31 were connected directly to terminal B, the video signal path would be loaded by the series combination of the collector capacitances of transistor 31 and the parasitic capacitance of diode 22. The value of resistor 37 should be larger than the impedance exhibited by parasitic capacitances CP1 and CP2 at the highest video frequencies of interest.

During clamping intervals when transistors 30 and 31 conduct and the feedback loop is closed, the cathode electrode of clamp diode 22 is coupled to a low impedance source at terminal B. This eliminates signal dependent clamping (offset) errors which would otherwise be developed due to signal dependent clamping current flowing through clamp diode 22 and any impedance in series with diode 22. Such low impedance at terminal B is approximately ten ohms or less and is produced by the feedback loop including transistors 30 and 31.

Decoupling resistor 37 is not "seen" by the clamping circuit including diode 22 and capacitor 18 during clamping intervals and does not contribute to the production of signal dependent clamping errors because resistor 37 is within the feedback loop also including elements 30, 31 and 38. The cathode of diode 22 sees only a low impedance. The desirable low impedance developed at terminal B during clamping intervals advantageous-

ly is not compromised as the brightness control in source 34, e.g., a potentiometer, is adjusted. The impedance at point B should be as low as possible. In this example the voltage at node B should be much smaller than 1.0 volt, as determined by the impedance at node B times the clamping current through diode 22.

Claims

1. A video signal DC restoration circuit, comprising:

a video driver amplifier having an input for receiving a video input signal having image and blanking intervals and having an output coupled to a first plate of a capacitor having a second plate coupled to a kinescope; a DC restoration amplifier to which blanking and brightness control signals are applied and having a feedback path including first and second resistors connected in series between output and input terminals of said amplifier; and a circuit path connected between a junction of said resistors and said second plate of said capacitor; characterized in that:

said DC restoration amplifier (30,31) includes an output transistor (31) having a first operating mode responsive to the presence of said blanking signal in which said feedback path is closed for providing an output signal proportional to said brightness control signal and having a second operating mode responsive to the absence of said blanking signal for operating in a non-conductive state in which said feedback path is opened;

said circuit path includes a diode (22) having an anode coupled to said second plate (A) of said capacitor (18) and having a cathode coupled to said junction (B), said diode having a parasitic capacitance (CP) associated therewith;

said junction (B) of said first (37) and second (38) resistors is coupled via a third resistor to a source of bias potential (VB); and

said diode being rendered conductive during said blanking interval in response to closure of said feedback path for applying a DC restoration voltage to said capacitor proportional to said brightness control voltage provided by said amplifier, said diode being rendered non-conductive during said image interval in response to opening of said feedback path, said parasitic capacitance being effectively decoupled from said amplifier by said first and second resistors and being effectively decoupled from said source of bias potential by said



third resistor.

2. A video signal DC restoration circuit as recited in Claim 1 further characterized in that:

said amplifier comprises a two-stage amplifier including a common collector connected input stage (30) and a common emitter connected output stage (31), said input stage having a common input connected to said second resistor of said feedback path, connected to a source (34) providing said brightness control signal and connected to a source (35) providing said blanking signal.

3. A video signal DC restoration circuit as recited in Claims 1 or 2 further characterized in that:

said third resistor (24) in said bias network is of a value selected to be larger than the impedance exhibited by said parasitic capacitance (CP) of said diode (22) at the highest video frequency of said video input signal.

Revendications

1. Circuit de restitution en continu de signal vidéo comprenant :

un amplificateur d'attaque vidéo ayant une entrée pour recevoir un signal d'entrée vidéo ayant des intervalles d'image et de suppression et ayant une sortie reliée à une première plaque d'un condensateur ayant une seconde plaque reliée à un tube d'image ; un amplificateur de restitution en continu auquel des signaux de commande de suppression et de luminosité sont appliqués et ayant une voie de contre-réaction comportant des première et seconde résistances montées en série entre des bornes de sortie et d'entrée dudit amplificateur ; et une voie de circuit montée entre une jonction de ladite résistance et de ladite seconde plaque dudit condensateur, caractérisé en ce que :

ledit amplificateur de restitution en continu (30, 31) comprend un transistor de sortie (31) ayant un premier mode de Fonctionnement en réponse à la présence dudit signal de suppression, auquel ladite voie de contre-réaction est fermée pour fournir un signal de sortie proportionnel audit signal de commande de luminosité et ayant un deuxième mode de fonctionnement en réponse à l'absence dudit signal de suppression pour fonctionner à un état de non-conduction auquel ladite voie de contre-réaction est ouverte ;

ladite voie de circuit comprend une diode (22) ayant une anode reliée à ladite seconde plaque (A) dudit condensateur (18) et ayant

une cathode reliée à ladite jonction (B), ladite diode ayant une capacité parasite (CP) associée à celle-ci ;

ladite jonction (B) desdites première (37) et seconde (38) résistances est reliée par une troisième résistance à une source d'un potentiel de polarisation (VB) ; et

ladite diode étant rendue conductrice pendant ledit intervalle de suppression en réponse à la fermeture de ladite voie de contre-réaction pour appliquer une tension de restitution en continu audit condensateur proportionnelle à ladite tension de commande de luminosité produite par ledit amplificateur, ladite diode étant rendue non conductrice pendant ledit intervalle d'image en réponse à l'ouverture de ladite voie de contre-réaction, ladite capacité parasite étant effectivement découplée dudit amplificateur par lesdites première et seconde résistances et étant effectivement découplée de ladite source dudit potentiel par ladite troisième résistance.

2. Circuit de restitution en continu de signal vidéo selon la revendication 1, caractérisé en ce que :

l'amplificateur précité comprend un amplificateur à deux étages comportant un étage d'entrée (30) relié en collecteur commun et un étage de sortie (31) relié en émetteur commun, ledit étage d'entrée ayant une entrée commune reliée à la seconde résistance précitée de la voie de contre-réaction précitée, reliée à une source (34) produisant le signal de commande de luminosité précité et reliée à une source (35) produisant le signal de suppression précité.

3. Circuit de restitution en continu de signal vidéo selon la revendication 1 ou 2, caractérisé en outre en ce que :

la troisième résistance précitée (24) dans le réseau de polarisation précité présente une valeur sélectionnée de façon à être plus grande que l'impédance produite par la capacité parasite précitée (CP) de la diode précitée (22) à la fréquence vidéo la plus élevée du signal d'entrée vidéo précité.

Ansprüche

1. Videosignal-Schwarzwerthalteschaltung mit:
einem Videotreiberverstärker, der einen Eingang zum Empfang eines Bild- und Austastintervalle enthaltenden videoeingangssignales sowie einen Ausgang aufweist, der mit einem ersten Belag eines Kondensators gekoppelt ist,



dessen zweiter Belag mit einer Bildröhre gekoppelt ist;

einem Schwarzwerthalteverstärker, dem Austast- und Helligkeitssteuersignale zugeführt werden und der einen Rückführungsweg aufweist, welcher einen ersten und einen zweiten Widerstand enthält, die in Reihe zwischen einem Ausgangs- und einen Eingangsanschluß des Verstärkers geschaltet sind; und

einer Schaltungsstrecke, die zwischen eine Verbindung der genannten Widerstände und den zweiten Belag des Kondensators geschaltet ist, **dadurch gekennzeichnet**, daß

der Schwarzwerthalteverstärker (30, 31) einen Ausgangstransistor (31) enthält, der eine erste Betriebsart aufweist als Reaktion auf das Vorhandensein des Austastsignales, bei der der Rückführungsweg geschlossen ist, um ein dem Helligkeitssteuersignal proportionales Ausgangssignal zu liefern, und eine zweite Betriebsart als Reaktion auf das Fehlen des Austastsignales, bei der er im nichtleitenden Zustand arbeitet, in dem die Rückführungsstrecke geöffnet ist;

die Schaltungsstrecke eine Diode (22) enthält, deren Anode mit dem zweiten Belag (A) des Kondensators (18) gekoppelt ist, deren Kathode mit der genannten Verbindung (B) gekoppelt ist und die mit einer Streukapazität (CP) behaftet ist;

die Verbindung (B) zwischen dem ersten (37) und dem zweiten (38) Widerstand über einen dritten Widerstand mit einer Quelle für ein Vorspannungspotential (VB) gekoppelt ist; und

die Diode während des Austastintervalles als Reaktion auf das Schließen des Rückführungsweges leitend gemacht wird, um an den Kondensator eine Schwarzwerthaltespannung zu liefern, die der vom Verstärker gelieferten Helligkeitssteuerspannung proportional ist, und daß die Diode während des Bildintervalles als Reaktion auf das Öffnen der Rückkopplungsstrecke nichtleitend gemacht wird, wobei die Streukapazität durch den ersten und den zweiten Widerstand effektiv vom Verstärker abgekoppelt und durch den dritten Widerstand effektiv von der Vorspannungspotentialquelle abgekoppelt ist.

2. Videosignal-Schwarzwerthalteschaltung nach Anspruch 1, **dadurch gekennzeichnet**, daß der Verstärker einen zweistufigen Verstärker mit einer Eingangsstufe (30) in Kollektorschaltung und einer Ausgangsstufe (31) in Emitterschaltung enthält und daß die Eingangsstufe einen gemeinsamen Eingang hat, der mit dem zweiten Widerstand des Rückkopplungsweges,

einer Quelle (34), die das Helligkeitssteuersignal liefert, und einer Quelle (35), die das Austastsignal liefert, verbunden ist.

3. Videosignal-Schwarzwerthalteschaltung nach Anspruch 1 oder 2, **dadurch gekennzeichnet**, daß der dritte Widerstand (34) im Vorspannungsnetzwerk einen Wert hat, der größer gewählt ist, als die Impedanz der Streukapazität (CP) der Diode (22) bei der höchsten Videofrequenz des Videoeingangssignales.

