

Description

This invention concerns a circuit for coupling a video output signal to an image display device such as a kinescope in a television receiver. An embodiment of this invention concerns a video output signal coupling circuit having signal limiting and frequency compensation characteristics.

In a television receiver a video output display driver stage provides a high level video output signal to an image display device such as a kinescope, which is often driven with as large a video signal as practical so as to produce a bright display. Examples of a video output display driver stage are shown in US-A-4331981 and US-A-4727336. It is also desirable for the display driver stage to exhibit as wide a bandwidth as possible so as to produce an image display with good image resolution particularly in areas of fine detail associated with high frequency video signal information. To accomplish this objective the display device can be driven by means of a low output impedance amplifier such as an emitter follower transistor stage. An example of a low output impedance amplifier stage is disclosed in JP 63-015518. The use of such a stage isolates an input capacitance of the display device from other elements of the display driver stage to prevent unwanted interaction which could lead to high frequency degradation due to a lowpass filtering effect, for example. However, it has been noticed that many kinescopes exhibit a "blooming" effect, resulting in distortion of displayed image detail, when driven at high signal levels (e.g. peak white levels) from a low impedance source such as an emitter-follower transistor.

In accordance with the present invention there is provided a video signal processing system for driving an image display device having a signal input electrode with an associated parasitic capacitance and comprising: a display driver amplifier having a signal input for receiving a video signal containing information to be displayed, and having an output circuit, including an impedance, for developing a video output signal with a magnitude suitable for driving said image display device; and a signal coupling path for conveying said video output signal from said output circuit to said signal input electrode of said image display device, wherein said signal coupling path comprises: first and second series resistors coupled to said input electrode of said image display device; and a capacitor coupled across one of said first and second resistors; said system being characterized in that said signal coupling path further comprises: an amplifier device with an input for receiving said video output signal, and a low impedance output, said first and second series resistors being coupled in the order named from said low impedance out-

put of said amplifier device to said input electrode of said image display device; means, including said amplifier device, for isolating said capacitor and said parasitic capacitance from said impedance in said output circuit of said display driver amplifier for both positive and negative amplitude excursions of said video output signal; and means coupling the junction of said first and second resistors to a source of bias potential representative of an image blanking level for biasing a signal level at said signal input electrode of said image display device toward said image blanking level.

The sole figure of the drawing illustrates a portion of a television receiver including a video output signal coupling network in accordance with the principles of the present invention.

A low level video signal from a source 10 is applied to a kinescope driver stage 20 including an input low voltage common emitter amplifier transistor 22 arranged in a cascode video amplifier configuration with an output high voltage common base amplifier transistor 24. A high level amplified video signal with a magnitude suitable for driving a signal input cathode electrode 30 of a kinescope 35 is developed in a collector output circuit of transistor 24, including a load resistor 25 coupled to a high operating voltage B+ (e.g., +230 volts). An amplified video output signal developed across resistor 25 is coupled to cathode electrode 30 via a network 26, a frequency compensated drive level compensation network 27 in accordance with the principles of the present invention, and a kinescope arc current limiting resistor 28, commonly referred to as a "flashover" resistor, operatively associated with network 27. The signal gain and the DC bias of driver stage 20 are respectively adjusted by means of a variable resistor 38 and a potentiometer 39 in the emitter circuit of transistor 22. Operating voltages for kinescope 35 are provided by a source 36.

A capacitance C3 represents parasitic kinescope and wiring capacitance associated with kinescope cathode electrode 30. The value of this capacitance is approximately 9 picofarads and can result in significant high frequency degradation if it is permitted to influence the video signal developed across resistor 25 in the output circuit of transistor 24. Network 26 is arranged to reduce or eliminate such high frequency degradation by decoupling such capacitance from the collector output circuit of transistor 24.

Coupling network 26 includes an NPN emitter follower transistor 41 with a low impedance emitter output electrode and PNP emitter follower transistor 42 with a low impedance emitter output electrode arranged in cascade in the output signal path from the collector output circuit of transistor 24 to kinescope 30. Parasitic collector-base capacitances

C1 and C2, e.g., 2 picofarads, are respectively associated with transistors 41 and 42 and include stray wiring and layout capacitances. Diodes 43 and 44 are coupled across the base-emitter junctions of transistors 41 and 42, respectively, and are poled for forward current conduction in a direction opposite to the forward current conduction direction of the associated base-emitter junction.

A rapid positive amplitude transition, which contains significant high frequency image detail information, is conveyed to kinescope 35 via conductive transistor 41 and conductive diode 44. Diode 43 and transistor 42 and reverse biased (non-conductive) at this time.

In the case of a rapid positive-going video signal amplitude transition at the collector output of transistor 24, the capacitance presented to the collector output of transistor 24 is substantially equal to

$$C1 + C2/\beta_{41} + C3/\beta_{41} \quad (1)$$

where capacitances C1, C2 and C3 are as discussed above and β_{41} is the forward current gain (Beta) of transistor 41, typically 100 minimum. Thus at the collector of driver transistor 24 the value of kinescope capacitance C3 is greatly reduced by the Beta (β) of transistor 41, and the value of relatively small capacitance C2 is reduced further by the Beta of transistor 41. Resistor 28 assists to isolate the kinescope capacitance from the output circuit of driver transistor 24, but the effect of such action is much less than that produced by network 26.

Rapid negative amplitude transitions, which also contain significant high frequency image detail information, are conveyed to kinescope 35 via conductive diode 43 and transistor 42. Transistor 41 and diode 44 are reverse biased at this time.

For rapid negative-going video signal amplitude transitions at the collector output of transistor 24, the capacitance presented to the collector output of transistor 24 is substantially equal to

$$C1 + C2 + C3/\beta_{42} \quad (2)$$

where β_{42} is the forward current gain of transistor 42, typically 100 minimum. Thus the relatively large value of kinescope capacitance C3 is greatly reduced by the Beta of transistor 42 at the collector of driver transistor 24.

A relatively large bypass capacitor 54 shunting a resistor 52 in network 27, as will be discussed subsequently, has a negligible effect upon the value of capacitance given by expressions (1) and (2) above since the value of capacitance presented to the emitter or transistor 42 is dominated by capacitance C3.

Note that the base-emitter junctions of transistors 41 and 42 are not bypassed by capacitors. Such bypassing of one or both of these transistors would defeat the purpose of isolating the output circuit of transistor 24 from capacitances such as kinescope capacitance C3 and capacitor 54 in this example, in the presence of positive or negative signal amplitude transients or both.

A display driver stage including coupling network 26 has been found to exhibit a significant improvement in high frequency response due to decoupling kinescope capacitance C3 from the output circuit of transistor 24, as well as a substantially symmetrical positive and negative transient response. In the latter regard it is noted that expressions (1) and (2) above contain different values of capacitance for positive and negative amplitude transients. The difference is small, however, and transistor 24 can more easily drive a capacitive load when exhibiting increasing conduction and an associated decreasing collector impedance in response to negative signal amplitude excursions, compared to driving a capacitance when exhibiting decreasing conduction and increasing collector impedance in response to positive amplitude excursions.

Network 26 can assume configurations other than that shown. For example, when a PNP transistor is employed for driver 24 the positions of transistors 41 and 42 with associated diodes 43 and 44 should be interchanged.

With the disclosed arrangement the value of collector load resistor 25 can be lowered in value because the kinescope does not directly load the collector circuit of transistor 24, i.e., the collector circuit is buffered via follower transistors 41 and 42. A lower value of collector load resistance advantageously enhances high frequency response since a smaller resistance value produces less of a lowpass filtering effect together with parasitic collector circuit capacitances.

Network 27 includes a series coupling resistor 52 and a frequency compensation capacitor 54 arranged in parallel as shown, together with flashover resistor 28. A resistor 56 is coupled between an operating voltage (B+) and a point in the signal path to which capacitor 54 is coupled.

Network 27 compensates for the tendency of an image display device such as kinescope 35 to "bloom", or conduct excessive current, when driven by a large magnitude video signal from a low impedance source such as the emitter output of PNP follower transistor 42. To this end resistor 28 and resistor 52 do not develop a significant voltage drop for kinescope current conduction in response to a video signal of low to moderate magnitude. However, resistors 52 and 28 develop a significant voltage drop for kinescope current con-

duction in response to a large magnitude video signal, e.g., representative of a bright image. This voltage drop reduces the signal drive to kinescope cathode electrode 30, thereby reducing or eliminating the likelihood that the kinescope will "bloom" under large signal conditions. The values of resistors 52 and 28 and capacitor 54 are chosen to yield a desired display drive impedance, particularly at low through middle video signal drive levels which determine image brightness and intensity, so as to maintain kinescope current conduction in accordance with a gamma correction function as is known. The values of resistors 52 and 28 can be tailored to provide a desired amount of gamma correction depending on the type of kinescope and its current conduction characteristics.

Capacitor 54 is a high frequency bypass element to compensate for a high frequency loss associated with a lowpass filtering effect produced by the coaction of kinescope capacitance C3 with resistors 28 and 52. The high frequency compensation provided by network 27 begins at approximately 500 KHz, which is well within the DC to 4.2 MHz video signal band according to NTSC standards. The amount of high frequency compensation, including high frequency boost, is a function of the values of capacitor 54, resistors 52 and 28, capacitance C3 and the impedance of kinescope cathode 30. The impedance of cathode 30 is a function of the current conduction level of cathode 30. In this example, more high frequency compensation is provided at higher cathode current levels.

Capacitor 54 could be coupled across resistor 28 instead of across resistor 28 as illustrated. However, it is preferred that the non-bypassed resistor be located as close to the kinescope as possible to minimize the damage to circuit boards and associated circuit elements due to kinescope arcing. Placing bypass capacitor 54 across both resistors 52 and 28 would defeat the intended arc current protection since such a capacitor coupling would provide an arc current path circumventing the current limiting effect of resistor 28 in this case.

Resistor 56 provides a bias for kinescope cathode 30 to assure that the kinescope is blanked during retrace intervals. Resistor 56 also assists capacitor 54 in providing the desired high frequency compensation at various signal drive levels. Specifically, resistor 56 helps to stabilize the effective impedance presented to the network including resistor 52 and capacitor 54, in the presence of kinescope impedance variations associated with changes in the level of kinescope current conduction due to changes in the drive signal level.

Claims

1. A video signal processing system for driving an image display device (35) having a signal input electrode with an associated parasitic capacitance and comprising:
 - a display driver amplifier (20) having a signal input (base 22) for receiving a video signal containing information to be displayed, and having an output circuit (collector 24), including an impedance (25), for developing a video output signal with a magnitude suitable for driving said image display device; and
 - a signal coupling path for conveying said video output signal from said output circuit to said signal input electrode of said image display device, wherein said signal coupling path comprises:
 - first (52) and second (28) series resistors coupled to said input electrode of said image display device; and
 - a capacitor (54) coupled across one of said first and second resistors; said system being characterized in that
 - said signal coupling path further comprises:
 - an amplifier device (41 or 42) with an input for receiving said video output signal, and a low impedance output, said first and second series resistors being coupled in the order named from said low impedance output of said amplifier device to said input electrode of said image display device;
 - means (26), including said amplifier device (41 or 42), for isolating said capacitor (54) and said parasitic capacitance from said impedance in said output circuit of said display driver amplifier for both positive and negative amplitude excursions of said video output signal; and
 - means coupling the junction of said first and second resistors to a source of bias potential representative of an image blanking level for biasing a signal level at said signal input electrode of said image display device toward said image blanking level.
2. A system according to Claim 1, characterized in that
 - said signal coupling path is DC coupled; and
 - said amplifier device (41 or 42) is an emitter-follower transistor with a base input electrode and a low impedance emitter output electrode.
3. A system according to Claim 1 or 2, characterized in that



duction in response to a large magnitude video signal, e.g., representative of a bright image. This voltage drop reduces the signal drive to kinescope cathode electrode 30, thereby reducing or eliminating the likelihood that the kinescope will "bloom" under large signal conditions. The values of resistors 52 and 28 and capacitor 54 are chosen to yield a desired display drive impedance, particularly at low through middle video signal drive levels which determine image brightness and intensity, so as to maintain kinescope current conduction in accordance with a gamma correction function as is known. The values of resistors 52 and 28 can be tailored to provide a desired amount of gamma correction depending on the type of kinescope and its current conduction characteristics.

Capacitor 54 is a high frequency bypass element to compensate for a high frequency loss associated with a lowpass filtering effect produced by the coaction of kinescope capacitance C3 with resistors 28 and 52. The high frequency compensation provided by network 27 begins at approximately 500 KHz, which is well within the DC to 4.2 MHz video signal band according to NTSC standards. The amount of high frequency compensation, including high frequency boost, is a function of the values of capacitor 54, resistors 52 and 28, capacitance C3 and the impedance of kinescope cathode 30. The impedance of cathode 30 is a function of the current conduction level of cathode 30. In this example, more high frequency compensation is provided at higher cathode current levels.

Capacitor 54 could be coupled across resistor 28 instead of across resistor 28 as illustrated. However, it is preferred that the non-bypassed resistor be located as close to the kinescope as possible to minimize the damage to circuit boards and associated circuit elements due to kinescope arcing. Placing bypass capacitor 54 across both resistors 52 and 28 would defeat the intended arc current protection since such a capacitor coupling would provide an arc current path circumventing the current limiting effect of resistor 28 in this case.

Resistor 56 provides a bias for kinescope cathode 30 to assure that the kinescope is blanked during retrace intervals. Resistor 56 also assists capacitor 54 in providing the desired high frequency compensation at various signal drive levels. Specifically, resistor 56 helps to stabilize the effective impedance presented to the network including resistor 52 and capacitor 54, in the presence of kinescope impedance variations associated with changes in the level of kinescope current conduction due to changes in the drive signal level.

Claims

1. A video signal processing system for driving an image display device (35) having a signal input electrode with an associated parasitic capacitance and comprising:
 - a display driver amplifier (20) having a signal input (base 22) for receiving a video signal containing information to be displayed, and having an output circuit (collector 24), including an impedance (25), for developing a video output signal with a magnitude suitable for driving said image display device; and
 - a signal coupling path for conveying said video output signal from said output circuit to said signal input electrode of said image display device, wherein said signal coupling path comprises:
 - first (52) and second (28) series resistors coupled to said input electrode of said image display device; and
 - a capacitor (54) coupled across one of said first and second resistors; said system being characterized in that
 - said signal coupling path further comprises:
 - an amplifier device (41 or 42) with an input for receiving said video output signal, and a low impedance output, said first and second series resistors being coupled in the order named from said low impedance output of said amplifier device to said input electrode of said image display device;
 - means (26), including said amplifier device (41 or 42), for isolating said capacitor (54) and said parasitic capacitance from said impedance in said output circuit of said display driver amplifier for both positive and negative amplitude excursions of said video output signal; and
 - means coupling the junction of said first and second resistors to a source of bias potential representative of an image blanking level for biasing a signal level at said signal input electrode of said image display device toward said image blanking level.
2. A system according to Claim 1, characterized in that
 - said signal coupling path is DC coupled; and
 - said amplifier device (41 or 42) is an emitter-follower transistor with a base input electrode and a low impedance emitter output electrode.
3. A system according to Claim 1 or 2, characterized in that



said capacitor (54) is coupled across said first resistor (52).

4. A system according to any one of the preceding claims, characterized in that said isolating means (26) includes:
 - an emitter follower transistor (41) comprising said amplifier device; and
 - an additional opposite conductivity type emitter-follower transistor (42) coupled in cascade with said first named emitter-follower transistor.
5. A system according to any one of the preceding claims characterized in that
 - said capacitor (54) with said one of said first (52) and second (28) resistors comprises a high frequency compensation circuit with respect to a range of high frequencies of said video output signal, to improve the high frequency information content of a displayed image.
6. A system according to any one of the preceding claims, further comprising an image display device (35) having an input, with an associated parasitic capacitance, connected to said signal coupling path.

Patentansprüche

1. Videosignal-Verarbeitungssystem zum Ansteuern einer Bild-Darstellungseinrichtung (35) mit einer zugehörigen parasitären Kapazität aufweisenden Signal-Eingangselektrode, enthaltend:
 - einen Anzeige-Treiberverstärker (20) mit einem Signal-Eingang (Basis 22) zum Erhalt eines Videosignals, das darzustellende Information beinhaltet, und mit einem Ausgangskreis (Kollektor 24), der eine Impedanz (25) zum Bilden eines Video-Ausgangssignals mit einer zur Ansteuerung der Bild-Anzeigeeinrichtung geeigneten Amplitude beinhaltet; und
 - einen Signal-Kopplungspfad zum Weitergeben des Video-Ausgangssignals von der Ausgangsschaltung an die Signal-Eingangselektrode der Bild-Darstellungseinrichtung, wobei der Signal-Kopplungspfad beinhaltet:
 - ersten (52) und zweiten (28) in Reihe geschalteten Widerstand, der an die Eingangselektrode der Bild-Darstellungseinrichtung gekoppelt ist; und
 - einen Kondensator (54), der parallel zu dem ersten oder dem zweiten Widerstand gekoppelt ist; wobei das System

dadurch gekennzeichnet ist, daß der Signal-Kopplungspfad beinhaltet:

- eine Verstärker-Einrichtung (41 oder 42) mit einem Eingang zum Erhalt des Video-Ausgangssignals und einem Ausgang mit niedriger Impedanz, wobei der erste und zweite Serien-Widerstand in der genannten Reihenfolge von dem Ausgang mit niedriger Impedanz der Verstärker-Einrichtung zu der Eingangselektrode der Bild-Darstellungseinrichtung gekoppelt ist;
- ein die Verstärker-Einrichtung (41 oder 42) beinhaltendes Mittel (26) zum Entkoppeln des Kondensators (54) und der parasitären Kapazität von der Impedanz in dem Ausgangskreis des Anzeige-Treiberverstärkers für positive und negative Amplitudenausschläge des Video-Ausgangssignals; und
- ein die Verbindung des ersten und zweiten Widerstands mit einer Quelle eines Vorspannungs-Potentials koppelndes Mittel, wobei das Potential für einen Bild-Austastpegel zum Vorspannen eines Signalpegels an der Signal-Eingangselektrode der Bild-Darstellungseinrichtung in Richtung auf den Bild-Austastpegel repräsentativ ist.

2. System nach Anspruch 1, dadurch gekennzeichnet,

- daß der Signal-Kopplungspfad gleichstrom-gekoppelt ist (DC); und
- daß die Verstärker-Einrichtung (41 oder 42) ein Emitterfolger-Transistor mit einer Basis-Eingangselektrode und einer Emitter-Ausgangselektrode mit geringer Impedanz ist.

3. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß der Kondensator (54) dem ersten Widerstand (52) parallelgeschaltet ist.

4. System nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß das Entkopplungsmittel (26) beinhaltet:

- einen Emitterfolger-Transistor (41) als Verstärker-Einrichtung; und
- einen zusätzlichen Emitterfolger-Transistor (42) mit umgekehrter Leitfähigkeit, der mit dem zuerst genannten Emitterfolger-Transistor in Kaskade geschaltet ist.

5. System nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß der Kondensator



sator (54) mit einem der ersten (52) und zweiten (28) Widerstände eine Hochfrequenz-Kompensationsschaltung bezüglich eines Bereichs von Hochfrequenzen des Video-Ausgangssignals bildet, um den Hochfrequenz-Informationsgehalt eines dargestellten Bildes zu verbessern.

6. System nach einem der vorhergehenden Ansprüche, weiter enthaltend eine Bild-Darstellungseinrichtung (35) mit einem eine zugehörige parasitäre Kapazität aufweisenden Eingang, der mit dem Signal-Kopplungspfad verbunden ist.

Revendications

1. Système de traitement de signal vidéo pour commander un dispositif d'affichage d'images (35) ayant une électrode d'entrée de signal avec une capacité parasite associée et comprenant :

un amplificateur de commande d'affichage (20) ayant une entrée de signal (base 22) pour recevoir un signal vidéo contenant de l'information à afficher et ayant un circuit de sortie (collecteur 24), comportant une impédance (25) pour développer un signal de sortie vidéo avec une amplitude appropriée à la commande dudit dispositif d'affichage d'images et,

une trajectoire de couplage de signaux pour convoyer ledit signal de sortie vidéo, provenant dudit circuit de sortie, à ladite électrode d'entrée de signal du dispositif d'affichage d'images, dans lequel ladite trajectoire de couplage de signaux comprend :

des première (52) et seconde (28) résistances couplées en série sur ladite électrode d'entrée dudit dispositif d'affichage d'images et,

un condensateur (54) couplé sur l'une desdites première et seconde résistances, ledit système étant caractérisé en ce que ladite trajectoire de couplage de signaux comprend en outre :

un dispositif amplificateur (41 ou 42) avec une entrée pour recevoir ledit signal de sortie vidéo et une sortie de faible impédance, lesdites première et seconde résistances en série étant couplées dans l'ordre indiqué, de ladite sortie à faible impédance du dispositif amplificateur à ladite électrode d'entrée du dispositif d'affichage d'images ;

des moyens (26), incluant ledit dispositif amplificateur (41 ou 42), pour isoler ledit condensateur (54) et ladite capacité parasite de ladite impédance dans le circuit de sortie de l'amplificateur de commande d'affichage

pour des excursions d'amplitude, à la fois positives et négatives, dudit signal de sortie vidéo ; et

des moyens couplant la jonction desdites première et seconde résistances à une source de potentiel de polarisation représentatif d'un niveau de suppression d'images pour polariser un niveau de signal à l'électrode d'entrée de signal du dispositif d'affichage d'images vers ledit niveau de suppression d'images.

2. Système selon la revendication 1, caractérisé en ce que ladite trajectoire de couplage de signaux est couplée en courant continu et

ledit dispositif amplificateur (41 ou 42) est un transistor à émetteur suiveur avec une électrode d'entrée de base et une électrode de sortie d'émetteur à faible impédance.

3. Système selon la revendication 1 ou 2, caractérisé en ce que ledit condensateur (54) est couplé sur ladite première résistance (52).

4. Système selon l'une quelconque des revendications précédentes, caractérisé en ce que lesdits moyens isolants (26) comprennent :

un transistor à émetteur suiveur (41) comprenant ledit dispositif amplificateur et,

un transistor à émetteur suiveur additionnel (42), d'un type de conductivité opposé, couplé en cascade avec ledit premier transistor à émetteur suiveur.

5. Système selon l'une quelconque des revendications précédentes, caractérisé en ce que

ledit condensateur (54) avec l'une desdites première (52) et seconde (28) résistances, comprend un circuit de compensation à haute fréquence, par rapport à un domaine de fréquences élevées dudit signal de sortie vidéo, pour améliorer le contenu de l'information à haute fréquence de l'image affichée.

6. Système selon l'une quelconque des revendications précédentes, comprenant en outre un dispositif d'affichage d'images (35), ayant une entrée, avec une capacité parasite associée, connectée à ladite trajectoire de couplage de signaux.