Three Dimensional Device Integration Method and Integrated Device

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to three-dimensionally integrated semiconductor devices and, in particular, to semiconductor devices vertically bonded together to form three-dimensional structures.

Discussion of the Background:

The ability to integrate determines the success of the semiconductor industry. This was first demonstrated with the invention of the integrated circuit (IC). The IC essentially consists of fabrication of electronic components at the surface of the semiconductor wafer followed by interconnection of these components with metalization on top of the components. The dramatic reduction in cost and increase in performance that has resulted from this integration has had a profound economic impact.

Since the invention of the IC, the semiconductor industry has experienced continued rapid growth due to continuous improvements in the integration density of various electronic components (i.e., transistors, diodes, resistors, capacitors, etc.) achieved. For the most part, this improvement in integration density has come from repeated reduction in minimum feature size which allow more components to be integrated in a given area. Additional improvement has come from increases in wafer size.

These integration improvements are essentially two-dimensional (2-D) in nature, in that the volume occupied by the integrated components is essentially at the surface of semiconductor wafer. Although dramatic improvements in lithography have resulted in considerable improvement in this 2-D integration, there are physical limits to the density which can be achieved in 2-D. One of these limits is simply the minimum size needed to make these components. Another limit is the significant increase in interconnect requirements between components as the component size is reduced.

Efforts to achieve integration beyond that available with 2-D has been explored and resulted in improvement in chip memory and further semiconductor industry growth. For instance, the trench capacitor uses significant semiconductor volume below the wafer surface

and allows more functionality to be achieve in a given chip area. Other efforts, directed at achieving higher levels of integration by increased use of the volume in a given chip area, have recently increased. One approach has been to iterate the integration process by adding semiconductor material on top of the interconnect metalization followed by additional interconnect metalization. Although this potentially results in more components per chip area, it suffers from other problems including significantly increased thermal budgets. In addition, this and other efforts are distinct in that they only use one substrate and then work on one surface of that substrate. Not subjecting the devices to the thermal processes involved in fabricating the interconnect would simplify and enhance the fabrication of the devices.

Another problem results from the lagging of the ability to scale interconnect dimensions compared to scaling device dimensions. Ideally, one wants the critical dimension of a via to be the same as a gate dimension. However, since the scaling of vias lags the scaling of devices, integration density is limited.

Further problems arise when trying to integrate different types of technologies into a single circuit or wafer. BiCMOS is one example. Typically, special processing techniques must be devised to be able to combine the technologies. Processes required for one technology often interfere with processes required for another. As a result, compromises are made. The overall development of the combined technology becomes frozen in time, making flexible integration of the technologies that are being combined very difficult if not impossible. In other words, the most advanced "best of breed" technologies are not combined and evolutions in the technologies cannot be exploited.

Another problem of combining technologies is that customization must occur up front. One must first design the processing to combine the technologies and thus the limitations are built into the device. Again, one cannot easily take advantage of evolutions and improvements in technology since that requires redesigning the processing.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method and device having high integration density.

It is another object of the invention to provide a method and device where different types of materials may be integrated.

It is a further object of the present invention to provide a method of integrating different types of devices, and a structure comprising the integrated devices.

It is yet another object of the invention to provide a method and device where different types of technologies are integrated.

It is a still further object of the invention to avoid or minimize the thermal budgets in interconnecting devices.

It is yet another object of the invention to allow the integration of the best available technologies without making significant processing compromises.

These and other objects of the invention may be achieved by a method of bonding including polishing respective first surfaces of first, second and third workpieces each to a desired surface roughness, bonding together said first surfaces of said first and second workpieces, polishing a second surface of one of said first and second workpieces after bonding to said surface roughness, and bonding said first surface of said third workpiece to said polished second surface.

The surfaces may be polished to a roughness of no more than about 5-10Å. The first workpiece may be obtained by forming a thin first material on a second material, the second workpiece may be obtained by forming a thin third material on a fourth material, and the third workpiece may be obtained by forming a fifth material on a sixth material. The method may include the steps of polishing the first, third and fifth materials to obtain the first surfaces.

The first and third materials may each be formed of a material having a high thermal conductivity and a high dielectric constant. The first, third and fifth materials may be selected from the group consisting of silicon dioxide, silicon and diamond-like carbon. The first, third and fifth materials may be formed to a thickness of about 1-10 times a surface non-planarity of the second, fourth and sixth materials, respectively.

The method may also include the steps of forming first through third semiconductor devices on respective first through third substrates as the first-third workpieces. Surfaces of the first and second semiconductor devices may be polished to obtain the respective first and second surfaces. In this example, a first material may be formed on the surface of the first semiconductor device and a second material may be formed on the surface of the second semiconductor device. The first and second materials may be polished to obtain the respective first and second surfaces.

An exposed surface of one of the first and second semiconductor devices may be polished to a desired surface roughness after bonding the first and second surfaces, and the first surface of the third semiconductor device may be bonded with the exposed surface.

In another example, an exposed surface of one of the first and second semiconductor devices may be polished to a surface roughness of no more than about 5-10Å after bonding the first and second surfaces. Surfaces of N-2 semiconductor devices may be polished each having a surface roughness of about no more than 5-10Å. The N-2 semiconductor devices may be bonded to the bonded first and second semiconductor devices to obtain an N-integrated bonded device. Substrates of each of the N-2 semiconductor devices may be removed in the integration process.

The first-third semiconductor devices may each comprise integrated circuits formed on substrates. One of the substrates of the first and second semiconductor devices may be removed after the bonding step. A surface exposed by removing the substrate may be polished to a surface roughness of about no more than 5-10Å, a surface of a third semiconductor device may be polished to a surface roughness of about no more than 5-10Å, and the surface of the third semiconductor device and the polished exposed surface may be bonded.

The method may also include the steps of using a surrogate substrate as the first workpiece, forming an integrated circuit on a second substrate as the second workpiece, polishing a surface of the first substrate, polishing a surface of the integrated circuit, and bonding the first substrate and the integrated circuit. A second surface of the integrated circuit may be polished, a second integrated circuit may be formed on a third substrate as the third workpiece, a surface of the second integrated circuit may be polished, and the polished surface of the second integrated circuit may be bonded to the first integrated circuit.

A first material may be formed on the surface of the substrate and polished. A second material may be formed on the surface of the integrated circuits and polished. The first and second materials may be formed to a thickness of about 1-10 times a surface non-planarity of the surfaces of the substrate and integrated circuits, respectively.

The method may also include steps of forming N thin films on a first material to obtain the first workpiece and polishing an uppermost one of the N films to obtain the desired surface roughness, and forming M thin films on a second material to obtain the second

workpiece and polishing an uppermost one of the M thin films to obtain the desired surface roughness. The method may also include at least one of the steps of polishing at least plural of the N thin films and polishing at least plural of the M thin films.

A surrogate substrate may be used as the first workpiece. A stress relieving layer may be formed on the surrogate substrate. A thin film may be formed on the stress relieving layer and the thin film may be polished to obtain the desired surface roughness.

The method may also include interconnecting the semiconductor devices. The connections may be between circuits or between individual devices. Interconnecting the two devices may include bonding a multi-layer interconnection to one of the devices after bonding the two devices.

After bonding the first and second semiconductor devices, one of the substrates may be removed to expose a surface. This surface may be polished and a third semiconductor device may be bonded to the polished exposed surface.

Semiconductor devices and integrated circuits of different technologies may be integrated.

The method according to the invention may also comprise bonding a first semiconductor device having a first substrate to a second semiconductor device having a second substrate, removing a portion of said first substrate to expose a remaining portion of said first semiconductor device, and interconnecting said first and second semiconductor devices.

Substantially all of the substrate may be removed. Surfaces of the first and second devices may be planarized and bonded. Interconnecting the devices may comprises bonding a multi-layer interconnection to one of the devices. A surrogate substrate may be bonded to one the devices, and the corresponding substrate removed. The other of the devices may be bonded to the portion exposed by removing the substrate.

A third device may be bonded to the first and second devices, and the three devices may be interconnected. A substrate of the third device may be removed before interconnection.

The objects of the invention may also be achieved by a bonded device having a first workpiece having a first surface with a surface roughness and a second workpiece having respective second and third surfaces each having the surface roughness, the first and second

surfaces being bonded together. A third substrate has a fourth surface with the surface roughness. The third and fourth surfaces are bonded together. The first workpiece may include a thin first material disposed upon second material, the second workpiece may include a thin third material disposed on a fourth material and the third workpiece may include a thin fifth material disposed on a sixth material. Surfaces of the thin first, third and fifth materials may comprise the first, second and fourth surfaces, respectively.

Each of the thin first, third and fifth materials may comprise a material having a high thermal conductivity and a high dielectric constant and may be selected from the group consisting of silicon, silicon dioxide and diamond-like silicon carbide. The thin first, third and fifth materials may have a thickness of about 1-10 times a surface non-planarity of the second, fourth and sixth materials, respectively. The thin first, third and fifth materials may each include a plurality of thin layers, an uppermost one of each of the plurality of layers comprising the first, second and fourth surfaces, respectively.

The first, second and third workpieces may comprise first, second and third semiconductor devices, respectively. The first, second and third semiconductor devices may comprise first, second and third integrated circuits, respectively. The first, second and third semiconductor devices may comprise first through third 2-D arrays of unconnected devices. The second and third devices may have substantially all of their respective substrates removed.

The first workpiece may comprise a surrogate substrate, and the second and third workpieces may each comprise a semiconductor device. The surrogate substrate may comprise a thin first material disposed upon a second material, where the first material comprises the first surface. The semiconductor devices may each include a thin material disposed on an integrated circuit and the thin materials comprises the second and third surfaces, respectively. The thin first, second and third materials may have a thickness of about 1-10 times a surface non-planarity of the second material and the two integrated circuits, respectively.

The first workpiece may include a thin first material, a second material and a stress relieving material formed between the thin first material and the second material, or the second workpiece may include a thin third material, a fourth material and a stress relieving material formed between the thin third material and the fourth material. Surfaces of the thin

first and third materials may include the first and second surfaces, respectively.

The device according to the invention may also comprise an integrated device having a first semiconductor device, a second semiconductor device, comprised of a layer of devices formed on a substrate which has been at least partially removed, bonded to said first semiconductor device, and interconnections connecting said first and second semiconductor devices.

The second device may comprises said layer of devices formed on a substrate which has been substantially removed, and a third semiconductor device, comprised of a layer of devices formed on a substrate which has been at least partially removed, may be bonded to the second device. The interconnections may comprise a multi-layer interconnection bonded to the second device. The first device may comprise a layer of devices formed on a substrate which has been substantially removed bonded to a surrogate substrate, and the second device may comprise the layer of devices formed on a substrate which has been substantially removed. The second and third workpieces may be of different technologies.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

FIG. 1 is a sectional diagram illustrating a step in the method according to the invention;

FIG. 2 is a sectional diagram illustrating a step in the method according to the invention;

FIG. 3 is a sectional diagram illustrating bonding two substrates according to the invention;

FIG. 4 is a sectional diagram a bonded device according to the invention;

FIG. 5 is a sectional diagram of a heterojunction bipolar transistor;

FIG. 6 is a sectional diagram illustrating bonding the transistor of FIG. 4 according to the invention;

FIG. 7 is a sectional diagram of a bonded device according to the invention;

FIG. 8 is a sectional diagram illustrating a step in bonding together two devices according to the invention;

FIG. 9 is a sectional diagram illustrating a step in bonding together two devices according to the invention;

FIG. 10 is a sectional diagram illustrating two devices bonded according to the invention;

FIGS. 11A and 11B are sectional diagrams of two devices to be bonded according to the invention;

FIG. 12 is a sectional diagram illustrating bonding of the devices of FIGS. 11A and 11B;

FIG. 13 is a sectional diagram illustrating a step of interconnecting the devices of FIGS. 11A and 11B;

FIG. 14 is a sectional diagram illustrating a step of bonding the bonded devices of FIGS. 11A and 11B to another device;

FIG. 15 is a sectional diagram illustrating bonding and interconnecting three devices;

FIGS. 16A-16D are diagrams illustrating bonding three integrated circuits;

FIG. 17A is a diagram of a layered interconnect structure;

FIG. 17B is a diagram of bonding the layered interconnect structure of FIG. 17A to an substrate having integrated circuits;

FIG. 18 is a diagram of a 2-D array of circuit elements; and

FIG. 19 is a diagram of bonded and interconnected 2-D arrays of circuit elements.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, and more particularly to FIG. 1 which illustrates a first embodiment of the method and device according to the invention. A substrate 10 has a upper surface 11 having a surface planarity. Substrate 10 preferably is a surrogate substrate or an integrated circuit wafer. The non-planarity of surface 11 shown in FIG. 1 is for illustrative purposes and is not meant to depict exact surface planarity conditions. Substrate 10 preferably has a relatively smooth and planar surface 11. The desired smoothness and planarity of the upper surface may be achieved through polishing. Chemical-mechanical polishing or CMP is one manner of achieving the desired smoothness and planarity. The

CMP process is optimized with appropriate selection of polishing pads, polishing slurries and polishing conditions to obtain the desired surface roughness and planarity.

On surface 11 is deposited a film 12 having a thickness greater than the surface non-planarity of surface 11. Film 12 should have good thermal conductivity and a high dielectric constant, such as SiO_2, diamond or diamond-like carbon (DLC). Thermal conductivities in the range of 1-10 W/cmK and relative dielectric constants in the range of 1-3 are preferable. A preferable range of thickness for film 11 is from 1-10 times the surface non-planarity of film 11. The upper surface 13 of film 13 is then polished to a planar surface with a roughness of 5-15 Å and preferably between 5-10 Å. A planar surface with a roughness of ≤5 Å is most preferred as a smoother planar surface will enhance the bonding properties of the film.

It is also possible to deposit film 12, polish upper surface 13, and then deposit another film (14 in FIG. 2), and polish the second film, to achieve the desired smoothness of the upper surface (15 in FIG. 2). Three or more films, repeating the depositing and polishing operations for each or for at least the upper film, may be used to achieve the desired surface roughness and planarity.

The substrate 10 is now ready for wafer bonding. Any type of substrate may be bonded to substrate 10. Referring to FIG. 3, a substrate 16, preferably an integrated circuit wafer containing active devices, is prepared in the same manner as substrate 10 by forming a film 17 having an exposed surface 18 with a surface roughness in the same range as surface 13 of film 12 (or surface 15 of film 14). A higher degree of planarity will further facilitate the bonding process. Film 17 may be formed of one or more layers with one or more polishing operations, as described above. Surfaces 18 and 12 are brought into contact with each other (shown by the arrows in FIG. 3). A bond, such as a Van der Waals bond, between surfaces 18 and 13 is formed (FIG. 4). A stronger bond can be achieved by subsequently heating the joined substrates and films.

The preferred manner of bonding is direct bonding without the use of applied pressure, voltage or temperature. It the substrate has an upper surface of SiO_2 (or other bonding material), one can polish that surface without depositing another SiO_2 layer, assuming that the upper surface of SiO_2 has sufficient thickness to obtain a sufficient surface roughness and planarity with, e.g., CMP.

Example

This example uses the case of attachment of a diamond substrate to a material such as GaAs, InP, or GaN when optimal thermal packaging and dielectric performance are desired. Bonding to a substrate of a material having a high thermal conductivity allows one to better manage thermal transfer. The diamond substrate, after preparing it for bonding, has a relatively smooth upper surface. As diamond substrates typically have a relatively rough surface, a relatively smooth and planar upper surface may be obtained by polishing. Polishing may be expensive and difficult to consistently obtain very smooth surfaces. It is also possible to form the diamond substrate on a copper susceptor. Diamond films typically "pop-off" the copper susceptor after deposition as the temperature is lowered, leaving a relatively smooth and planar surface where growth initiated and a rougher surface where growth terminated.

On top of the upper surface is deposited a thin layer of silicon dioxide. The silicon dioxide layer should be thicker than the non-planarity of the diamond surface, e.g., 1-10 times, but as thin as possible to optimize performance. The silicon dioxide layer is then polished to a smooth surface suitable for wafer bonding, for example, ≤5 Å. The diamond substrate having the thin silicon layer is now ready for wafer bonding.

At this point any type of device formed on any type of substrate may be bonded to the surface of silicon dioxide layer. For this example, a heterojunction bipolar transistor (HBT), as described in application Serial No. 09/165,203, the disclosure of which is incorporated herein by reference, may be used. The HBT is processed to the point where it is ready for attachment of a surrogate substrate, as shown in FIG. 5. Typically, this would include the steps of forming the emitter metalization, performing base etching, applying base metalization, applying a passivation/planarization level and applying a thermal shunt. In FIG. 5 there is collector layer 22 formed on a GaAs substrate 20, planarizing material 21, base region 23, base contacts 24, emitter 25 and emitter contact 26. It should be noted that FIG. 5, while illustrating a single device, is not so limited. A wafer containing a number of devices or an integrated circuit may also be bonded in the same manner.

On top of the planarized surface of the HBT is deposited another very thin layer of silicon dioxide 27. The thickness of silicon dioxide layer 27 is thicker than the non-planarity of the planarized surface of the HBT (e.g., 1-10 times) but as thin as possible to optimize

performance. The surface of the silicon dioxide layer 27 is polished to a smoothness sufficient for wafer bonding, for example ≤ 5 Å. Layers 27 and 12 are then bonded by placing them in close proximity. The surfaces are preferably placed in close proximity after a wet cleaning process, followed by a drying operation to force the liquid from between the layers 27 and 12. A Van der Waals bond is formed. A stronger bond can be achieved by subsequently heating joined layers 27 and 12.

When layers 12 and 27 are heated after joining, stress may be generated which lead to some deleterious effects in the formed device and surrogate substrate. It is possible to form a stress-relieving layer between the diamond substrate and silicon dioxide layer and between the HBT device and silicon dioxide layer 27. This is illustrated as films 28 and 29 in FIG. 6. The stress relieving layer is a homogeneous or composite layer with material, i.e., Young's modulus, such that this layer will yield the application of stress before other layers.

While the bonding has been described using a silicon dioxide film polished to a desired surface roughness, other films are possible. For example, silicon or DLC may also be used. In the case of silicon, oxygen may be implanted into the bonding layers below their respective surfaces to form a compliant layer. The compliant layer is a layer equivalent to the stress-relieving layer. One would prefer to use a Si, SiC or DLC film versus an SiO_2 film, when, for example, improved thermal conductivity is desired.

It is also possible to choose the passivation/planarization material in the device being bonded to optimize the dielectric constant, thermal conductivity and resistivity adjacent to the active device. In particular, DLC is effective due to it relatively high thermal conductivity and low dielectric constant compared to other materials.

As shown in FIG. 5, the HBT device 14 typically is formed on substrate 20. After bonding the device to substrate 10, substrate 20 can be removed through a process such as polishing, or grinding and polishing. allowing access to backside contacts.

In a second embodiment of the invention, N 2D arrays of devices are bonded together by repeating the method described in the first embodiment N times. Starting with the bonded device shown in FIG. 7 (the HBT device is shown without the component detail as 30), the substrate 20 is removed and the exposed surface of device 30 is polished, if necessary, to a level of smoothness advantageous for wafer bonding. Polishing and grinding may be used during the removal of substrate 20. Another layer of silicon dioxide 31 is deposited on the

exposed surface of device 30 and polished to the desired surface roughness, in a manner as described above for layers 12 or 27 (FIG. 8).

A next wafer, shown without the device details as 32 with substrate 34 in FIG. 9 has a thin layer of silicon dioxide 33 formed on the surface opposite substrate 34. Film 33 is formed and polished in the same manner as films 11, 27 and 31. Film 33 is then bonded to the exposed surface of layer 31. The resulting device is shown in FIG. 10, after removal of the substrate 34. The upper surface of the second bonded device may again be polished, another silicon dioxide layer 35 deposited in preparation for bonding of a third device. This can be N times to produce an N-integrated device. The devices so bonded may be interconnected vertically.

Example

An example of the bonding between multiple devices is shown in FIGS. 11A, 11B and 12-15. FIGS. 11A, 11B and 12-15 illustrate how the bonding according to the present invention can be used to integrate N 2D arrays of devices, how they can be interconnected to form a vertically-integrated multi-wafer module, and how different technologies may be joined.

FIGS. 11A and 11B illustrate two devices to be bonded. In this example, the devices of FIGS. 11A and 11B are dissimilar integrated circuit wafers having interconnections. In FIG. 11A a symmetric-intrinsic HBT (SIHBT) wafer contains an SIHBT surrogate substrate 40, planarizing material 41 formed on substrate 40, SIHBT device 43 and interconnects 42 and 44, preferably formed of a metal. FIG. 11B illustrates a VCSEL device having a VCSEL substrate 45, planarizing material 46, VCSEL device 48 and interconnects 47 and 49, again preferably formed of metal. As shown in FIG. 12, the devices of FIGS. 11A and 11B are bonded in the method as described above, that is, a material such as silicon dioxide is deposited on the upper surface of each device and then polished to a surface roughness of about 5-10Å. A high degree of planarity is also desirable. The bonded devices are shown in FIG. 12.

Next, as illustrated in FIG. 13, substrate 40 is removed exposing interconnect 44. A via hole 50 is etched through planarizing material 41 and into planarizing material 46 to expose a portion of interconnect 47. While one via hole 50 is shown, it is to be understood that any number of vias may be formed in order to make the appropriate connection(s) to the

devices in the two bonded substrates.

Interconnect 51 is formed in via hole 50 interconnecting the devices 43 and 48. At this point the process could be stopped if only two wafers were required to be bonded. If one or more devices need to be further integrated, the process may continue by forming a bonding layer 52 made of, for example, silicon dioxide, which is then polished to a surface roughness of 5-10Å, in the same manner as described above. In this case, the process may include a step of filling any cavity formed in interconnect 50 to more easily produce a smooth surface of layer 52. The device, as shown in FIG. 14 is now ready to be bonded with another wafer, if desired.

For the wafers of different technologies, the planarizing material may be the same. The two different technologies are separated by the layers of planarizing material do not interact. Each only interacts with the planarizing material. Since the properties of the planarizing material are both well known and are commonly used in current processes, no new materials are needed to combine the technologies. The invention provides a very manufacturable manner of combining different technologies.

Moreover, all of the customization takes place at the end of the processing. Both wafers are separately manufactured and then bonded. The interconnection is performed after the bonding. Customization of combined technologies takes place at the end of the process. Whatever technology one needs may be obtained, and these technologies may be those that are readily and commercially available. The need for designing a new process is eliminated. More control over the final combined product is possible as well-defined and devices fabricated with a stable process may be selected for combining, unlike a new, unqualified combined process where little manufacturing, reliability or longer term information is available.

The bonding of a third wafer to the structure of FIG. 14 is illustrated in FIG. 15. It is noted that FIG. 15 illustrates an additional metalization 53 formed by etching planarizing material 41 and 46 to expose a portion of interconnect 60 of another device having elements 60-62. Interconnect 53 has an extended portion on the surface of planarizing material 41 to facilitate interconnection on another level. The device in the third wafer in this case can be a CMOS device 56 having interconnects 55 and 57. Another via is etched through planarizing material 58 and through bonding material 52, exposing a portion of interconnect 51 to allow

connection with interconnect 59. Interconnect 59 is also connected with interconnect 55 of CMOS device 56. Another interconnect 54 is formed by etching a via through materials 58 and 52 to expose a portion of interconnect 53. An interconnect 54 is formed to contact interconnect 53. It should be noted that FIG. 15 does not explicitly show the bonding layers formed between the devices but is to be understood that these are the devices are formed using the process described above in connection with the first embodiment.

What is also apparent from FIG. 15 that the present invention utilizes both sides of a contact. For example, if the pad at the top of contact 51 is a contact pad or a metal ling, then the bottom surface of the pad (or line) is connected with interconnect 47 lying under the pad (or line) while the top of the pad (or line) is connected with contact 59 overlapping with interconnect 55. This can reduce drive requirements.

FIG. 15 also illustrates the advantage of the invention of not being constrained to one layer (or possibly two layers) for circuit topography. One has the ability to design three dimensionally. Circuit layouts can be optimized if one is given the ability to separate a type or class of device from others where either the functioning or processing interferes or is incompatible. Circuit layouts are minimized in area since three dimensions are used instead of only two. For example, three conventional chips of nominally the same area with optionally different technologies can be implemented in one third the area by stacking vertically. The area reduction is even greater if one considers the reduced packaging requirements of the individual chips vs. the stacked chips. Stacking vertically is also conducive to the insertion of ground, bias, or other planes between chips or within a chip for improved signal isolation during routing.

Typically, in a system signals are amplified and then transmitted over buses between integrated circuits. This requires a lot of level-shifting, buses and compensation for various differences in signal levels amongst the elements making up the system. As one example, a pixel in a light detecting device receives a very small packet of charge which is then shifted out of the device and into a memory device. The light detecting device and the memory in this case may both be separate integrated circuits, requiring amplification of the charge packet through buffers and system buses between the pixel and memory device. The signal levels are then shifted down in order to store the information in a memory cell in the memory device. When the information in the memory is needed to be processed, the information is

then level-shifted again using more buffers and system buses to transmit the data over to a processor, which also may be formed using a separate integrated circuit. The power levels for the various signals are determined by the interconnection and the buses.

The present invention allows one to obtain element-to-element communication and addressability. In the present, the power levels of signals may be determined by the element, and not the interconnect, i.e., the system buses and drivers. As an example, as shown in FIG. 16A-16D, a first integrated circuit consisting of an array of pixels for sensing a light signal, etc. is fabricated on a first substrate (FIG. 16A). In simplified fashion, the a pixel 72 is formed in a semiconductor layer 71, which is formed on a substrate 70. On a second substrate is fabricated the memory device needed to store the information when it is shifted out of the pixel array, and is shown in FIG. 16B. A semiconductor layer 74 is formed on a substrate 73. Memory cells 75 are formed in layer 74. Lastly, a processor device for processing the information is manufactured on a third substrate shown in FIG. 16C. Various elements 78 are shown (in simplified form) in layer 77 formed on substrate 76. Each of the substrates may then be bonded together (with the pixel array on top in order to expose it to the light).

The three substrates may be bonded together. A surrogate substrate (not shown) may be attached to an upper surface of layer 71 using the techniques described above, and substrate 70 removed. The u-per surface of layer 74 of the memory device is then bonded to the surface exposed by removing substrate 70. Substrate 73 may then be removed, and the upper surface of layer 77 is bonded to the surface exposed by removing substrate 73. The surrogate substrate may be removed to exposed the pixels 72. The interconnections may be made directly between the three substrates, in the manner discussed above, eliminating the need for the numerous buffers and system buses required to interconnect the system when the system is designed using separate integrated devices. The bonded circuit is shown in FIG. 16D. It should be noted that FIG. 16D does not illustrate the various layers used to bond the different devices, and that portions of the layers 71, 74, and 77 may be removed during the removal of the corresponding substrates, as desired.

Another example would be a typical microprocessor where the microprocessor contains a certain amount of on-board ROM while a larger amount of storage is accessed via system buses on a separate RAM. In this case, the processor with the on-board ROM may be

fabricated on a first substrate and the memory may be fabricated on a second substrate. The two substrates are to be bonded together and the processor directly bonded to the memory device, again eliminating the need for system buses, level shifters and other buffers.

The present invention not only allows the fabrication of systems in a more compact and directly accessible manner, but also allows a smaller footprint. Each of the separate devices described above would take up at least three times the amount of space compared to the present invention they are stacked upon each other, assuming chips of about the same size.

A fourth embodiment of the invention uses the techniques described above to create the interconnect separately from the underlying integrated circuit. Typically, circuits require a number of levels of interconnect in order to provide all the complex functions required. Six or more levels of interconnect may be needed. This requires a significant amount of thermal processing, exposing the underlying active devices to higher thermal budgets and complicating the fabricating process. The present invention may be used to fabricate the active devices separately and then forming layers of interconnect by bonding according to the present invention. In particular, each level of interconnect may be formed on separate substrates, then bonded together and interconnected as needed. Several or all of the interconnect layers may be fabricated at one time. The bonded together or single interconnected substrate may then be bonded to the substrate having the active devices. Techniques similar to those described above for interconnecting the different wafers shown in FIG. 15 may be employed. When finished, the stack of interconnected layers may be bonded to the active devices.

This is illustrated in FIGS. 17A and 17B, where a stack of interconnect having layers 80-83 is bonded according to the principles of the invention and shown in FIG. 17A is then bonded to the integrated circuit shown in FIG. 16B or 16C.. FIG. 17B shows the completed device with the layers used in the bonding process omitted for clarity. In this case, the substrate of the integrated circuit may be removed and bonded to a more favorable thermal material, such as diamond-like carbon. With this embodiment, one can obtain tighter processing control by not having to compensate or make compromises for the various effects of the increased thermal budget due to the typical processing of the multiple layers of integrated circuit interconnection on top of the active devices.

Another application of the invention is the selection of the interconnect layers. By being able to separately process the interconnect, more design flexibility may by obtained. Certain layers, for example those handling high speed signals, may be more critical than others. The critical levels may be separated from each other by other non-critical layers to minimize overlap. Conversely, non-critical layers may be put in adjacent layers when the overlap is not a problem for high speed operation of the device.

Apparent from the above embodiments, the substrate of the integrated circuits may be completely removed in the above embodiments. The result is a 2-D array of device elements immersed in insulative planarizing material. One example of this is shown in FIG. 18. Each of the elements may be completely isolated from every other element, i.e., a 2-D array of devices as opposed to a circuit layer. A second wafer to be bonded may be processed in the same way, giving another 2-D array of device elements. The arrays of devices may then be interconnected in a desired manner to create circuits, subcircuits, etc. This can be extended to bonding different technologies together, for example, CMOS and bipolar, to create a BiCMOS wafer. In this case the most advanced CMOS and bipolar technologies may be combined since the two wafers are separately processed. One can then, when needing to create a combined technology device or circuit, use existing advanced, qualified technologies rather than having to design a new combined process or settle for an existing combined technology which does not use and cannot take advantage of the most advanced technologies or evolutions in technologies.

Third wafer and subsequent wafers may also be processed where the substrate is removed to create a 2-D array of devices ready to be bonded to the first and second arrays. The third device may be yet another technology. FIG. 19 gives an example.

While particular devices and materials have been described in connection with the first and second embodiments, the invention is not so limited. The invention is applicable to any type of device formed on any type of substrate. Moreover, any type of technology may be used to fabricate the devices being bonded. For example, GaAs devices on a GaAs substrate may be bonded to HBT devices. Also, silicon-based devices formed on silicon wafers may also be bonded to either the GaAs-based devices or the HBT type devices. Technologies such as CMOS, BiCMOS, npn and pnp HBT, VCSEL, PIN, HFET, MESFET, MOSFET, and JFET may also be used.

The method according to the invention provides a three-dimensional, laminar integrated circuit structure. The device is a multi-chip module having a high integration density with reduced interconnection parasitics compared to other multi-chip modules. The module offers great flexibility as it can combine different devices and different technologies.

Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.



Claims:

1. A method of integrating workpieces each having an first surface and an opposing second surface, comprising:

polishing respective first surfaces of first, second and third workpieces each to a desired surface roughness;

bonding together said first surfaces of said first and second workpieces;

polishing a second surface of one of said first and second workpieces after bonding to said surface roughness; and

bonding said first surface of said third workpiece to said polished second surface.

2. A method as recited in claim 1, comprising:

forming a thin first material on a second material to obtain said first workpiece;

forming a thin third material on a fourth material to obtain said second workpiece;

forming a thin fifth material on a sixth material to obtain said third workpiece; and

polishing said first, third and fifth materials as said step of polishing first surfaces.

3. A method as recited in claim 2, comprising:

forming said first, third and fifth materials each of a material having a high thermal conductivity and a high dielectric constant.

4. A method as recited in claim 2, comprising:

forming said first, third and fifth materials selected from the group consisting of silicon dioxide, silicon and diamond-like carbon.

5. A method as recited in claim 2, comprising:

forming said first material to a thickness of about 1-10 times a surface non-planarity of said second material;

forming said third material to a thickness of about 1-10 times a surface non-planarity of said fourth material

forming said fifth material to a thickness of about 1-10 times a surface non-planarity of said sixth material.

6. A method as recited in claim 1, comprising:

forming a first semiconductor device on a first substrate as said first workpiece;

forming a second semiconductor device on a second substrate as said second workpiece; and

forming a third semiconductor device on a third substrate as said third workpiece.

7. A method as recited in claim 6, comprising:

forming a first material on an upper surface said first semiconductor device;

forming a second material on an upper surface of said second semiconductor device;

polishing each of said first and second materials to said surface roughness; and

bonding said first and second polished materials.

8. A method as recited in claim 6, comprising:

polishing an exposed surface of said one of said first and second semiconductor devices to said surface roughness after bonding said first and second workpieces;

forming a third material on said third semiconductor device;

polishing said third surface to said surface roughness; and

bonding said polished third surface with said polished exposed surface.

9. A method as recited in claim 6, comprising:

polishing an exposed surface of said one of said first and second semiconductor devices to said surface roughness after bonding said first and second workpieces;

forming N-2 workpieces each having a semiconductor device formed on a substrate, where N is an integer having a value of at least 3;

polishing surfaces of said N-2 workpieces each to said surface roughness; and

bonding said N-2 semiconductor devices to said bonded first and second semiconductor workpieces to obtain an N-integrated bonded device.

10. A method as recited in claim 9, comprising:

removing respective substrates of said N-2 workpieces after bonding said respective substrates.

11. A method as recited in claim 1, comprising:

using a first substrate as said first workpiece;

forming a first integrated circuit on a second substrate as said second workpiece;

polishing a first surface of said first substrate to said surface roughness;

polishing a second surface of said integrated circuit to said surface roughness;

bonding said first and second surfaces;

forming a second integrated circuit on a third substrate as said third workpiece;

polishing a third surface of said integrated circuit to said surface roughness; and

* C L M S *

bonding said third surface to said second workpiece.

12. A method as recited in claim 11, comprising:

forming a first material on a surface said first substrate;

polishing said first material to said surface roughness;

forming second and third materials on respective surfaces of said first and second integrated circuits; and

polishing said second and third materials to said surface roughness.

13. A method as recited in claim 12, comprising:

forming said first material to a thickness of about 1-10 times a surface non-planarity of said surface of said first substrate; and

forming said second and third materials each to a thickness of about 1-10 times a surface non-planarity of respective surfaces of said first and second integrated circuits.

14. A method as recited in claim 11, comprising:

using a surrogate substrate selected from the group consisting of diamond, diamond-like carbon and silicon carbide as said first workpiece.

15. A method as recited in claim 1, comprising:

forming N thin films on a first material to obtain said first workpiece;

polishing an uppermost one of said N thin films to said surface roughness;

forming M thin films on a second material to obtain said second workpiece; and

polishing an uppermost one of said M thin films to said surface roughness;

where N and M are integers each having a value of at least 2.

16. A method as recited in claim 15, comprising at least one of:

polishing at least plural of said N thin films; and

polishing at least plural of said M thin films.

17. A method as recited in claim 1, comprising:

using a surrogate substrate as said first workpiece;

forming a stress-relieving layer on said surrogate substrate;

forming a thin film on said stress-relieving layer; and

polishing said thin film to said surface roughness.

18. A method as recited in claim 1, comprising:

forming a thin silicon film on a material to obtain said first workpiece;

* C L M S *

implanting oxygen into a surface of said first thin; and

polishing said first thin silicon to said surface roughness.

19. A method as recited in claim 1, comprising:

polishing said respective first surfaces and said second surface to a desired planarity.

20. A method as recited in claim 6, comprising:

polishing surfaces of said first through third semiconductor devices to a desired planarity.

21. A method as recited in claim 1, comprising:

forming a first semiconductor device in said first workpiece;

forming a second semiconductor device in said second workpiece; and

interconnecting said first and second semiconductor devices after bonding said first and second workpieces.

22. A method as recited in claim 21, comprising·

interconnecting between respective individual devices in said first and second semiconductor devices.

23. A method as recited in claim 21, comprising:

interconnecting between respective circuits in said first and second semiconductor devices.

24. A method as recited in claim 21, comprising:

forming a third semiconductor device as said third workpiece; and

interconnecting said first, second and third semiconductor devices.

25. A method as recited in claim 24, comprising:

forming N-3 semiconductor devices on respective substrates, where N is an integer haivng a value of at least 4;

bonding said N-3 devices with said first, second and third workpieces; and

interconnecting said N devices.

26. A method as recited in claim 24, comprising:

after bonding said first and second semiconductor devices, removing a substrate of one of said first and second semiconductor devices;

polishing a surface exposed by said removing step to said surface roughness;

bonding said third semiconductor device to said exposed surface; and

* C L M S *

removing a substrate of said third semiconductor device.

27. A method as recited in claim 26, wherein:

interconnecting said first, second and third semiconductor devices comprises bonding a multi-layer interconnect to said third semiconductor device.

28. A method as recited in claim 1, comprising:

forming first and second semiconductor devices as said first and second workpieces;

forming a multi-layer interconnection as said third workpiece; and

interconnecting said first and second semiconductor devices using said multi-layer interconnection.

29. A method as recited in claim 1, comprising:

forming respective first, second and third semiconductor devices as said first, second and third workpieces;

forming a multi-layer interconnection;

bonding said interconnection to said first, second and third workpieces; and

interconnecting said first, second and third semiconductor devices using said interconnection.

30. A method as recited in claim 1, comprising:

forming respective first, second and third components of an electrical system as said first, second and third workpieces; and

interconnecting said first, second and third components.

31. A method as recited in claim 30, wherein:

said interconnecting step comprises bonding a multi-layer interconnection to one of said workpieces.

32. A method as recited in claim 1, comprising:

forming a two-dimensional array of unconnected devices in a substrate as each of said first and second workpieces; and

connecting said first devices to said second devices.

32. A method as recited in claim 1, comprising:

forming a substrate of a high thermal conductivity material as said first workpiece;

forming a two-dimensional array of unconnected devices in a substrate as each of said second and third workpieces; and

* C L M S *

interconnecting said first devices and said second devices.

33. A method as recited in claim 32, comprising:

said second and third workpieces being of different technologies.

34. A method as recited in claim 33, wherein:

each of said first and second workpieces comprise a technology selected from the group consisting of CMOS, BiCMOS, npn and pnp HBT, VCSEL, PIN, HFET, MESFET, MOSFET, and JFET.

35. A method as recited in claim 1, comprising:

forming said first workpiece as a semiconductor device using a first technology; and

forming said second workpiece as a semiconductor device using a second technology different than said first technology.

36. A method as recited in claim 1, comprising:

forming said first workpiece as a surrogate substrate;

forming said second workpiece as a semiconductor device using a first technology; and

forming said third workpiece as a semiconductor device using a second technology different than said first technology.

37. A method as recited in claim 1, comprising:

polishing respective first surfaces of first, second and third workpieces each to a surface roughness of no more than about 5-10 Å.

38. A method of integrating semiconductor devices, comprising:

bonding a first semiconductor device having a first substrate to a second semiconductor device having a second substrate;

removing a portion of said first substrate to expose a remaining portion of said first semiconductor device; and

interconnecting said first and second semiconductor devices.

39. A method as recited in claim 38, wherein:

said interconnecting comprises bonding a multi-layer interconnect to said remaining portion of said first device.

40. A method as recited in claim 38, comprising:

removing substantially all of said first substrate.

41. A method as recited in claim 38, comprising:

planarizing surfaces of said first and second devices; and

bonding said surfaces.

42. A method as recited in claim 38, comprising:

bonding a third semiconductor device to said remaining portion; and

interconnecting said first, second and third semiconductor devices.

43. A method as recited in claim 38, comprising:

bonding a surrogate substrate to said remaining portion of said first device; and

removing said second substrate to expose a remaining portion of said second device.

44. A method as recited in claim 38, comprising:

bonding said second device to a surrograte substrate;

removing at least a portion of said second substrate of said second device to expose a remaining portion of said second device; and

bonding said first device to said remaining portion of said second device.

45. A method as recited in claim 44, comprising:

removing substantially all of each of said first and second substrates.

46. A method as recited in claim 44, comprising:

bonding a third semiconductor device to said remaining portion of said first device; and

interconnecting said first, second and third semiconductor devices.

47. A method as recited in claim 46, comprising:

removing at least a portion of a third substrate of said third device to expose a remaining portion of said third device.

48. A method as recited in claim 47, comprising:

removing substantially all of said first, second and third substrates.

49. A method as recited in claim 47, comprising:

bonding a multi-layer interconnect to said remaining portion of said third device.

50. A method as recited in claim 38, comprising:

forming N semiconductor devices on respective substrates, where N is a nonzero positive integer;

bonding said N devices to said first and second devices;



interconnecting said first, second and N devices.

51. A method as recited in claim 50, comprising:

removing at least a portion of substrates of each of said N devices to expose respecitve remaining portions; and

bonding an (N+1)th device to a remaining portion of an Nth device.

52. A method as recited in claim 51, comprising:

removing substantially all of said first and second substrates and said substrates of said N devices.

53. A bonded device, comprising:

a first workpiece having a first surface with a desired surface roughness;

a second workpiece having second and third surfaces each with said surface roughness;

a third workpiece having a fourth surface with said surface roughness;

said first and second surfaces bonded together; and

said third and fourth surfaces bonded together.

54. A device as recited in claim 53, wherein:

said first workpiece comprises a thin first material disposed on a second material;

said second workpiece comprises a thin third material disposed on a fourth material;

said third workpiece comprises a thin fifth material disposed on a sixth material;

a surface of said thin first material comprises said first surface;

a surface of said thin third material comprises said second surface; and

a surface of said thin fifth material comprises said fourth surface.

55. A device as recited in claim 54, wherein:

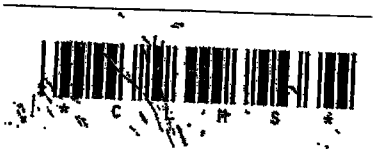
each of said thin first, second and third materials comprises a material having a high thermal conductivity and a high dielectric constant.

56. A device as recited in claim 54, wherein:

each of said thin first, second and third materials comprises a material selected from the group consisting of silicon dioxide, silicon and diamond-like silicon carbide.

57. A device as recited in claim 54, comprising:

said thin first material having a thickness of about 1-10 times a surface non-planarity of said second material;



said thin third material having a thickness of about 1-10 times a surface non-planarity of said fourth material; and

said thin fifth material having a thickness of about 1-10 times a surface non-planarity of said sixth material.

58. A device as recited in claim 54, wherein:

said thin first material comprises a plurality of thin layers, an uppermost one of said layers comprising said first surface;

said thin third material comprises a plurality of thin layers, an uppermost one of said layers comprising said second surface; and

said thin fifth material comprises a plurality of thin layers, an uppermost one of said layers comprising said fourth surface.

59. A device as recited in claim 53, wherein:

said first workpiece comprises a first semiconductor device;

said second workpiece comprises a second semiconductor device; and

said third workpiece comprises a third semiconductor device.

60. A device as recited in claim 59, wherein:

said first semiconductor device comprises a first integrated circuit having one surface as said first surface; and

said second semiconductor device comprises a second integrated circuit having one surface as said second surface and an opposing surface as said third surface; and

said third semiconductor device comprises a third integrated circuit having one surface as said fourth surface.

61. A device as recited in claim 60, wherein:

each of said first, second and third semiconducotr devices comprises a two-dimensional array of unconnected devices.

62. A device as recited in claim 53, comprising:

said first workpiece comprises a first semiconductor device formed in a first substrate;

said second workpiece comprises a second semiconductor device formed in a second substrate, at least a portion of second substrate being removed; and

said third workpiece comprises a third semiconductor device formed in a third substrate, at least a portion of third substrate being removed.



63. A device as recited in claim 62, comprising:

said second semiconductor device comprises said second semiconductor device formed in a second substrate, substantially all of second substrate being removed; and

said third semiconductor device comprises said third semiconductor device formed in a third substrate, substantially all of third substrate being removed.

64. A device as recited in claim 53, wherein:

said first workpiece comprises a surrogate substrate; and

said second and third workpieces comprises respective first and second semiconductor devices.

65. A device as recited in claim 64, wherein:

said surrogate substrate comprises a thin first material disposed on a second material;

said thin first material comprises said first surface;

said second and third semiconductor devices respectively comprise thin second and third materials disposed on respective upper surfaces;

said thin second material comprises said second surface; and

said thin third material comprises said fourth surface.

66. A device as recited in claim 65, comprising:

said thin first material having a thickness of about 1-10 times a surface non-planarity of said second material;

said thin second material having a thickness of about 1-10 times a surface non-planarity of said upper surface of said second device; and

said thin third material having a thickness of about 1-10 times a surface non-planarity of said upper surface of said third device.

67. A device as recited in claim 53, wherein at least one of:

said first workpiece comprises a thin first material, a second material and a stress-relieving material formed between said thin first material and said second material, a surface of said thin first material comprising said first surface; and

said second workpiece comprises a thin third material, a fourth material and a stress-relieving material formed between said thin third material and said fourth material, a surface of said thin third material comprising said second surface.

68. A device as recited in claim 53, wherein:

* C L M S *

said first workpiece comprises a surrogate substrate; and

said second and third workpieces each comprise a semiconductor device.

69. A device as recited in claim 53, wherein:

said third workpiece comprises a surrogate substrate; and

said first and second workpieces each comprise a semiconductor device.

70. A device as recited in claim 53, wherein:

said first and second workpieces each comprises a semiconductor device; and

said third workpiece comprises a multi-layer interconnection.

71. A device as recited in claim 53, comprising:

said first and second workpieces each comprises a semiconductor circuit; and

said interconnection connecting individual devices from said circuits of said first and second devices together.

72. A device as recited in claim 53, comprising:

said first and second workpieces each comprises an integrated circuit; and

said interconnection connecting individual circuits from said integrated circuits of said first and second devices together.

73. A device as recited in claim 53, comprising:

said surface roughness being no more than 5-10Å.

74. An integrated device, comprising:

a first semiconductor device;

a second semiconductor device, comprised of a layer of devices formed on a substrate which has been at least partially removed, bonded to said first semiconductor device; and

interconnections connecting said first and second semiconductor devices.

75. A device as recited in claim 74, wherein:

said second device comprises said layer of devices formed on a substrate which has been substantially removed.

76. A device as recited in claim 74, comprising:

a third semiconductor device, comprised of a layer of devices formed on a substrate which has been at least partially removed, bonded to said second device.

77. A device as recited in claim 76, wherein:

said second device comprises said layer of devices formed on a substrate which has



been substantially removed; and

said third device comprises said layer of devices formed on a substrate which has been substantially removed.

78. A device as recited in claim 74, wherein:

said interconnections comprise a multi-layer interconnect bonded to said second device.

79. A device as recited in claim 74, wherein:

said first device comprises a layer of devices formed on a substrate which has been substantially removed bonded to a surrogate substrate.

80. A device as recited in claim 79, wherein:

said second device comprises said layer of devices formed on a substrate which has been substantially removed.

81. A device as recited in claim 74, wherein:

said second and third workpieces being of different technologies.

82. A device as recited in claim 81, wherein:

each of said first and second workpieces comprise a technology selected from the group consisting of CMOS, BiCMOS, npn and pnp HBT, VCSEL, PIN, HFET, MESFET, MOSFET, and JFET.

