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4 **Formation Of Raised Source/Drain Structures In NFET With Embedded SiGe**
5 **in PFET**
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8 **Abstract**
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11 A structure and method for forming raised source/drain structures
12 in a NFET device and embedded SiGe source/drains in a PFET device. We
13 provide a NFET gate structure over a NFET region in a substrate and PFET gate
14 structure over a PFET region. We provide NFET SDE regions adjacent to the
15 NFET gate and provide PFET SDE regions adjacent to the PFET gate. We form
16 recesses in the PFET region in the substrate adjacent to the PFET second
17 spacers. We form a PFET embedded source/drain stressor in the recesses. We
18 form a NFET S/D epitaxial Si layer over the NFET SDE regions and a PFET S/D
19 epitaxial Si layer over PFET embedded source/drain stressor. The epitaxial Si
20 layer over PFET embedded source/drain stressor is consumed in a subsequent
21 salicide step to form a stable and low resistivity silicide over the PFET embedded
22 source/drain stressor. We perform a NFET S/D implant by implanting N-type ions
23 into NFET region adjacent to the NFET gate structure and into the NFET S/D
24 stressor Si layer to form the raised NFET source/drains.
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26 **Fig. 10**