WHAT IS CLAIMED IS:

1. A nonvolatile memory device comprising:

a first memory stack comprising a plurality of first memory cells vertically stacked on each other;

a second memory stack comprising a plurality of second memory cells vertically stacked on each other, wherein the second memory stack is vertically stacked on the first memory stack; and

a control logic configured to set a voltage level of a second voltage applied for a second memory operation to a second memory cell of the plurality of second memory cells in the second memory stack based on a first voltage applied to a first memory cell of the plurality of first memory cells in the first memory stack in a first memory operation,

wherein cell characteristics of the first memory cell are determined using the first voltage.

2. The nonvolatile memory device of claim 1,

wherein the first memory stack and the second memory stack are separately formed through an independent channel hole forming process.

3. The nonvolatile memory device of claim 1 or claim 2,

wherein control logic is configured to:

perform the first memory operation on the first memory cell using a plurality of

voltages;

complete the first memory operation using the first voltage among the plurality of voltages, wherein the cell characteristics of the first memory cell is determined at the first voltage;

set the second voltage based on the first voltage; and

perform the second memory operation on the second memory cell using the second voltage.

4. The nonvolatile memory device of any one of claims 1 to 3, wherein:

the first memory stack has a first channel hole and the second memory stack has a second channel hole connected to the first channel hole;

an etch profile of the first channel hole is substantially the same as an etch profile of the second channel hole; and

a bottom of the second channel hole has a width smaller than a width of a top of the first channel hole.

5. The nonvolatile memory device of any one of claims 1 to 4, wherein:

each of the plurality of first memory cells is connected to a corresponding word line of first through N^{th} word lines according to a stacked order of each of the plurality of the first through N^{th} word lines in the first memory stack;

each of the plurality of second memory cells is connected to a corresponding word line of $(N+1)^{th}$ through M^{th} word lines according to a stacked order of each of the plurality

of $(N+1)^{th}$ through M^{th} in the second memory stack;

the first voltage is a voltage applied to the first memory cell connected to a k^{th} word line;

the second voltage is a voltage applied to the second memory cell connected to a $(k+N)^{th}$ word line;

the k^{th} word line and the $(k+N)^{th}$ word line are positioned at substantially the same level in the first memory stack and the second memory stack respectively; and

N is an integer of one or greater, M is an integer greater than N, and k is an integer between one and N inclusive.

6. The nonvolatile memory device of claim 5,

wherein the control logic is further configured to set a voltage level of the second voltage to be the same as a voltage level of the first voltage.

7. The nonvolatile memory device of claim 5,

wherein the control logic is further configured to set a voltage level of the second voltage to be higher or lower than a voltage level of the first voltage by an offset.

8. The nonvolatile memory device of claim 7,

wherein the control logic is further configured to:

apply a plurality of first read voltages to perform a first read operation on the first memory cell, wherein the first read operation is completed at a first read voltage of the

plurality of first read voltages;

apply a plurality of second read voltages to perform a second read operation on the second memory cell, wherein the second read operation is completed at a second read voltage of the plurality of second read voltages of the second read operation; and

determine a voltage level difference between the first read voltage and the second read voltage as the offset.

9. The nonvolatile memory device of claim 7,

wherein the control logic is configured to:

apply a plurality of first program voltages to perform a first program operation on the first memory cell, wherein the first program operation is completed at a first program voltage of the plurality of first program voltages;

apply a plurality of second program voltages to perform a second program operation on the second memory cell, wherein the second program operation is completed at a second program voltage of the plurality of second program voltages; and

determine a voltage level difference between the first program voltage and the second program voltage as the offset.

10. The nonvolatile memory device of claim 5, wherein:

the first voltage is a first read voltage for determining a data state of the first memory cell;

the second voltage is a second read voltage for determining a data state of the

second memory cell; and

the control logic is configured to set a voltage level of the second read voltage based on a voltage level of the first read voltage.

11. The nonvolatile memory device of claim 10,

wherein, the control logic is further configured to, when an error correction for the first memory cell fails, determine a voltage level of the first read voltage by sequentially applying a plurality of read retry voltages to the first memory cell, and

wherein when an error correction for the second memory cell fails, the control logic is configured to read data from the second memory cell by applying the second read voltage.

12. The nonvolatile memory device of claim 5, wherein:

the first voltage is a first program voltage for programming data in the first memory cell;

the second voltage is a second program voltage applied for programming data in the second memory cell as a start bias voltage; and

the control logic is configured to set a voltage level of the second program voltage based on a voltage level of the first program voltage.

13. The nonvolatile memory device of claim 12,

wherein, the control logic is configured to, when a program operation is performed

on the first memory cell, determine the voltage level of the first program voltage by sequentially applying a plurality of program voltages to the first memory cell, and when a program operation is performed on the second memory cell, program data therein by applying the second program voltage as a start bias voltage.

14. The nonvolatile memory device of any one of claims 5 to 13,

wherein the control logic is further configured to:

program the first memory cell connected to the k^{th} word line; and

after the programming for the first memory cells connected to the k^{th} word line is completed, program the second memory cell connected to the $(k+N)^{th}$ word.

15. The nonvolatile memory device of claim 14,

wherein the control logic is further configured to, after the programming of the second memory cell connected to the $(k+N)^{th}$ word line is completed, program another first memory cell connected to the $(k+1)^{th}$ word line.

16. The nonvolatile memory device of any one of claims 5 to 13, wherein:

the control logic is further configured to:

program data using a first bit program mode in each of the plurality of first memory cells connected to first through p^{th} word lines;

program data using a second bit program mode in each of the first memory cells connected to $(p+1)^{th}$ through N^{th} word lines and in each of the second memory cells

connected to $(N+1)^{th}$ through q^{th} word lines;

program data using a third bit program mode in each of the second memory cells connected to $(q+1)^{th}$ through M^{th} word lines; and

p is an integer less than N and q is an integer between (N+2) and (M-2) inclusive.

17. The nonvolatile memory device of claim 16,

wherein more bits per a memory cell are programmed in the second bit program mode than in each of the first and third bit program modes.

18. A nonvolatile memory device comprising:

a first memory stack including a plurality of first memory cells sequentially connected to first through N^{th} word lines;

a second memory stack including a plurality of second memory cells sequentially connected to $(N+1)^{th}$ through M^{th} (M is an integer greater than N+1) word lines; and

a control logic configured to sequentially program a first memory cell of the plurality of first memory cells connected to one of the first through N^{th} word lines in the first memory stack and a second memory cell of the plurality of second memory cells connected to one of the $(N+1)^{th}$ through M^{th} word lines,

wherein the one of the first through N^{th} word lines and the one of the $(N+1)^{th}$ through M^{th} word lines are positioned at the same level in the first and second memory stacks respectively, and

wherein the control logic is configured to set a voltage level of a second voltage

applied to the second memory cell based on a first voltage applied to the first memory cell.

19. The nonvolatile memory device of claim 18,

wherein the control logic is further configured to repeat a pair of programming a remaining one of the plurality of first memory cells at a third program voltage and programming a remaining one of the plurality of second memory cells by applying a fourth voltage determined based on the third program voltage,

wherein the remaining one of the plurality of first memory cells and the remaining one of the plurality of second memory cells are positioned at the same level in the first memory stack and the second memory stack respectively.

20. A method of programming a memory device comprising a first memory stack and a second memory stack, the method comprising:

completing a program operation on one of a plurality of first memory cells comprised in the first memory stack using a first program voltage;

determining a second program voltage based on the first program voltage; and

programming one of a plurality of second memory cells comprised in the second memory stack by applying the second program voltage to the one of the plurality of the second memory cells as a start bias voltage,

wherein the one of the plurality of first memory cells and the one of the plurality of second memory cells are positioned at the same level in the first memory stack and the second memory stack respectively.