

CLAIMS:

1. A digital comparator coupled to a pair of pull-up resistors and a pair of pull-down resistors whereby both pairs of resistors are coupled to a gate terminal of an output stage, the digital comparator comprising:

a single-edge detector stage configured to detect a first rising edge in a received first digital signal, and to detect a first falling edge in a received second digital signal, whereby when the first rising edge is detected and when the first falling edge is not simultaneously detected, a detector node is set to a low voltage level, and when the first falling edge is detected, the detector node is set to a high voltage level;

a consecutive two-edge detector stage coupled to the single-edge detector stage, the consecutive two-edge detector stage configured to detect the voltage level of the detector node, a consecutive second rising edge in the received first digital signal and a consecutive second falling edge in the received second digital signal,

whereby when the consecutive second rising edge is detected and when the voltage level of the detector node is simultaneously detected to be at a low voltage level, the consecutive two-edge detector stage causes one of the pair of pull-up resistors to pull up a voltage at the gate terminal, and

when the consecutive second falling edge is detected and when the voltage level of the detector node is simultaneously detected to be at a high voltage level, the consecutive two-edge detector stage causes one of the pair of pull-down resistors to pull down the voltage at the gate terminal;

a consecutive three-edge detector stage coupled to the single-edge and the consecutive two-edge detector stages, the consecutive three-edge detector stage configured to detect the voltage level of the detector node, a consecutive third rising edge in the received first digital signal and a consecutive third falling edge in the received second digital signal,

whereby when the consecutive third rising edge is detected and when the voltage level of the detector node is simultaneously detected to be at a low voltage level, the consecutive three-edge detector stage causes the other one of the pair of pull-up resistors to pull up the voltage at the gate terminal, and

when the consecutive third falling edge is detected and when the voltage level of the detector node is simultaneously detected to be at a high voltage level, the consecutive three-edge detector stage causes the other one of the pair of pull-down resistors to pull down the voltage at the gate terminal.

2. The digital comparator according to claim 1, whereby when the consecutive two-edge detector stage and the consecutive three-edge detector stage detects a high voltage level at the detector node, the consecutive two-edge and three-edge detector stages cause the pair of pull-up resistors to be disabled.
3. The digital comparator according to claim 1, whereby when the consecutive two-edge detector stage and the consecutive three-edge detector stage detects a low voltage level at the detector node, the consecutive two-edge and three-edge detector stages cause the pair of pull-down resistors to be disabled.
4. The digital comparator according to claim 1, wherein level shifters are provided at inputs of the single-edge detector stage, at outputs of the consecutive two-edge detector stage and the consecutive three-edge detector stage.
5. A digital low-dropout circuit having the digital comparator according to claim 1, the digital low-dropout circuit using the output stage to generate a stable output voltage, the circuit comprising:
 - a first inverter ring oscillator that is controllable by an output voltage of the output stage to generate the first digital signal; and
 - a second inverter ring oscillator that is controllable by a reference voltage to generate the second digital signal.
6. The digital low-dropout circuit according to claim 5 wherein a sub-digital comparator is provided to control a pseudo-voltage of the digital comparator.
7. The digital low-dropout circuit according to claim 6 whereby the sub-digital comparator comprises:
 - a differential amplifier having a first input coupled to a voltage divider and a second input coupled to a third inverter ring oscillator that is controllable by the reference voltage.
8. The digital low-dropout circuit according to claim 5 wherein a Miller capacitor is provided between the gate terminal and an output node of the output stage.
9. The digital low-dropout circuit according to claim 5 wherein a feed-forward capacitor is provided between an output node of the output stage and the input of the second inverter ring oscillator.

10. A method of controlling a digital comparator that is coupled to a pair of pull-up resistors and a pair of pull-down resistors whereby both pairs of resistors are coupled to a gate terminal of an output stage, the method comprising:

detecting, using a single-edge detector stage, a first rising edge in a received first digital signal, and a first falling edge in a received second digital signal, whereby when the first rising edge is detected and when the first falling edge is not simultaneously detected, setting a detector node to a low voltage level, and when the first falling edge is detected, setting the detector node to a high voltage level;

detecting, using a consecutive two-edge detector stage coupled to the single-edge detector stage, the voltage level of the detector node, a consecutive second rising edge in the received first digital signal and a consecutive second falling edge in the received second digital signal,

whereby when the consecutive second rising edge is detected and when the voltage level of the detector node is simultaneously detected to be at a low voltage level, causing one of the pair of pull-up resistors to pull up a voltage at the gate terminal, and

when the consecutive second falling edge is detected and when the voltage level of the detector node is simultaneously detected to be at a high voltage level, causing one of the pair of pull-down resistors to pull down the voltage at the gate terminal;

detecting, a consecutive three-edge detector stage coupled to the single-edge and the consecutive two-edge detector stages, the voltage level of the detector node, a consecutive third rising edge in the received first digital signal and a consecutive third falling edge in the received second digital signal,

whereby when the consecutive third rising edge is detected and when the voltage level of the detector node is simultaneously detected to be at a low voltage level, causing the other one of the pair of pull-up resistors to pull up the voltage at the gate terminal, and

when the consecutive third falling edge is detected and when the voltage level of the detector node is simultaneously detected to be at a high voltage level, causing the other one of the pair of pull-down resistors to pull down the voltage at the gate terminal.

11. The method according to claim 10, whereby when the consecutive two-edge detector stage and the consecutive three-edge detector stage detects a high voltage level at the

detector node, the method comprises the step of causing the pair of pull-up resistors to be disabled.

12. The method according to claim 10, whereby when the consecutive two-edge detector stage and the consecutive three-edge detector stage detects a low voltage level at the detector node, the method comprises the step of causing the pair of pull-down resistors to be disabled.
13. The method according to claim 10, wherein level shifters are provided at inputs of the single-edge detector stage, at outputs of the consecutive two-edge detector and at outputs of the consecutive three-edge detector stage.