

SEMICONDUCTOR PACKAGE STRUCTURE AND MANUFACTURING METHOD

ABSTRACT

The embodiments of the present application disclose a semiconductor package structure and a manufacturing method. The semiconductor package structure includes: a first base plate provided with a first surface; a first chip stack body located on the first base plate, where the first chip stack body includes a plurality of first semiconductor chips that are successively stacked onto one another in a direction perpendicular to the first base plate, and is electrically connected to the first surface of the first base plate; an interposer layer located on the chip stack body and provided with a first interconnection surface, where the first interconnection surface is provided with a first interconnection region and a second interconnection region, and the first interconnection region is electrically connected to the first base plate; and a molding layer configured to seal the first chip stack body, the interposer layer and the first surface of the first base plate. The first interconnection region is unsealed by the molding layer, and the second interconnection region is sealed by the molding layer. A first material layer is formed on a sidewall between the first interconnection region and a top surface of the molding layer on the second interconnection region.

[Fig. 1]