

The invention claimed is :

1. A method to evaluate a semiconductor-superconductor heterojunction for use in a qubit register of a topological quantum computer, the method comprising:  
measuring a radio-frequency (RF) junction admittance of the semiconductor-superconductor heterojunction to obtain mapping data;  
finding by analysis of the mapping data one or more regions of a parameter space consistent with an unbroken topological phase of the semiconductor-superconductor heterojunction;  
measuring a sub-RF conductance including a non-local conductance of the semiconductor-superconductor heterojunction in each of the one or more regions of the parameter space to obtain refinement data; and  
finding by analysis of the refinement data a boundary of the unbroken topological phase in the parameter space and a topological gap of the semiconductor-superconductor heterojunction for at least one of the one or more regions of the parameter space.
2. The method of claim 1 wherein the analysis of the mapping data includes density-based clustering on zero-bias peak data from opposite ends of the semiconductor-superconductor heterojunction.
3. The method of claim 1 further comprising validating a zero-bias peak (ZBP) in each of the one or more regions by checking stability of the ZBP to variations in cutter-gate voltage.
4. The method of claim 1 wherein the analysis of the refinement data includes verifying gap closure at the boundary of each of the one or more regions of the parameter space.
5. The method of claim 1 wherein the semiconductor-superconductor heterojunction is one of a series of analogously prepared semiconductor-superconductor heterojunctions, the method further comprising meta-analysis of zero-bias peak data across the series to compute a probability of finding a topological region in another analogously prepared semiconductor-superconductor heterojunction.
6. The method of claim 1 wherein measuring the sub-RF conductance includes enacting local and non-local conductance measurement suitable for extracting an energy gap of the

semiconductor-superconductor heterojunction.

7. The method of claim 1 wherein the semiconductor-superconductor heterojunction comprises a semiconductor wire and at least three terminals supporting admittance and conductance measurement at opposite ends of the semiconductor wire.

8. The method of claim 1 wherein the semiconductor-superconductor heterojunction comprises a plurality of electrostatic control terminals.

9. An instrument configured to evaluate a semiconductor-superconductor heterojunction for use in a qubit register of a topological quantum computer, the instrument comprising:

a controller having a processor and computer memory coupled operatively to the processor,  
the controller being configured to:

measure a radio-frequency (RF) junction admittance of the semiconductor-superconductor heterojunction to obtain mapping data;

find by analysis of the mapping data one or more regions of a parameter space consistent with an unbroken topological phase of the semiconductor-superconductor heterojunction;

measure a sub-RF conductance including a non-local conductance of the semiconductor-superconductor heterojunction in each of the one or more regions of the parameter space to obtain refinement data; and

find by analysis of the refinement data a boundary of the unbroken topological phase in the parameter space and a topological gap of the semiconductor-superconductor heterojunction for at least one of the one or more regions of the parameter space.

10. The instrument of claim 9 wherein the controller is configured to analyze the mapping data using density-based clustering on zero-bias peak data from opposite ends of the semiconductor-superconductor heterojunction.

11. The instrument of claim 9 wherein the controller is further configured to validate a zero-bias peak (ZBP) in each of the one or more regions by checking stability of the ZBP to variations in cutter-gate voltage.

12. The instrument of claim 9 wherein the controller is configured to analyze the refinement data by verifying gap closure at the boundary of each of the one or more regions of the parameter space.

13. The instrument of claim 9 wherein the semiconductor-superconductor heterojunction is one of a series of analogously prepared semiconductor-superconductor heterojunctions, wherein the controller is configured to meta-analyze zero-bias peak data across the series to compute a probability of finding a topological region in another analogously prepared semiconductor-superconductor heterojunction.

14. The instrument of claim 9 wherein the instrument is coupled operatively to an RF admittance-measurement device and to a sub-RF conductance-measurement device.

15. A method for building a topological quantum computer, the method comprising :  
fabricating a semiconductor-superconductor heterojunction having at least three terminals configured to support electronic admittance testing ;

measuring a radio-frequency (RF) junction admittance of the semiconductor-superconductor heterojunction to obtain mapping data;

finding by analysis of the mapping data one or more regions of a parameter space consistent with an unbroken topological phase of the semiconductor superconductor heterojunction;

measuring a sub-RF conductance including a non-local conductance of the semiconductor -superconductor heterojunction in each of the one or more regions of the parameter space to obtain refinement data;

finding by analysis of the refinement data a boundary of the unbroken topological phase in the parameter space and a topological gap of the semiconductor-superconductor heterojunction for at least one of the one or more regions of the parameter space; and

incorporating the semiconductor-superconductor heterojunction in a qubit register of the topological quantum computer provided that the found boundary and topological gap are within respective predefined ranges.

16. The method of claim 15 wherein the analysis of the mapping data includes density-based clustering on zero-bias peak data from opposite ends of the semiconductor-superconductor heterojunction.

17. The method of claim 15 further comprising validating a zero-bias peak (ZBP) in each of the one or more regions by checking stability of the ZEP to variations in cutter-gate voltage.

18. The method of claim 15 wherein the analysis of the refinement data includes verifying gap closure at the boundary of each of the one or more regions of the parameter space.

19. The method of claim 15 wherein the semiconductor-superconductor heterojunction is one of a series of analogously prepared semiconductor-superconductor heterojunction, the method further comprising meta-analysis of zero-bias peak data across the series to compute a probability of finding a topological region in another analogously prepared semiconductor-superconductor heterojunction.

20. The method of claim 15 wherein one or more values characterizing the boundary in the parameter space are used as tuning parameters for addressing the semiconductor-superconductor heterojunction in the qubit register.