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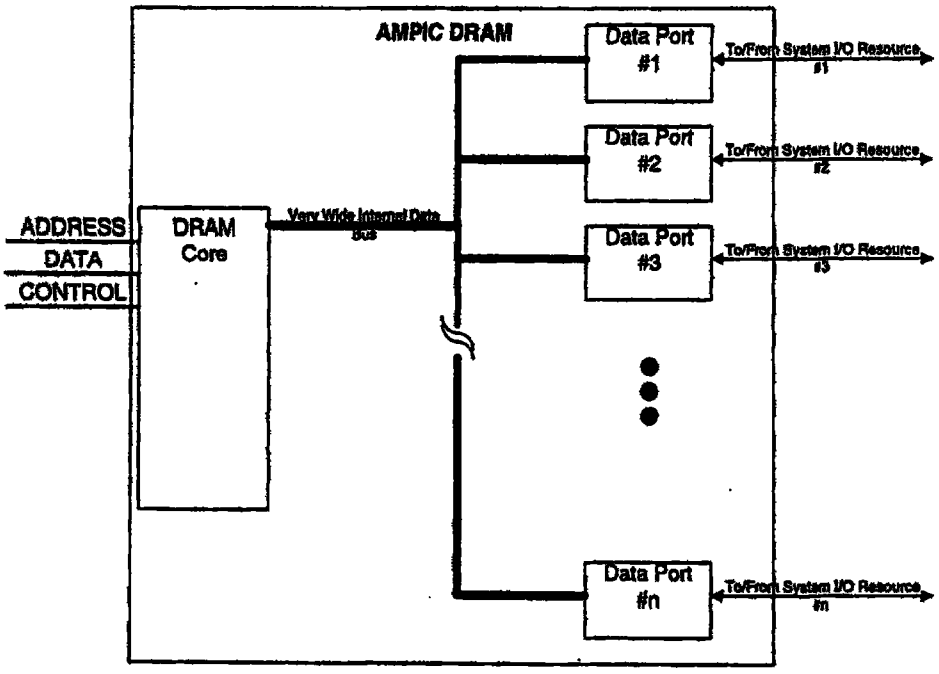
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(54) Title: MULTI-PORT INTERNALLY CACHED DRAMS



(57) Abstract

Apparatus for and method of enhancing the performance of multi-port internal cached DRAMs and the like by providing for communicating to system I/O resources messages sent by other such resources and the message location within the DRAM array, and further providing for efficient internal data bus usage in accommodating for both small and large units of data transfer.