FIG. 1

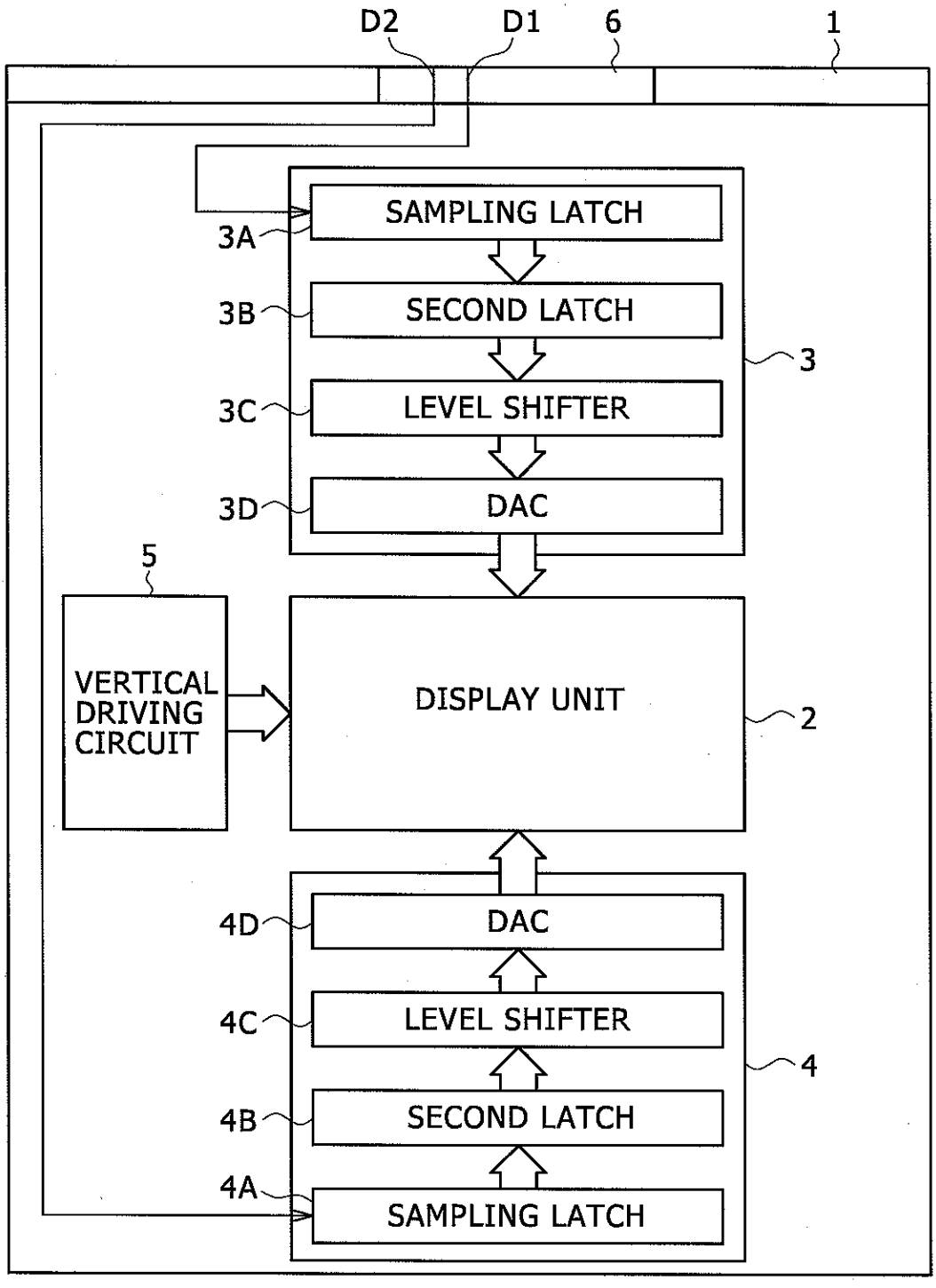

D2
D1
6
1
SAMPLING LATCH
3A
SECOND LATCH
3B
LEVEL SHIFTER
3C
DAC
3D
3
5
VERTICAL DRIVING CIRCUIT
DISPLAY UNIT
2
DAC
4D
LEVEL SHIFTER
4C
SECOND LATCH
4B
SAMPLING LATCH
4A
4

FIG. 2

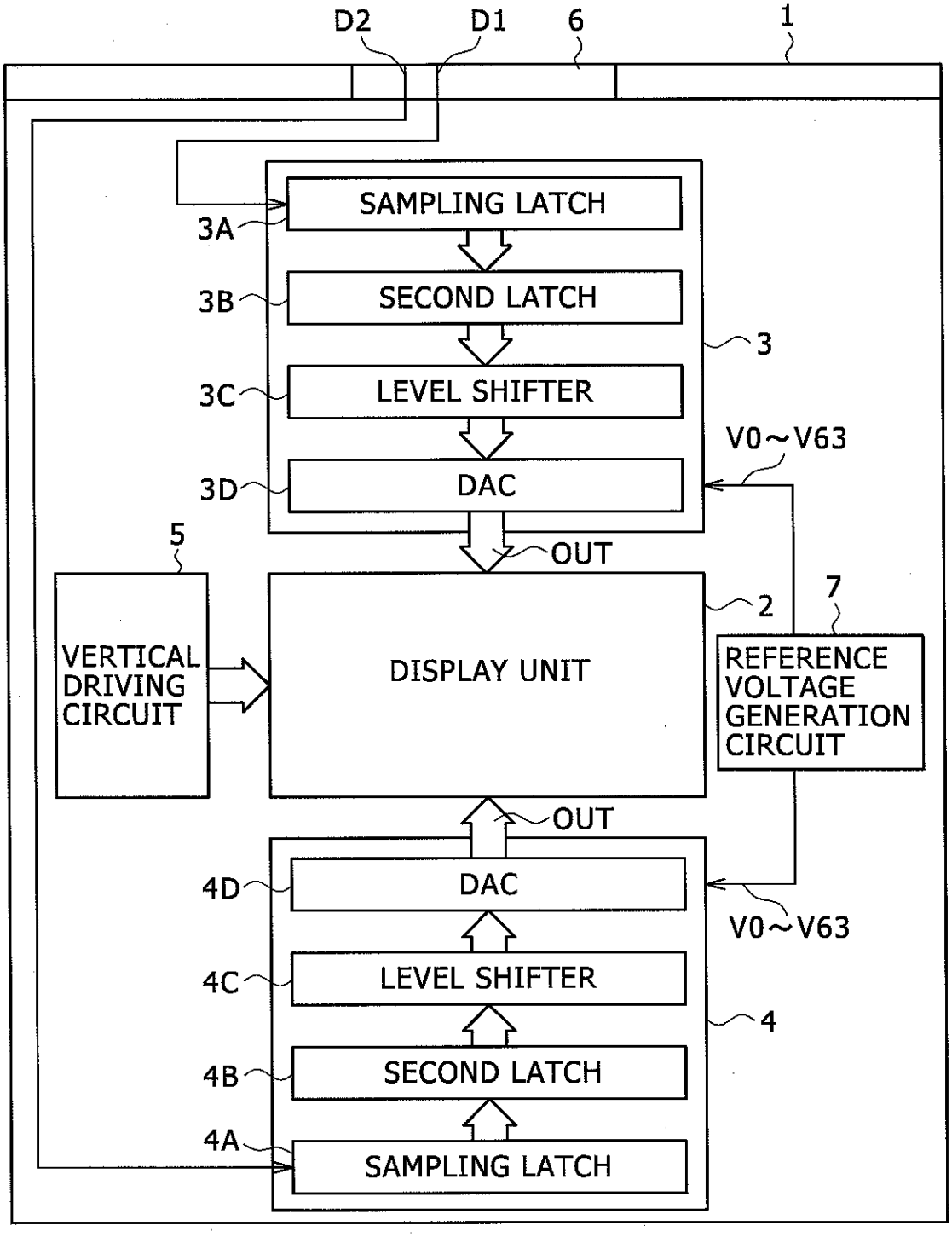

D2
D1
6
1
SAMPLING LATCH
3A
3B
SECOND LATCH
3
3C
LEVEL SHIFTER
V0～V63
3D
DAC
5
OUT
VERTICAL DRIVING CIRCUIT
DISPLAY UNIT
2
7
REFERENCE VOLTAGE GENERATION CIRCUIT
OUT
4D
DAC
V0～V63
4C
LEVEL SHIFTER
4
4B
SECOND LATCH
4A
SAMPLING LATCH

FIG. 3

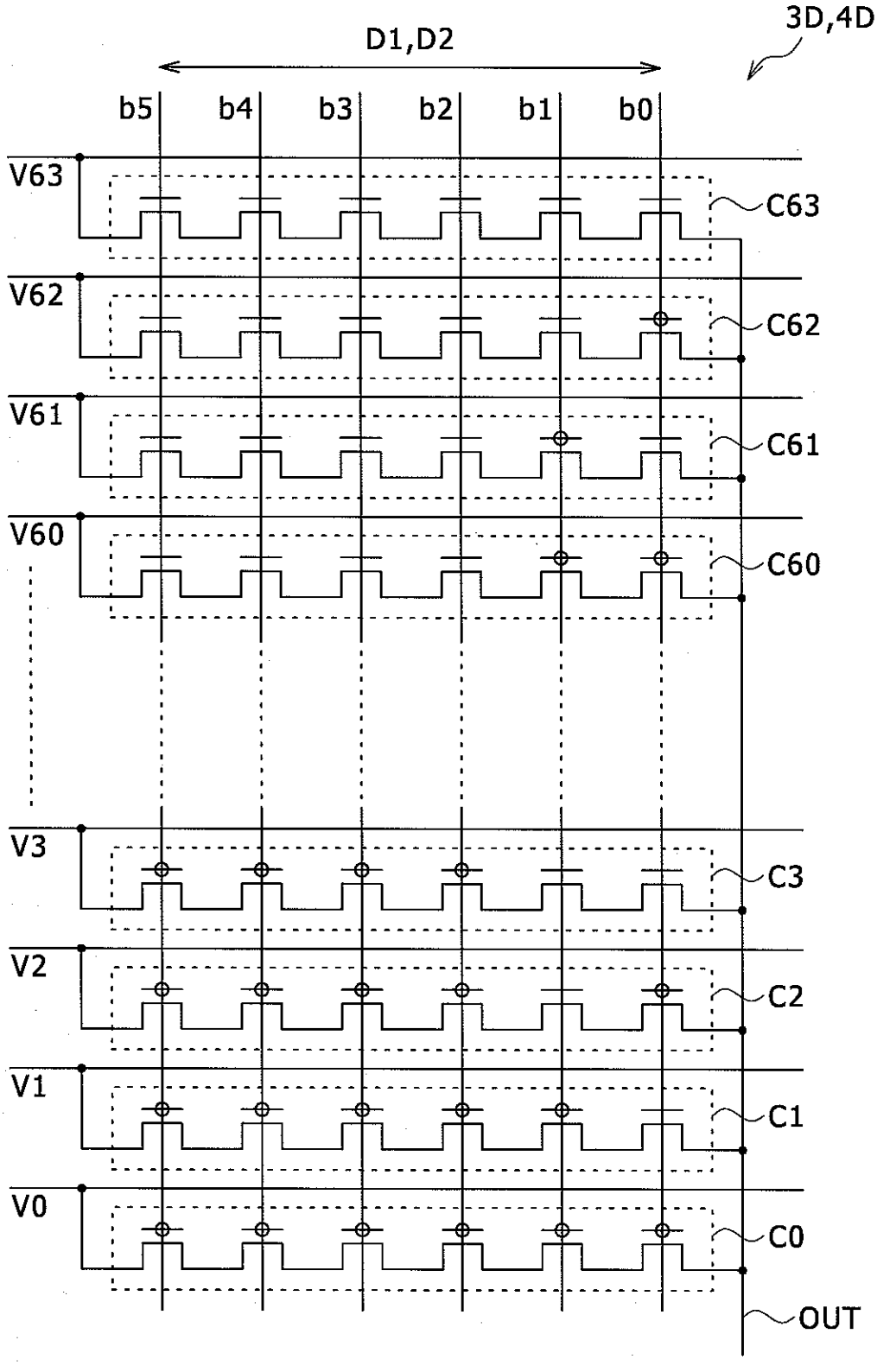

3D,4D
D1,D2
b5
b4
b3
b2
b1
b0
V63
V62
V61
V60
V3
V2
V1
V0
C63
C62
C61
C60
C3
C2
C1
C0
OUT

FIG. 4

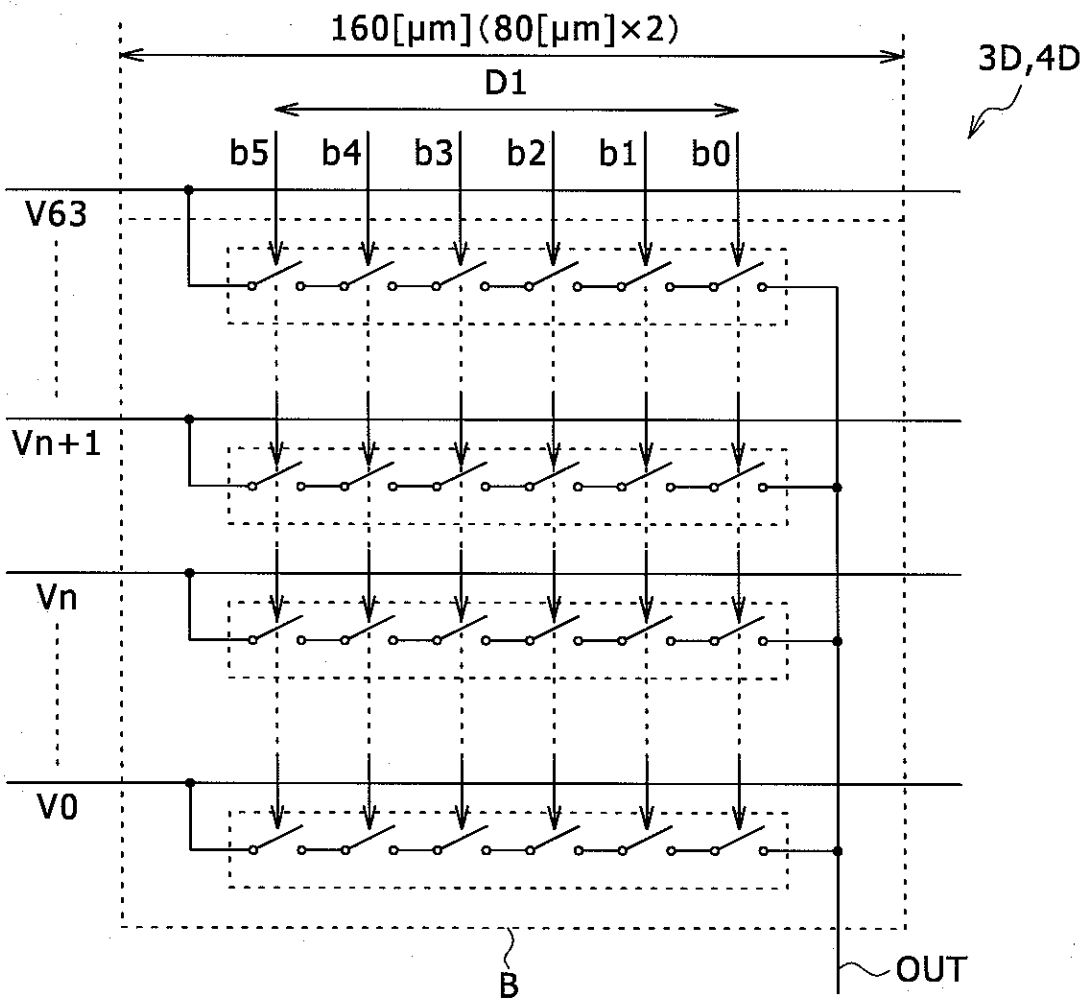


FIG. 5

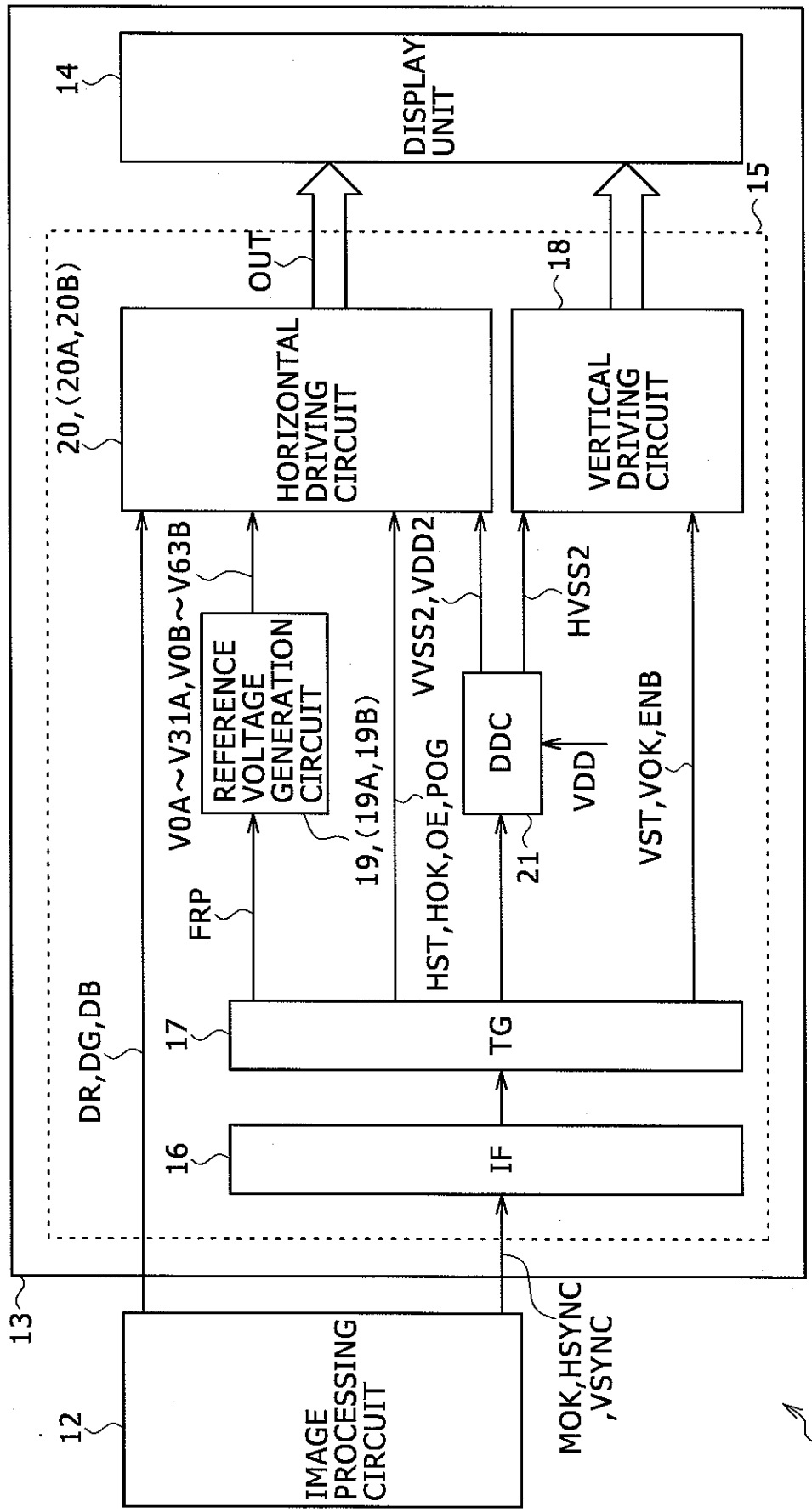

11
13
12
IMAGE PROCESSING CIRCUIT
MOK,HSYNC ,VSYNC
14
DISPLAY UNIT
15
18
OUT
20,(20A,20B)
HORIZONTAL DRIVING CIRCUIT
VERTICAL DRIVING CIRCUIT
V0A~V31A,V0B~V63B
VVSS2,VDD2
HVSS2
REFERENCE VOLTAGE GENERATION CIRCUIT
19,(19A,19B)
HST,HOK,OE,POG
DDC
21
VDD
VST,VOK,ENB
FRP
DR,DG,DB
17
TG
16
IF

FIG. 6

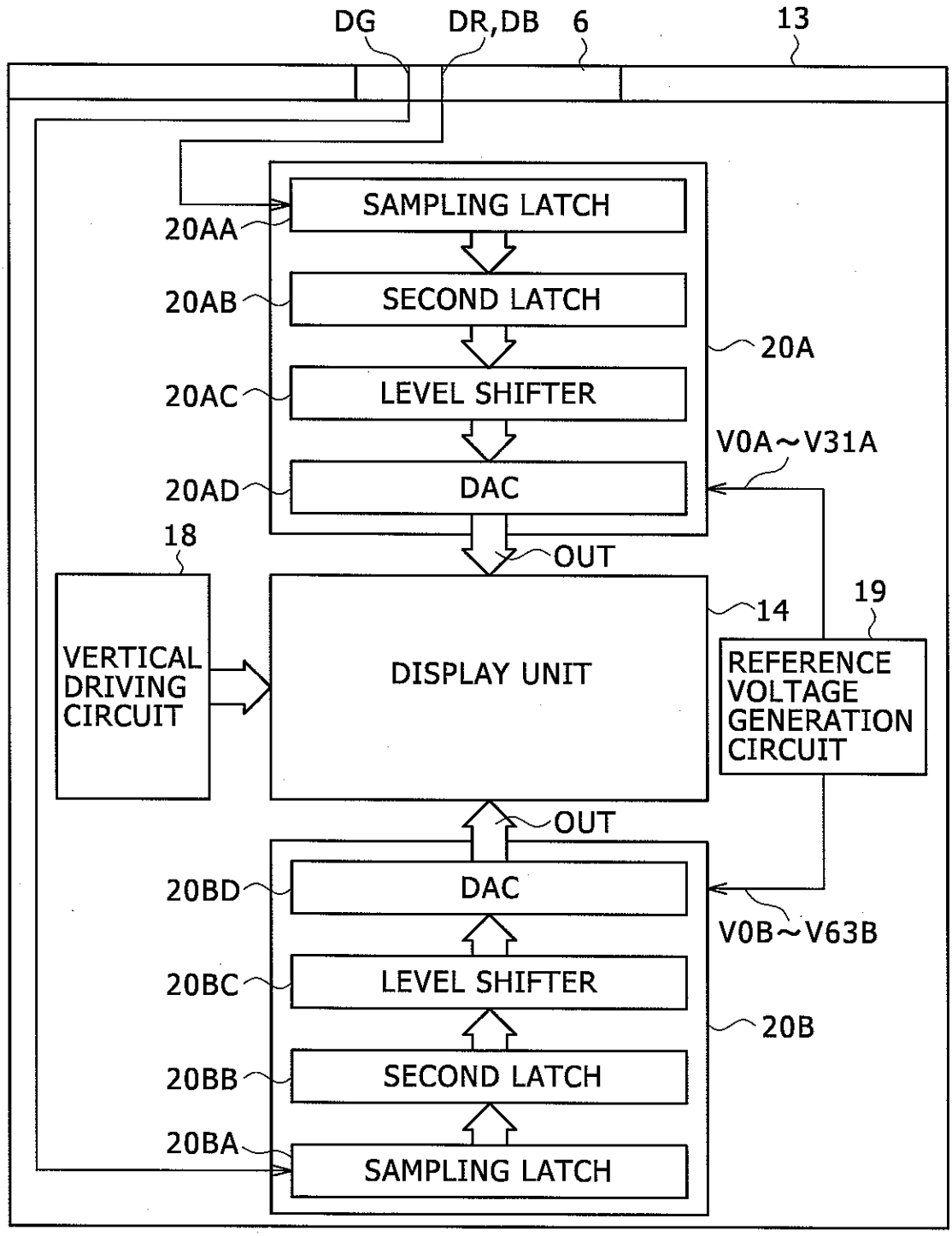

DG
DR,DB
6
13
SAMPLING LATCH
20AA
SECOND LATCH
20AB
LEVEL SHIFTER
20AC
DAC
20AD
20A
V0A～V31A
18
OUT
VERTICAL DRIVING CIRCUIT
DISPLAY UNIT
14
19
REFERENCE VOLTAGE GENERATION CIRCUIT
OUT
DAC
20BD
V0B～V63B
LEVEL SHIFTER
20BC
20B
SECOND LATCH
20BB
SAMPLING LATCH
20BA

FIG. 7

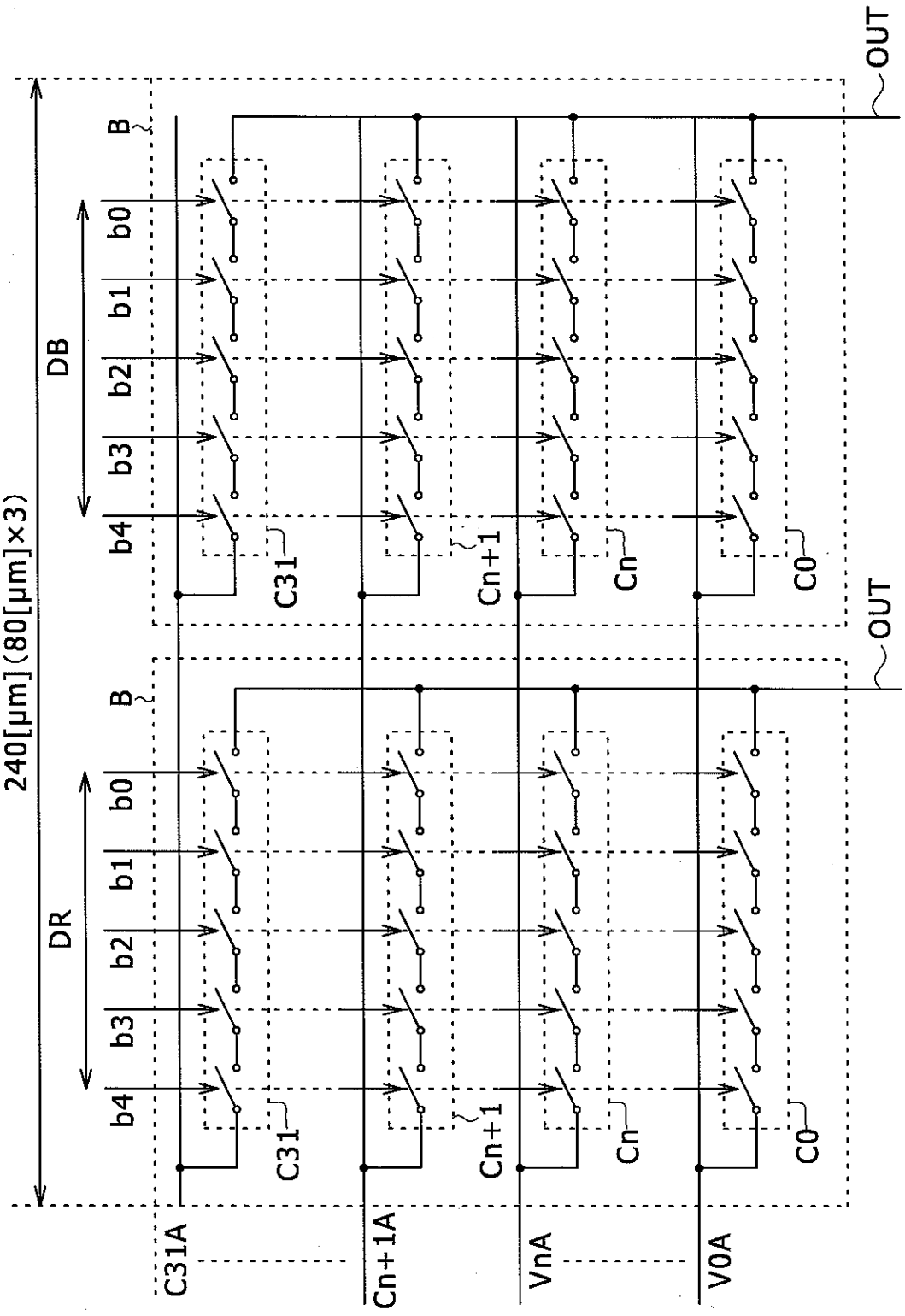

240[μm](80[μm]×3)
DR
DB
B
b0
b1
b2
b3
b4
C31
Cn+1
Cn
C0
OUT
C31A
Cn+1A
VnA
V0A

FIG. 8

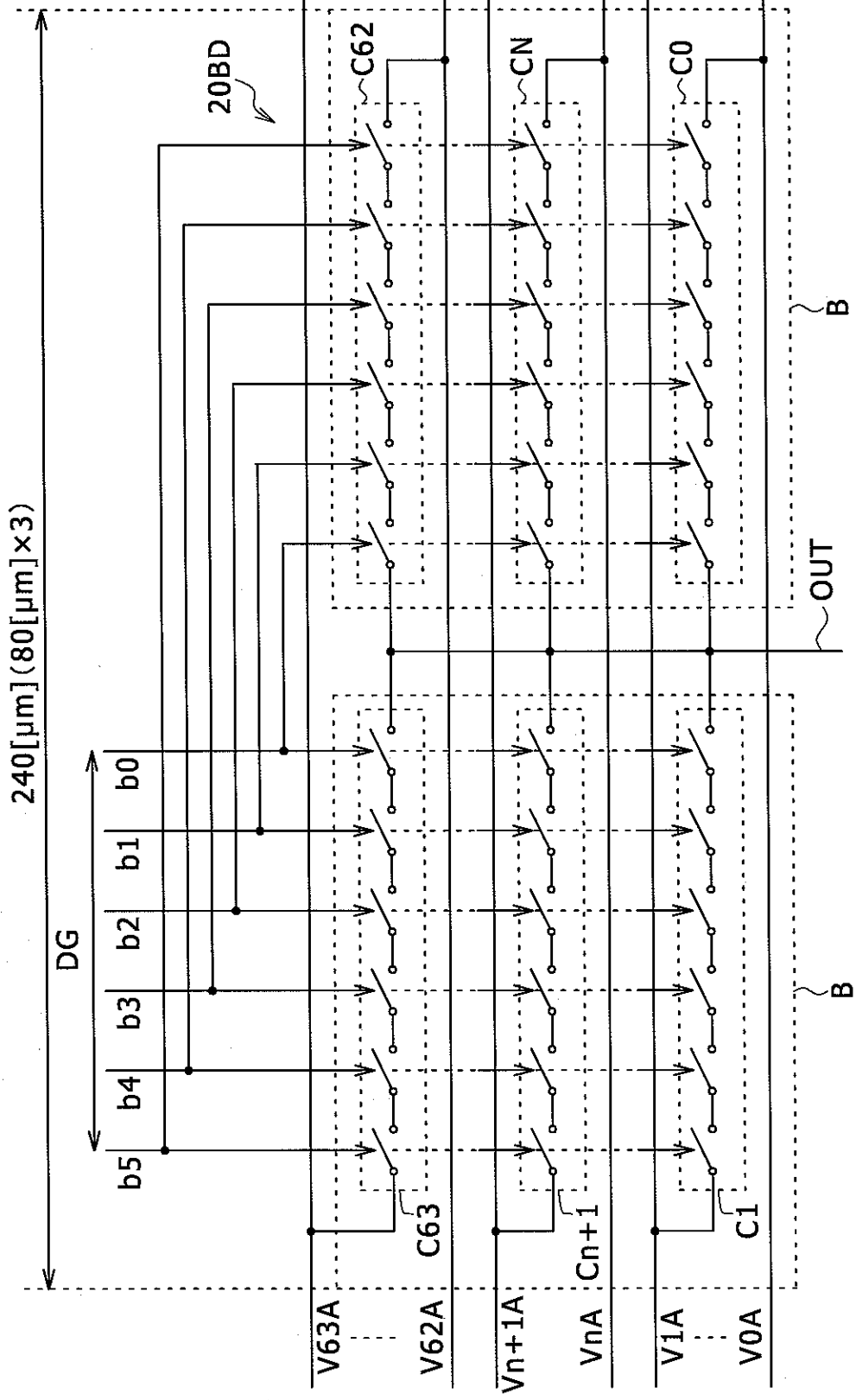
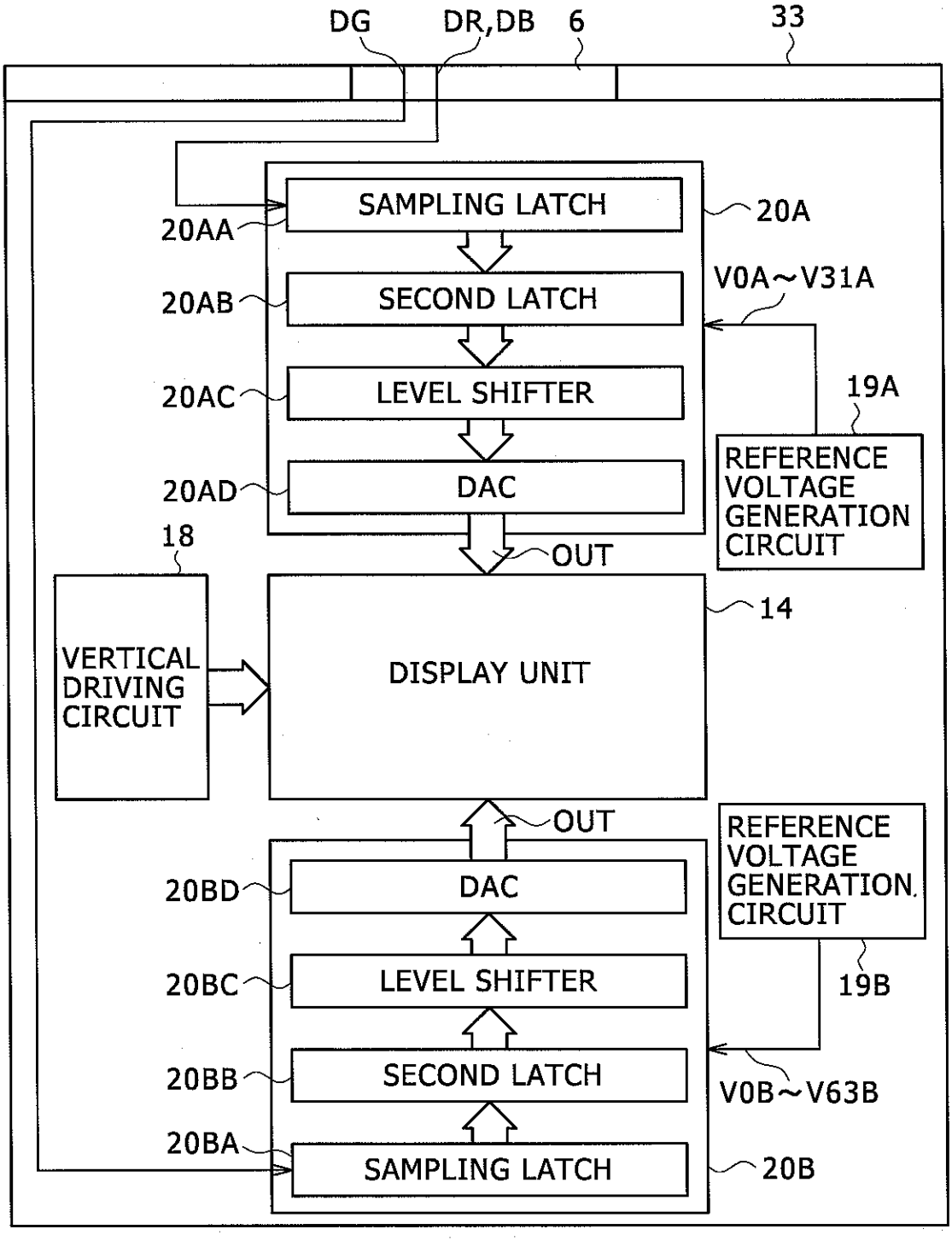

240[μm](80[μm]×3)
DG
b0
b1
b2
b3
b4
b5
20BD
C62
CN
C0
C63
Cn+1
C1
B
B
OUT
V63A
V62A
Vn+1A
VnA
V1A
V0A

FIG. 9


DG
DR,DB
6
33
SAMPLING LATCH
20A
20AA
20AB
SECOND LATCH
V0A～V31A
20AC
LEVEL SHIFTER
19A
20AD
DAC
REFERENCE VOLTAGE GENERATION CIRCUIT
18
OUT
VERTICAL DRIVING CIRCUIT
DISPLAY UNIT
14
OUT
REFERENCE VOLTAGE GENERATION CIRCUIT
20BD
DAC
20BC
LEVEL SHIFTER
19B
20BB
SECOND LATCH
V0B～V63B
20BA
SAMPLING LATCH
20B