WHAT IS CLAIMED IS

1. A semiconductor junction comprising:

a first semiconductor material; and

a second material;

wherein the first semiconductor material and the second ~~semiconductor~~ material being extrinsically undoped,

wherein at least a portion of a valence band of the second material has a higher energy level than at least a portion of the conduction band of the first semiconductor material (type-III band alignment),

wherein a flow of a majority of free carriers across the semiconductor junction is diffusive, ~~and~~

wherein a region of generation and/or recombination of a plurality of free carriers is confined to a two-dimensional surface of the second material, and at the interface of the first semiconductor material and the second material, and

wherein the first semiconductor material is a group III-nitride heterostructure or group III-nitride multiple quantum well structure.

~~2. The semiconductor junction of claim 1, wherein the first semiconductor material is a group III-nitride heterostructure or group III-nitride multiple quantum well structure.~~

~~3.~~ 2. The semiconductor junction of claim 1 ~~2~~, wherein the first semiconductor material is indium-rich $In_{1-x}Ga_xN$ ($0 \leq x \leq 0.2$), and the second material is a two-dimensional interlayer within the first semiconductor material formed by $In_{1-x}Ga_xP$ ($0 \leq x \leq 0.6$)~~.~~.

~~4.~~ 3. The semiconductor junction of claim 1, wherein the first semiconductor material is between 1-500 nm thick, and the second material is no more than 100 monolayers thick.

~~5.~~ 4. The semiconductor junction of claim 1, wherein the first semiconductor material is a ternary or quaternary group III-nitride.

~~6.~~ 5. The semiconductor junction of claim 1, wherein the second material is a two-dimensional (2D) interlayer of graphite or metal-/transition-metal oxides / dichalcogenides.

~~7.~~ 6. The semiconductor junction of claim 1, wherein the first semiconductor material has an aperiodic superlattice structure.

~~8.~~ 7. The semiconductor junction of claim 1, wherein the second material is a two-dimensional interlayer disposed between the first semiconductor material and a third material~~, the third material also forming a two-dimensional interlayer between the second material and a fourth material~~.

~~9.~~ 8. The semiconductor junction of claim 1, wherein the confinement of free carriers at the semiconductor junction is carriers being confined in a semiconductor junction formed from a type-III band alignment.

~~10.~~ 9. The semiconductor junction of claim 1, wherein the confinement of free carriers leads to surface plasmon (SP) generation and propagation conditions in the IR and VIS spectral range.

~~11.~~ 10. A method comprising :

providing a semiconductor junction comprising:

a first semiconductor material; and

a second material,

wherein at least a portion of a valence band of the second material has a higher energy level than at least a portion of the conduction band of the first semiconductor material;

applying a bias to lower the valence band of the second material with respect to the conduction band of the first semiconductor material resulting in a lower transverse current; and

increasing the bias to further reduce electrons in the conduction band, thereby reducing the transverse current to a direction of the bias such that when all of the initial carriers diffused into the lower conduction band is offset by the bias, the transverse current disappears,

wherein the first semiconductor material is a group III-nitride heterostructure or group III-nitride multiple quantum well structure.