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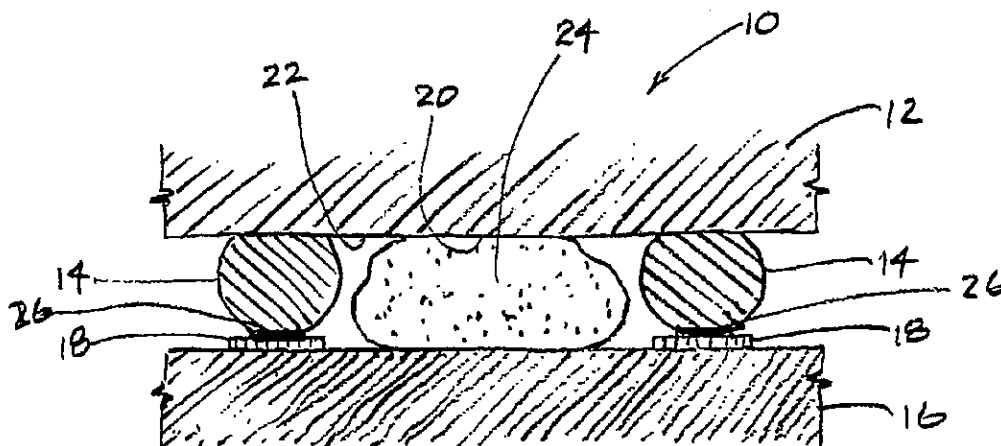
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(54) Title: PACKAGING STRUCTURE AND METHOD



(57) Abstract: A method for forming metallurgical interconnections and polymer adhesion of a flip chip (12) to a substrate (16) includes providing a chip (12) having a set of bumps (14) formed on a bumpy side (22) thereof and a substrate (16) having a set of interconnect points (18) on a metallization thereon, providing a measured quantity of polymer adhesive (24) in a middle region of the chip (12) on the bump side (22), aligning the chip (12) with the substrate (16) so that the set of bumps (14) aligns with the set of interconnect points (18), pressing the chip (12) and the substrate (16) toward one another so that a portion of the polymer adhesive (24) contacts the substrate (16) and the bumps (14) contact the interconnect points (18), and heating the bumps (14) to a temperature sufficiently high to form a metallurgical connection between the bumps (14) and the interconnect (18). Also, a flip chip (12) package is made by the method. In some embodiments the metallurgical connection includes an alloy of gold and tin at the interface between the bumps (14) and the interconnect points (18).

PACKAGING STRUCTURE AND METHOD

BACKGROUND OF THE INVENTION

This invention relates to flip chip packaging and, more particularly, to providing a
5 Au/Sn alloy interconnection between a chip and a substrate.

Conventional methods for interconnecting a flip chip to a substrate include an
Anisotropic Conductive Film (ACF) with Ni or Ni/Au coated polymer particles in which a
contact type interconnection is made. Fragments of the polymer film which remain
10 trapped at the interconnection point often lead to poor electrical contact and reduced
reliability of the package. Additionally, the polymer film reduces the reliability of the
bonding interface during the chip bonding process. Conventional flip chip techniques
that use either ACF, Non-Conductive Adhesive (NCA) or Non Conductive Polymer
(NCP) also suffer from problems in curing the adhesive on adjacent bonding sites on a
15 substrate during the chip bonding process.

What is needed is a flip chip structure and method that provides for metallurgical
interconnection between the flip chip and the substrate and that further provides for
improved bonding between the chip and the substrate.
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BRIEF SUMMARY OF THE INVENTION

In a first aspect, the present invention provides a method for connecting a flip chip and
a substrate, the method comprising: providing a chip having a set of bumps formed on
25 a bump side thereof, providing a substrate having a set of interconnect points on a
metallization thereon, providing a measured quantity of a polymer adhesive in a middle
region of the chip on the bump side, aligning the chip with the substrate so that the set
of bumps aligns with the set of interconnect points, pressing the chip and the substrate
toward one another so that a portion of the polymer adhesive contacts the substrate
30 and the bumps contact the interconnect points, and heating the bumps to a
temperature sufficiently high to form a metallurgical connection at an interface between
the bumps and the interconnect points.

In some embodiments the bumps are stud bumps, and are formed of gold; and the
35 interconnect points include spots of tin, preferably pure tin, on the metallization. In

other embodiments the bumps are formed of a metal such as, for example, copper plated with Au or with Ni/Au or electroless Ni/Au; and the interconnect points also may include such materials. In embodiments in which the stud bumps are made of Au and the interconnect points are spots of Sn, the heating step raises the temperature of the bumps sufficiently to create an alloy between the Au and the Sn in a bonding phase at the interface; in preferred embodiments the bonding phase comprises a 80:20 Au:Sn alloy. For such an alloy the bumps may be sufficiently heated by heating the die to a temperature greater than about 200°C, preferably about 232°C.

10 In some embodiments the method further includes underfilling with a polymer.

In a second aspect, the present invention provides a chip package structure made according to the first aspect. The chip package structure comprises a chip having bumps formed thereon and a substrate having interconnect points on a metallization thereon, the bumps forming contacts with the interconnect points, wherein each said contact comprises an interconnection layer situated at an interface between the bump and the interconnection point in contact therewith, the layer comprising an alloy of the material of the bump and the material of the interconnect point.

20 In a third aspect, the present invention provides a chip package structure comprising: a chip having bumps formed thereon and a substrate having interconnect points on a metallization thereon, the bumps forming contacts with the interconnect points, wherein each said contact comprises an alloy of the material of the bump and the material of the interconnect point, the alloy being limited to a layer situated at an interface between the bump and the interconnect point; and a first cured adhesive polymer forming a spot situated in a middle region between the bump surface of the chip and the surface of the substrate, there being no first cured adhesive polymer at the contacts.

30 In some embodiments a cured adhesive polymer is situated in a middle region between the bump surface of the chip and the surface of the substrate.

In some embodiments the bump material is gold or is a metal such as copper plated with gold or with Ni/Au or with electroless Ni/Au; and the interconnect points also

include such materials. In some embodiments the alloy at the interface is an alloy of Au and Sn, and preferably the alloy is a 20:80 Sn:Au alloy.

5 BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B are diagrammatic sketches in a sectional view showing an illustrative embodiment of stages according to the invention for making a packaging structure according to the invention.

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DETAILED DESCRIPTION OF THE INVENTION

A description of an exemplary embodiment of the invention follows. Using the disclosure herein, substantially conventional apparatus can be modified for use in the process of the invention.

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With reference to the Figs., there are shown in Fig. 1A a chip and a substrate in alignment prior to forming the interconnect according to the invention, and in Fig. 1B a completed interconnect. The flip chip configuration, shown generally at 10, includes a plurality of bumps, e.g. 14, formed on the chip 12, the bumps preferably being gold (Au) stud bumps. The corresponding
5 interconnection points, on a standard substrate 16 metallization are provided with a plurality of preferably pure tin (Sn) spots 18. A central area 20 of the chip on a bump side 22 further includes a spot of adhesive 24 small enough that it does not spread to the gold studs and the interconnection area during a subsequent bonding process. As the chip is connected to the substrate in the flip chip format, the adhesive holds the chip to the substrate and the ends of the
10 stud bumps 14 react with the pure tin spots 18 on the substrate to make metallurgical interconnections 26.

A substrate strip populated with a row or an array of chips assembled in this manner can be molded using simple tooling, readily adapted from conventional equipment. The molding preferably provides die underfilling and molding compound along the perimeters of the die
15 simultaneously. Solder balls can then be attached and the completed chips can be singularized by, for example, sawing the substrate.

The flip chip is aligned with the substrate in such a manner that the gold stud bumps on the chip align with the tin spots on the substrate. After alignment and contact between the Sn spots and the Au stud bumps, the die is heated to a temperature and for a time sufficient to give a
20 metallurgical reaction at the interface between the bumps and the spots, preferably in excess of about 200 °C. For an Au - Sn junction, a suitable temperature the temperature is about 232 °C, and a suitable time is 1 - 2 seconds. At this temperature, the Sn spots melt and the temperature at the bonding interface increases significantly, thereby dissolving some Au from both a metallization layer on the substrate and the stud bumps to create a bonding phase at the interface
25 between the Sn spots and the Au stud bumps. Preferably a 80 %:20 % Au:Sn alloy composition is formed at the interface. Such an alloy provides both reliable electrical contact and advantageous mechanical properties.

As the Sn/Au interconnection is made the adhesive spot cures to hold the die in space. A subsequent underfilling process of the structure is thereby facilitated as the center region of the
30 chip is already filled with the adhesive polymer. Overmolding fills the remaining space under the die and the space between the chips, resulting in a robust structure.

An alternative embodiment provides for direct contact between the gold stud bumps and a standard metallization on the substrate. A metallization bond able to withstand the stresses of subsequent processing is thereby formed as there is no interposing polymer at the bonding interface during the chip bonding process.

5 To achieve wafer scale packaging, a wafer having stud bumps thereon is placed face up on a heating stage. Substrate pieces, inspected and singulated, with appropriate amounts of adhesive are then picked, aligned, placed and bonded to wafer sites applying conventional process conditions of temperature and pressure. Ultrasonic scrubbing may be employed to clean the substrate site before thermal compression bonding. The disclosed process provides for little waste of substrate material as only particular rejected sites will be discarded, rather than the entire substrate strip. Additionally, it is not necessary to bond to the rejected dies on the wafer. After fully populating the wafer, the wafer is molded for underfilling and interchip space filling. Dicing the wafer then follows the molding and solder ball mounting steps to singulate the dies.

10 In alternative embodiments the stud bumps include Cu plated with Ni and Au, plated Au or electroless Ni/Au, and these materials may be also provided on the bonding sites of the substrate. With the advances in Cu terminal metallurgy, the bonding sites may be finished with Ni and heavy soft Au, thereby providing for interconnections between the wafer and substrate I/Os either by thermal compression bonding utilizing Au or by fusion at low temperatures utilizing Sn like metals to form suitable bonding phases. Once metallurgical contacts are formed, the structure is underfilled and transfer molded simultaneously.

20 Other embodiments are within the following claims.

CLAIMS

1. A method for providing connection between a flip chip and a substrate, comprising:
 - 5 providing a chip having a set of bumps formed on a bump side thereof;
 - providing a substrate having a set of interconnect points on a metallization thereon;
 - providing a measured quantity of a polymer adhesive in a middle region of the chip on the bump side;
 - 10 aligning the chip with the substrate so that the set of bumps aligns with the set of interconnect points;
 - pressing the chip and the substrate toward one another so that a portion of the polymer adhesive contacts the substrate and the bumps contact the interconnect points; and
 - 15 heating the bumps to a temperature sufficiently high to form a metallurgical connection at an interface between the bumps and the interconnect points.
2. The method of claim 1, wherein the bumps are stud bumps.
- 20 3. The method of claim 1, wherein the bumps comprise gold.
4. The method of claim 1, wherein the bumps are plated with a metal comprising gold.
5. The method of claim 1, wherein the interconnect points comprise tin.
- 25 6. The method of claim 5, wherein the interconnect points comprise pure tin.
7. The method of claim 1, wherein the interconnect points comprise a metal plated with a metal comprising gold.
- 30 8. The method of claim 1, wherein the bumps are stud bumps comprising Au and the interconnect points comprise Sn, and the heating step raises the temperature of the bumps sufficiently to create an alloy between the Au and the Sn in a bonding phase at the interface.

9. The method of claim 8, wherein the heating step raises the temperature of the bumps sufficiently to create an alloy comprising a 80:20 Au:Sn in a bonding phase at the interface.

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10. The method of claim 1, wherein the heating step raises the die to a temperature greater than about 200°C.

10 11. The method of claim 1, wherein the heating step raises the die to a temperature about 232°C.

12. The method of claim 1, further comprising underfilling with a polymer.

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13. A chip package structure made according to the method of claim 12.

14. A chip package structure comprising:

20 a chip having bumps formed thereon and a substrate having interconnect points on a metallization thereon, the bumps forming contacts with the interconnect points, wherein each said contact comprises an interconnection layer situated at an interface between the bump and the interconnection point in contact therewith, the layer comprising an alloy of the material of the bump and the material of the interconnect point.

25 15. The chip package structure of claim 14, wherein a cured adhesive polymer is situated in a middle region between the bump surface of the chip and the surface of the substrate.

30 16. The chip package structure of claim 14, wherein the bump material comprises gold and the interconnect points comprise Sn, and the alloy at the interface comprises a Au/Sn alloy.

17. The chip package structure of claim 16, wherein the alloy at the interface is a 20:80 Sn:Au alloy.

35 18. A chip package structure comprising:

a chip having bumps formed thereon and a substrate having interconnect points on a metallization thereon, the bumps forming contacts with the interconnect points, wherein each said contact comprises an alloy of the material of the bump and the material of the interconnect point, the alloy being limited to a layer situated at an interface between the bump and the interconnect point; and

a first cured adhesive polymer forming a spot situated in a middle region between the bump surface of the chip and the surface of the substrate, there being no first cured adhesive polymer at the contacts.

10 19. The chip package structure of claim 18, wherein the bump material comprises gold and the interconnect points comprise Sn, and the alloy at the interface comprises a Au/Sn alloy.

15 20. The chip package structure of claim 18, further comprising a second cured adhesive polymer forming an underfill.