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SPECIFICATION

TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and, more particularly, to a technique which is effective when applied to the mounting of a plurality of semiconductor devices on the mounting face of a mounting board.

As a semiconductor device suitable for the reduced size or thickness of an electronic device, there is a semiconductor device having the TSOP (Thin Small Out-line Package) structure. In this semiconductor device of the TSOP structure, for example, a semiconductor chip, constituted of a DRAM (Dynamic Random Access Memory), is encapsulated in a package made of resin.

This package is so formed as to have a rectangular plane shape. At and along one side face of the package, there are arranged a plurality of outer leads. These outer leads are individually so formed as to have a gull-wing shape and are individually connected electrically to a plurality of external terminals (bonding pads) arrayed on one side

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of a major surface of the semiconductor chip. On the other side face opposed to the one side face of the package, moreover, there are arrayed a plurality of outer leads. These outer leads are individually so formed as to have a gull-wing shape and are individually connected electrically with a plurality of external terminals which are arrayed on the other side of the principal face of the semiconductor chip. In short, the semiconductor device of TSOP structure is constructed of a two-way lead array structure in which a plurality of outer leads electrically connected to the semiconductor chip are individually arrayed on the two side faces of the package, opposed to each other.

Semiconductor devices of the TSOP structure thus constructed are regularly mounted over the mounting board of a memory card which is additionally connected to an electronic device such as a personal computer or office computer. This mounting is usually performed by printing the electrode pads (the land regions of the wiring), arranged over the mounting face of the mounting board, with pasty solder by a screen printing method, and by fixing the electrode pads of the mounting board and the outer leads of the semiconductor devices with solder.

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Incidentally, a semiconductor device of the TSOP structure is disclosed in Nikkei Maikurodevaisu [pp. 34 to 45, the June issue, 1990] issued by NIKKEI BP.

SUMMARY OF THE INVENTION

The aforementioned semiconductor device of the TSOP structure has the following problems because a plurality of outer leads electrically connected to the external terminals of a semiconductor chip are individually arrayed on the two side faces, opposed to each other, of the package.

(1) When semiconductor devices of the TSOP structure are mounted over the mounting face of the mounting board in the direction perpendicular to one side face of the package, the outer leads, electrically connected to the external terminals of the semiconductor chip, are opposed to each other between the adjoining semiconductor devices. In a memory card, therefore, considering the displacement of the semiconductor devices and the extrusion of the solder at the mounting time, a spacing region is provided between the outer leads of one semiconductor device and the outer leads of the other semiconductor device to prevent the short-circuiting between the adjoining semiconductor devices. However, the spacing region

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has to be formed for every space between semiconductor devices so that the mounting density of the semiconductor devices over the mounting board drops by a value corresponding to the areas of the spacing regions.

(2) When a plurality of semiconductor devices of the TSOP structure are mounted in a direction perpendicular to one side face of the package, between the adjoining semiconductor devices, the outer leads arrayed on one side face of the package of one semiconductor device are present between the outer leads arrayed on the other side face of the package of the one semiconductor device, and the outer leads arranged on the one side face of the package of the other semiconductor device. In short, between the outer leads having the same functions, there are present the outer leads which have different functions. In the memory card, therefore, the wiring existing over the mounting board are routed in a roundabout way to electrically connect the outer leads of the same functions of the individual semiconductor devices. However, such wiring increases the area occupied by the wiring so that the mounting density of the semiconductor devices over the mounting board drops by a value corresponding to the increase in the

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area.

An object of the present invention is to provide a semiconductor device which can be mounting at a high density.

The aforementioned and other objects and novel features of the present invention will become apparent from the following description to be made with reference to the accompanying drawings.

The summary of a representative of the aspects of the invention to be disclosed will be briefly described in the following.

Semiconductor devices mounted on the mounting face of a mounting board have a structure in which each semiconductor chip is encapsulated in a package having a rectangular plane shape, in which a plurality of outer leads electrically connected to external terminals of the semiconductor chip are arrayed on the one side face of the package, and in which a plurality of outer leads not electrically connected to the external terminals of the semiconductor chip are arrayed on the other side face opposed to the one side face of the package.

According to the above-specified means, when these semiconductor devices are mounted on the mounting face of the mounting board and arranged in a

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direction perpendicular to one side face of the package, between the semiconductor devices adjoining in that direction, the outer leads arrayed on one side face of the package of one semiconductor device, and the outer leads arrayed on the other side face of the package of the other semiconductor device are opposed to each other. However, the outer leads of the one semiconductor device are electrically connected to the external terminals of the semiconductor chip, but the outer leads of the other semiconductor device are not electrically connected to the external terminals of the semiconductor chip, so that the outer leads electrically connected to the external terminals of the semiconductor chip are not opposed to each other. As a result, even if the spacing region between the outer leads of the one semiconductor device and the outer leads of the other semiconductor device is reduced or eliminated and if the semiconductor devices are displaced or have extrusion of solder at the packaging time, no short-circuiting takes place between the adjoining ones of the semiconductor devices which are mounted in the direction perpendicular to one side face of the package. As a result, the spacing region between the outer leads of one semiconductor device and the outer leads of the

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other semiconductor device can be reduced or eliminated to mount the semiconductor devices over the mounting board at an accordingly high density.

When semiconductor devices are mounted on the mounting face of the mounting board in a direction perpendicular to one side face of the package, between the adjoining semiconductor devices, there are arranged between the outer leads arrayed on one side face of the package of one semiconductor device, and the outer leads arrayed on one side face of the package of the other semiconductor device, the outer leads which are arrayed on the other side face of the package of the one semiconductor device. However, these outer leads arrayed on the other side face of the package of the one semiconductor device are not electrically connected to the external terminals of the semiconductor chip so that, there are no outer leads between the outer leads of the one semiconductor device and the outer leads of the other semiconductor device having different functions. Without routing the wiring extending over the mounting board in a roundabout way, therefore, it is possible to electrically connect the outer leads of the same functions of the individual semiconductor devices which are mounted in a direction perpendicular to one

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side face of the package. As a result, the wiring region can be reduced or eliminated to mounting the semiconductor devices in an accordingly high density.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a top plan view showing the state that the upper portion of the package of a semiconductor device of Embodiment 1 of the present invention is removed;

Fig. 2 is a section taken along line A-A shown in Fig. 1;

Fig. 3 is a top plan view showing a memory card in which the semiconductor devices are mounted on the mounting face of a mounting board;

Fig. 4 is an enlarged top plan view showing an essential portion of the memory card;

Fig. 5 is a top plan view showing the state that the upper portion of the package of a semiconductor device of Embodiment 2 of the present invention is removed;

Fig. 6 is a top plan view showing a memory card in which the semiconductor devices are mounted on the mounting face of a mounting board;

Fig. 7 is an enlarged top plan view showing an essential portion of the memory card;

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Fig. 8 is a top plan view showing the state that the upper portion of a package of a semiconductor device of Embodiment 3 of the present invention is removed;

Fig. 9 is a top plan view showing the state that upper portion of a package of a semiconductor device of Embodiment 4 of the present invention is removed;

Fig. 10(A) is a section taken along line A-A of Fig. 4;

Fig. 10(B) is a section taken along line B-B of Fig. 4;

Fig. 11 is a perspective view showing an electronic device to which is applied the memory card MC of the present invention;

Fig. 12 is a top plan view showing the memory card MC;

Figs. 13 and 14 are sections taken along lines A-A and B-B of Fig. 12;

Fig. 15 is an external view of a semiconductor device of Embodiment 5 of the present invention;

Fig. 16 is an explanatory view for explaining the names and functions of lead pins of Fig. 15;

Fig. 17 is a top plan block diagram showing a flash memory chip mounted in the semiconductor device of Fig. 15;

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Fig. 18 is a top plan view showing the front side of the memory card of the present invention;

Fig. 19 is a top plan view showing the back side of the memory card of the present invention;

Fig. 20 is a section taken along lines A-A of Figs. 18 and 19; and

Fig. 21 is a block diagram showing the system configuration of a memory card (ATA card) of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The embodiments of the present invention will be described in detail with reference to the accompanying drawings.

Incidentally, throughout all the drawings for illustrating the embodiments of the present invention, the parts and portions having the same functions will be designated by common reference numerals while omitting their repeated description.

(Embodiment 1)

Fig. 1 is a top plan view showing the state that the upper portion of the package of a semiconductor device of Embodiment 1 of the present invention is removed, and Fig. 2 is a section taken along line A-A shown in Fig. 1.

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As shown in Figs. 1 and 2, a semiconductor device 10 of the present embodiment has a TSOP (Thin Small Out-line Package) structure. This semiconductor device 10 has a semiconductor chip 1 mounted on one surface of a tab 4 which is supported by four tab-suspension leads 5. The semiconductor chip 1 is fixed, although not shown, to one surface of the tab 4 through an adhesive layer of Ag paste or the like.

The aforementioned semiconductor chip 1 is constructed mainly of a semiconductor substrate which is a single-crystal silicon substrate having a rectangular plane shape. In the major surface (element forming surface) of the semiconductor substrate, there is constructed a DRAM (Dynamic Random Access Memory) as a memory circuit system, for example. Over the major surface of the semiconductor substrate, moreover, there is formed a multilayer wiring layer in which plural stages of wiring layers and insulating layers are individually stacked.

On one side (one long side) of the major surface of the aforementioned semiconductor chip 1, there are arrayed a plurality of external terminals (bonding pads) BP along the one side. These external terminals BP are individually formed in the uppermost wiring layer of the multilayer wiring and are electrically

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connected to the memory circuit system.

Outside the one side of the semiconductor chip 1, there are arrayed a plurality of inner leads 2A along the one side. These inner leads 2A are individually connected electrically through bonding wires 6 to the external terminals BP which are arrayed on the one side of the major surface of the semiconductor chip 1.

Outside the other side (the other long side) opposed to the one side of the semiconductor chip 1, there are arrayed a plurality of inner leads 2B along the other side. These inner leads 2B are not individually connected electrically to the external terminals BP of the semiconductor chip 1.

The aforementioned semiconductor chip 1, inner leads 2A, inner leads 2B, tabs 4, tab suspension leads 5 and bonding wires 6 are encapsulated in a package 7 so formed as to have a rectangular plane shape. This package 7 is formed by a transfer molding method, for example, although not limited thereto. The transfer molding method is a technique for forming a package with an epoxy resin to which are added a phenol curing agent, silicone rubber and a filler.

On one side face 7A of the aforementioned package 7, there are arranged a plurality of outer leads 3A along the side face. On the other side face 7B

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opposed to the one side face 7A of the package 7, there are also arrayed a plurality of outer leads 3B along the side face. These outer leads 3A and 3B are individually formed into a gull-wing shape.

The aforementioned outer leads 3A are individually integrated with the inner leads 2A which are arrayed outside the one side of the semiconductor chip 1. Moreover, the aforementioned outer leads 3B are individually integrated with the inner leads 2B which are arrayed outside the other side of the semiconductor chip 1. In short, the semiconductor device 10 of the present embodiment is constructed of the bidirectional lead array structure in which the outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on and along the one side face 7A of the package 7 whereas the outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arranged at and along the other side face 7B opposed to the one side face of the package 7.

The aforementioned outer leads 3A, outer leads 3B and tab suspension leads 5 are individually integrated with the lead frame at a step of manufacturing the semiconductor device. These outer leads 3A and 3B and tab suspension leads 5 are individually cut from the

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lead frame after the inner leads 2A and 2B, the tabs 4, the tab suspension leads 5 and the bonding wires 6 are encapsulated in the package 7. After this, the outer leads 3A and 3B are individually formed into the gull-wing shape. Incidentally, the lead frame is made of a Cu alloy or an Fe-Ni (having 42 or 50 [%] of Ni content, for example) alloy, for example.

To the aforementioned outer leads 3A and outer leads 3B, there are applied an address signal, a row-address strobe signal, a column-address strobe signal, an output enable signal, a write enable signal and a data input/output signal.

A plurality of semiconductor devices 10 thus constructed are regularly arranged as one memory system, as shown in Fig. 11, on a mounting board of a memory card (an electronic unit) MC which is additionally connected to an electronic device PC such as a personal computer or an office computer. This mounting is usually carried out by applying pasty solder by a screen printing method to the electrode pads (the land regions of the wiring) which are arranged on the mounting face of the mounting board, and by fixing the electrode pads of the mounting board and the outer leads of the semiconductor device 10 with solder.

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The electronic device PC is equipped with a liquid crystal display 16, a keyboard 17, a control pad 18, and a slot 19 for receiving the memory card MC.

When the connector side 20 of the memory card MC is inserted into the slot 19, data such as graphic data are transferred between the electronic device PC and the memory card MC.

This memory card MC is formed, as shown in Figs. 12, 13 and 14, into a hollow structure having a generally rectangular plate shape, for example, by sandwiching an outer frame 15 of plastic between covers 14 of stainless steel. In this structure, there is arranged the mounting board 11, one edge of which is fixed to the outer frame 15. The body of the memory card MC is constructed by mounting a plurality of semiconductor devices, as will be described with reference to Figs. 3 and 4, on the mounting board 11.

In the aforementioned memory card (electronic unit), as shown in Fig. 3 (a top plan view), a plurality of semiconductor devices 10 are directionally arranged and mounted in a matrix shape on the mounting face of a mounting board 11. In order to recognize the mounting direction of the individual semiconductor devices 10, marks 22 are made on the

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surface of the package 7. Incidentally, reference numeral 21 designates connector terminals for connection with the electronic device PC. Of these semiconductor devices 10, the semiconductor devices 10 mounted in the direction (Y-direction) perpendicular to the one side face 7A of the package 7, are shown in Fig. 4 (an enlarged top plan view of an essential portion of Fig. 3). Between two adjoining semiconductor devices 10, the outer leads 3A arrayed on the one side face 7A of the package 7 of one semiconductor device 10, and the outer leads 3B arrayed on the other side face 7B of the package 7 of the other semiconductor device 10 are opposed to each other. However, the outer leads 3A of the one semiconductor device 10 are electrically connected to the external terminals BP of the same semiconductor device 10, but the outer leads 3B of the other semiconductor device 10 are not electrically connected to the external terminals BP of the same semiconductor chip 1, so that the outer leads 3A electrically connected to the external terminals BP of the semiconductor chips 1 are not opposed to each other. As a result, even if the spacing region between the outer leads 3A of the one semiconductor device 10 and the outer leads 3B of the other semiconductor device

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10 is reduced or eliminated and if the semiconductor devices 10 are displaced or extrusion of the solder occurs at the mounting time, no short-circuiting takes place between adjoining semiconductor devices 10 which are mounted in the direction perpendicular to the one side face 7A of the package 7. In other words, in order to electrically isolate the adjoining leads 3A and 3B between the adjoining semiconductor devices 10, lands 13 (foot prints) formed on the mounting board 11 are arranged, considering predetermined spacings (the positioning allowance of the leads and the extrusion width of solder). In the case of the present embodiment, as shown in Fig. 10(A) and 10(B), the adjoining lands 13 of the wiring 12 can be formed with spacings less than the aforementioned predetermined spacings or integrated with no spacing. Moreover, the wiring 12 can be generally linearly formed below the package 7 to improve the mounting efficiency.

Between the adjoining ones of the semiconductor devices 10 mounted in the direction (Y-direction) perpendicular to the one side face 7A of the package 7, the outer leads 3B arrayed on the other side face 7B of the package 7 of one semiconductor device 10 are provided between the outer leads 3A arrayed one the one side face 7A of the package 7 of the one semi-

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conductor device 10, and the outer leads 3A arrayed on the on side face 7A of the package 7 of the other semiconductor device 10. However, the outer leads 3B arrayed on the other side face 7B of the package 7 of the one semiconductor device 10 are not electrically connected to the external terminals BP of the same semiconductor chip 1, so that there is no such outer leads between the outer leads 3A of the one semiconductor device 10 and the outer leads 3A of the other semiconductor device 10 having functions different from those of the outer leads 3A. As a result, for the leads such as chip select leads 3A (CS) which must be electrically independent, roundabout routed wiring 12A is required. For the other common signal leads or power supply leads, however without roundabout routing of the wiring 12 extending over the mounting board 11, it is possible to electrically connect the outer leads 3A of the same functions of the individual semiconductor devices 10 mounted in the direction perpendicular to the one side face 7A of the package 7, through the generally straight wiring 12.

Thus, the following effects can be achieved in the present embodiment.

(1) Semiconductor devices 10 mounted on the mounting

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face of the mounting board 11 has a structure in which the semiconductor chip 1 is packaged in a package 7 having a rectangular plane shape, a plurality of outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed along the one side face of the package 7, and a plurality of outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed along the other side face 7B opposed to the one side face 7A of the package 7. When these semiconductor devices 10 are mounted on the mounting face of the mounting board 11 and arranged in a direction perpendicular to the one side face 7A of the package 7, between the semiconductor devices 10 adjoining in the direction, the outer leads 3A arrayed on the one side face 7A of the package 7 of the one semiconductor device 10, and the outer leads 3B arrayed on the other side face 7B of the package 7 of the other semiconductor device 10 are opposed to each other. However, the outer leads 3A of the one semiconductor device 10 are electrically connected to the external terminals BP of the semiconductor chip 1, but the outer leads 3B of the other semiconductor device 10 are not electrically connected to the external terminals BP of the semiconductor chip 1, so

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that the outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are not opposed to each other. As a result, even if the spacing region between the outer leads 3A of the one semiconductor device 10 and the outer leads 3B of the other semiconductor device 10 is reduced or eliminated and if the semiconductor devices 10 are displaced or extrusion of the solder occurs at the mounting time, no short-circuit takes place between the adjoining ones of the semiconductor devices 10 which are mounted in the direction perpendicular to the one side face 7A of the package 7. As a result, the spacing region between the outer leads 3A of the one semiconductor device 10 and the outer leads 3B of the other semiconductor device 10 can be reduced or eliminated to mount the semiconductor devices 10 on the mounting board 11 in an accordingly high density.

Moreover, when the semiconductor devices 10 are arranged in the direction perpendicular to the one side face 7A of the package 7 and mounted on the mounting face of the mounting board 11, between the semiconductor devices 10 adjoining in that direction, the outer leads 3B arrayed on the other side face 7B of the package 7 of one semiconductor device 10 are present between the outer leads 3A arrayed one the one

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side face 7A of the package 7 of the one semiconductor device 10, and the outer leads 3A arrayed on the on side face 7A of the package 7 of the other semiconductor device 10. However, the outer leads 3B arrayed on the other side face 7B of the package 7 of the one semiconductor device 10 are not electrically connected to the external terminals BP of the same semiconductor chip 1, so that there is not present such outer leads between the outer leads 3A of the one semiconductor device 10 and the outer leads 3A of the other semiconductor device 10 having functions different from those of the outer leads 3A. As a result, without roundabout routing of the wiring 12 extending in the Y-direction on the mounting board 11, it is possible to electrically connect the outer leads 3A of the same functions of the individual semiconductor devices 10 mounted in the direction perpendicular to the one side face 7A of the package 7. As a result, the wiring region can be reduced or eliminated to mount the semiconductor devices 10 at an accordingly high density on the mounting board 11.

By the outer leads 3A arranged on the one side face 7A of the package 7 and the outer leads 3B arrayed on the other side face 7B of the package 7, moreover, the semiconductor devices 10 can be stably

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fixed to the mounting board 11 thereby to enhance the shock resistance of the semiconductor devices 10.

(2) In the memory card (electronic unit), a plurality of semiconductor devices 10 each having a structure in which a semiconductor chip 1 is encapsulated in a package 7 having a rectangular plane shape, a plurality of outer leads 3A, as electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the one side face of the package 7, and a plurality of outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the other side face 7B opposed to the one side face 7A of the package 7 are mounted on the mounting face of the mounting board 11 in the direction perpendicular to the one side face 7A of the package 7. Between the adjoining semiconductor devices 10, therefore, the spacing region between the outer leads 3A of the one semiconductor device 10 and the outer leads 3B of the other semiconductor device 10 can be reduced or eliminated to reduce the plane size of the memory card correspondingly. Without roundabout routing of the wiring 12 extending on the mounting board 11, moreover, the outer leads 3A of the same functions of the individual semiconductor devices 10 arranged in

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the direction perpendicular to the one side face 7A of the package 7 can be electrically connected. As a result, the area of the wiring 12 can be reduced or eliminated to reduce the plane size of the memory card correspondingly.

(Embodiment 2)

Fig. 5 is a top plan view showing the state that the upper portion of the package of a semiconductor device of Embodiment 22 of the present invention is removed.

As shown in Fig. 5, a semiconductor device 10 of the present embodiment is constructed of a TSOP structure. In this semiconductor device 10 of the TSOP structure, a semiconductor chip 1 is mounted on one surface of a tab 4 which is supported by four tab suspension leads 5.

A plurality of inner leads 2A are arrayed outside and along one side of the semiconductor chip 1. These individual inner leads 2A are electrically connected through bonding wires 6 to external terminals BP which are arrayed on the one side of the major surface of the semiconductor chip 1.

A plurality of inner leads 2B are arrayed outside and the other side (the other long side) opposed to the one side of the semiconductor chip 1. These

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individual inner leads 2B are not electrically connected to the external terminals BP of the semiconductor chip 1.

Outside and along one of the two sides perpendicular to the one side of the semiconductor chip 1, there are arrayed a plurality of inner leads 2C. These individual inner leads 2C are electrically connected through bonding wires 6 to a plurality of external terminals BP which are arrayed on one of the two sides perpendicular to the one side of the major surface of the semiconductor chip 1.

The aforementioned semiconductor chip 1, inner leads 2A, inner leads 2B, inner leads 2C, tab 4, tab suspension leads 5 and bonding wires 6 are encapsulated in a package 7 which is so formed as to have a rectangular plane shape.

A plurality of outer leads 3A are arrayed on one side face 7A of the package 7. A plurality of outer leads 3B are arrayed on the other side face 7B opposed to the one side face 7A of the package 7. A plurality of outer leads 3s 3C are arrayed on one 7C of the two side faces perpendicular to the one side face of the package 7. These outer leads 3A, 3B and 3C are formed into a gull-wing shape.

The outer leads 3A are individually integrated

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with the inner leads 2A which are arrayed outside the one side of the semiconductor chip 1. Moreover, the outer leads 3B are individually integrated with the inner leads 2B which are arrayed outside the other side of the semiconductor chip 1. Moreover, the outer leads 3C are individually integrated with the inner leads 2C which are arrayed outside one of the two sides perpendicular to the one side of the semiconductor chip 1. In other words, the semiconductor device 10 of the present embodiment has a three-way lead array structure in which the outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the one side face 7A of the package 7, the outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1, are arrayed on the other side face 7B opposed to the one side face 7A of the package 7, and the outer leads 3C electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the one side face 7C of the two side faces perpendicular to the one side face 7A of the package 7.

A plurality of semiconductor devices 10 thus constructed are regularly arranged on the mounting board of the memory card (electronic unit) which is

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additionally connected to the electronic device such as a personal computer or an office computer.

In the aforementioned memory card (electronic unit), as shown in Fig. 6 (a top plan view), the semiconductor devices 10 are mounted in a matrix shape in the arrangement direction on the mounting face of the mounting board 11. Of these semiconductor devices 10, the semiconductor devices 10 mounting in the same direction (X-direction) as that of the one side face 7A of the package 7 are constructed, as shown in Fig. 7 (an enlarged top plan view of an essential portion of Fig. 6), such that the outer leads 3C arrayed on the side face 7C of the package 7 of the one semiconductor device 10, and the outer leads 3C arrayed on the side face 7C of the package 7 of the other semiconductor device 10 are not opposed to each other. As a result, when the one semiconductor device 10 and the other semiconductor device 10 are mounted in a packed state and even if they are displaced or extrusion of the solder occurs at the mounting time, no short-circuit takes place between the adjoining ones of the semiconductor devices 10 which are mounted in the direction perpendicular to the one side face 7A of the package 7. As a result, the semiconductor devices 10 can be mounted in the packed state in the

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same direction as that of the one side face 7A of the package 7 thereby to mounting them at an accordingly high density.

Of the semiconductor devices 10 mounted in the same direction (the X-direction in the drawing) as that of the one side face 7A of the package 7, moreover, between the adjoining semiconductor devices 10, there are no such other outer leads between the outer leads 3C arrayed on the side face 7C of the package 7 of the one semiconductor device 10, and the outer leads 3C arrayed on the side face 7C of the package 7 of the other semiconductor device 10 having functions different from those of the outer leads 3C. Without roundabout routing of the wiring (not-shown) extending in the X-direction inside the mounting board, therefore, it is possible to electrically connect the outer leads 3C of the same functions of the individual semiconductor devices 10 which are mounted in the same direction as that of the one side face 7A of the package 7. As a result, the wiring region of the wiring extending in the X-direction can be reduced or eliminated to mount the semiconductor devices 10 at an accordingly high density. In other words, the area where the wiring is routed in a roundabout way can be reduced to the minimum by

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linearly connecting the outer leads 3A of the semiconductor devices 10 adjoining each other in the Y-direction to each other through the surface wiring layer 12 of the mounting board and by linearly connecting the outer leads 3C of the semiconductor devices 10 adjoining each other in the X-direction to each other through only one specific layer of the internal wiring of the mounting board.

(Embodiment 3)

Fig. 8 is a top plan view showing the state that the upper portion of the package of a semiconductor device of Embodiment Mode is removed.

As shown in Fig. 8, the semiconductor device 10 of the present embodiment is constructed of a two-way lead array structure in which a semiconductor chip 1 is encapsulated in a package 7 having a rectangular plane shape, in which a plurality of outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on a part of the one side face 7A of the package 7 and along the one side face, a plurality of outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the other region of the one side face 7A of the package 7 and along the one side face, in which a plurality of outer

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leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on a part of the other side face 7B opposed to the partial region of the one side face 7A of the package 7 and along the other side face, and a plurality of outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the other region of the other side face 7B opposed to the other region of the one side face 7A of the package 7 and along the other side face.

When the semiconductor devices 10 thus constructed are mounted in plurality in a matrix shape in a direction on the mounting face of the mounting board, between the adjoining ones 10 of the semiconductor devices 10 mounted in the direction perpendicular to the one side face 7A of the package 7, like Embodiment 1, the outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are not opposed to each other. Between the adjoining ones 10 of the semiconductor devices 10 mounted in the direction perpendicular to the one side face 7A of the package 7, moreover, there are no such outer leads between the outer leads 3A of the one semiconductor device 10 and the outer leads 3A of the other semiconductor device 10 having functions

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different from those of the outer leads 3A. As a result, like Embodiment 1, the semiconductor devices 10 can be mounted at a high density.

(Embodiment 4)

Fig. 9 is a top plan view showing the state that the upper portion of the package of a semiconductor device of Embodiment 4 is removed.

As shown in Fig. 9, the semiconductor device 10 of Embodiment 4 is constructed of a three-way lead array structure in which a semiconductor chip 1 is encapsulated in a package 7 having a rectangular plane shape, in which a plurality of outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on a part of the one side face 7A of the package 7 and along the one side face, a plurality of outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the other part of the one side face 7A of the package 7 and along the one side face, a plurality of outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on a part of the other side face 7B opposed to a part of the one side face 7A of the package 7 and along the other side face, a plurality of outer leads 3A electrically

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connected to the external terminals BP of the semiconductor chip 1 are arrayed on the other part of the other side face 7B opposed to the other part of the one side face 7A of the package 7 and along the other side face, and a plurality of outer leads 3C electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed along one side face 7C of the two side faces perpendicular to the one side face 7A of the package 7.

When the semiconductor devices 10 thus constructed are mounted in plurality in a matrix shape in a direction on the mounting face of the mounting board, between the adjoining ones 10 of the semiconductor devices 10 mounted in the same direction as that of the one side face 7A of the package 7, like the foregoing Embodiment Mode 2, the outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are not opposed to each other. As a result, like Embodiment 1, the semiconductor devices 10 can be mounted at a high density.

(Embodiment 5)

Fig. 15 is a top plan view showing a semiconductor device (package) of Embodiment 5.

A semiconductor device 100 is constructed, as in

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Embodiment 1, of a TSOP structure, and a semiconductor chip 23 mounted with a flash memory (EEPROM) shown in Fig. 17 is encapsulated in a package 7. Over the major surface of the semiconductor chip 23, there are formed four memory arrays MA each having a plurality of memory cells arranged in a matrix shape, word decoders WD, column decoders CD and sense amplifiers SA for selecting a predetermined memory cell from each memory array MA, a power supply circuit VC having a power voltage generator and a booster circuit, a control circuit CC serving as an interface with an external device such as an input/output circuit. Moreover, the bonding pads BP are arranged along only one long side of the semiconductor chip 23, and the peripheral circuits including the power supply circuit VC and the control circuit CC are positively arranged in the vicinities of the bonding pads BP to equalize the signal wiring lengths in the chip and to reduce the chip size. The individual bonding pads BP correspond to power supply pins and signal pins Vcc, Vss, I/O and so on, as shown in Figs. 15 and 16, and are connected through the wires 6 to the inner leads 2A of the corresponding power supply pins and signal pins. The individual pin functions are shown in Fig. 16, and the NC pins (3B) are in an electrically

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floating state in the package.

The aforementioned semiconductor devices 100 are mounted on the mounting board 11, as shown in Figs. 18 and 19, constituting the body of the memory card. Fig. 18 is a top plan view showing the front side of the mounting board 11, and Fig. 19 is a top plan view showing the back side, opposed to the surface side, of the mounting board 11. Fig. 20 is a section taken along lines A-A of Figs. 18 and 19.

On the back side of the mounting board 11, there are mounted a QFP package GA mounted with a gate array chip, a QFP package MPU mounted with microcomputer, and a TSOP package DM mounted with a DRAM chip. On the mounting board 11, moreover, there are mounted a chip capacitor C and a chip resistor R for matching the impedance, and a clock generator GE for feeding clock signals.

The packages thus mounted on the mounting board 11 constitutes an ATA (AT Attachment) card 24, as shown in Fig. 21. Here will be briefly described the system configuration of the ATA card 24.

The ATA (AT Attachment) card 24 of Fig. 21 conforms to the interface and protocol which are used when an AT compatible machine makes an access to a hard disk and is standardized by the PCMCIA (Personal

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Computer Memory Card International Association).

Numeral 25 designates a pin connector section of the ATA card, corresponding to the external terminals 21, through which signals are exchanged with a PC (Personal Computer) or a PDA (Personal Digital Assistant). The number, names and Nos. of the external terminals are determined by the PCMCIA.

The data and addresses from the outside are introduced at first through signal lines 26 into the gate array GA. This gate array GA controls the PCMCIA interface (PCIN), the microcomputer MPU, the DRAM (Dynamic Random Access Memory), the flash memory 100, and the data transfer between the flash memory 100 and the PCMCIA interface. The exchanges of the data and addresses between the individual elements in the card are executed through the local data bus and the local address bus designated by numeral 27.

The MPU controls the data according to commands from the outside. The data from the outside are fed through the DRAM to the flash memory 100 or from the flash member 100 to the DRAM so that they may be processed, i.e., written in or read out at high rate. Moreover, the MPU controlles through a CE (Chip Enable) bus 28 which flash memory 100 data are to be written in or read out. In order to improve the

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reliability of the data stored in the flash memory 100, moreover, the MPU controls the ECC (Error Check Correction) processing (control of the number of rewrites of the individual sectors, control of the access to defective sectors) and the ware leveling (averaging the number of rewrites of the individual sectors).

Although the invention made by us has been specifically described, taking the case of Embodiments, it should not be limited thereto but can naturally be modified in various manners without departing from the gist thereof.

For example, the present invention can be applied to a semiconductor device in which the semiconductor chip is encased in a package made of ceramic.

Moreover, the present invention can be applied to a semiconductor device having an LOC (Load On Chip) structure or a COL (Chip On Lead) structure.

Moreover, the present invention can be applied to a semiconductor device in which is mounted a semiconductor chip constructed of a memory circuit system made up of a SRAM (Static Random Access Memory), an EPROM (Electrically Programmable Read Only Memory), an EEPROM (Electrically Erasable Programmable ROM) and a flash memory (flash EEPROM).

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WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

(1) a generally rectangular semiconductor chip having a plurality of bonding pads and a plurality of semiconductor elements over its major surface,

said semiconductor chip having a pair of long sides extending in a first direction and a pair of short sides extending in a second direction generally perpendicular to said first direction, and

said bonding pads being arranged along one of said pair of long sides;

(2) a plurality of first leads arranged outside said semiconductor chip and along the one of said pair of long sides,

said first leads individually including inner lead portions and outer leads, and the leading end portions of said inner lead portions being electrically connected to the corresponding bonding pads by bonding wires;

(3) a plurality of second leads arranged outside said semiconductor chip and along the other of said paired long sides,

said second leads individually including inner lead portions and outer leads, and

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said second leads being not electrically connected to said semiconductor chip; and

(4) a package in which said semiconductor chip, the inner lead portions of said first leads, the inner lead portions of said second leads, and said bonding wires are packaged,

said package being formed into a generally rectangular shape having a pair of long sides extending in said first direction and a pair of short sides extending in said second direction,

wherein the outer leads of said first leads protrude from one of the paired long sides of said package whereas the outer leads of said second leads protrude from the other of said paired long sides, and wherein the outer leads of said first leads and the outer leads of said first leads arranged in positions opposed to each other are electrically connected outside said package.

2. A semiconductor device according to claim 1, wherein the outer leads of said first leads and the outer leads of said second leads protrude from said package in parallel with said second direction, and the outer leads of said opposed first and second leads are arranged generally linearly in said second

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direction.

3. A semiconductor device according to claim 1, wherein said opposed first and second leads are connected through wiring outside said package.

4. A semiconductor device according to claim 1, wherein said semiconductor chip includes a memory array formed on its major surface, and an input/output circuit arranged between said memory array and said bonding pads.

5. A semiconductor device comprising:

(a) a mounting board having a plurality of wirings on its major surface; and

(c) a plurality of semiconductor packages mounted on the major surface of said mounting board,

each of said semiconductor packages including:

(1) a generally rectangular semiconductor chip having a plurality of bonding pads and a plurality of semiconductor elements on its major surface,

said semiconductor chip having a pair of long sides extending in a first direction and a pair of short sides extending in a second direction generally perpendicular to said first direction, and

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said bonding pads being arranged along one of said pair of longer sides;

(2) a plurality of first leads arranged outside said semiconductor chip and along the one of said pair of long sides,

said first leads individually including inner lead portions and outer leads, and the leading end portions of said inner lead portions being electrically connected to the corresponding bonding pads by bonding wires;

(3) a plurality of second leads arranged outside said semiconductor chip and along the other of said paired long sides,

said second leads individually including inner lead portions and outer leads, and said second leads being not electrically connected to said semiconductor chip; and

(4) a package in which said semiconductor chip, the inner lead portions of said first leads, the inner lead portions of said second leads, and said bonding wires are packaged,

said package being formed into a generally rectangular shape having a pair of long sides extending in said first direction and a pair of short sides extending in said second direction,

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the outer leads of said first leads protruding from one of the pair of long sides of said package, and

the outer leads of said second leads protruding from the other of said pair of long sides,

wherein said semiconductor packages are so arranged at predetermined spacings in said second direction that the first leads and the second leads of the adjoining semiconductor packages are opposed to each other, and wherein the leading ends of the outer leads of the first leads and the second leads of said adjoining semiconductor packages are connected through the wiring which is formed on the major surface of said mounting board.

6. A semiconductor device according to claim 5, wherein the leading end portions of the first leads of said adjoining semiconductor packages are arranged on first land portions of said wiring whereas the leading end portions of the second leads of said adjoining semiconductor packages are arranged on second land portions of said wiring, and wherein the spacing between said first land portions and said second land portions is narrower than the spacing between said outer leads.

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7. A semiconductor device according to claim 5, wherein the leading end portions of the first leads of said adjoining semiconductor packages are arranged on first land portions of said wiring whereas the leading end portions of the second leads of said adjoining semiconductor packages are arranged on second land portions of said wiring, and wherein said first land portions and said second land portions are integrally formed.

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ABSTRACT OF THE DISCLOSURE

Disclosed are a resin-encapsulated semiconductor package and a packaging structure, suited for a high density mounting. Specifically, outer leads are protruded from the two long sides of a rectangular package. The inner leads in the package, connected to the outer leads protruding from one long side, are connected through wires to the bonding pads of a semiconductor chip encapsulated in the package, whereas the inner leads in the package, connected to the outer leads protruding from the other long side, are in an electrically floating state in the package. The semiconductor packages are arranged in a direction on a card-shaped mounting board, and the opposed outer leads of adjoining semiconductor packages are electrically connected by wiring on the mounting board. The wiring is so laid below the semiconductor packages that they extend generally linearly.

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FIG. 1

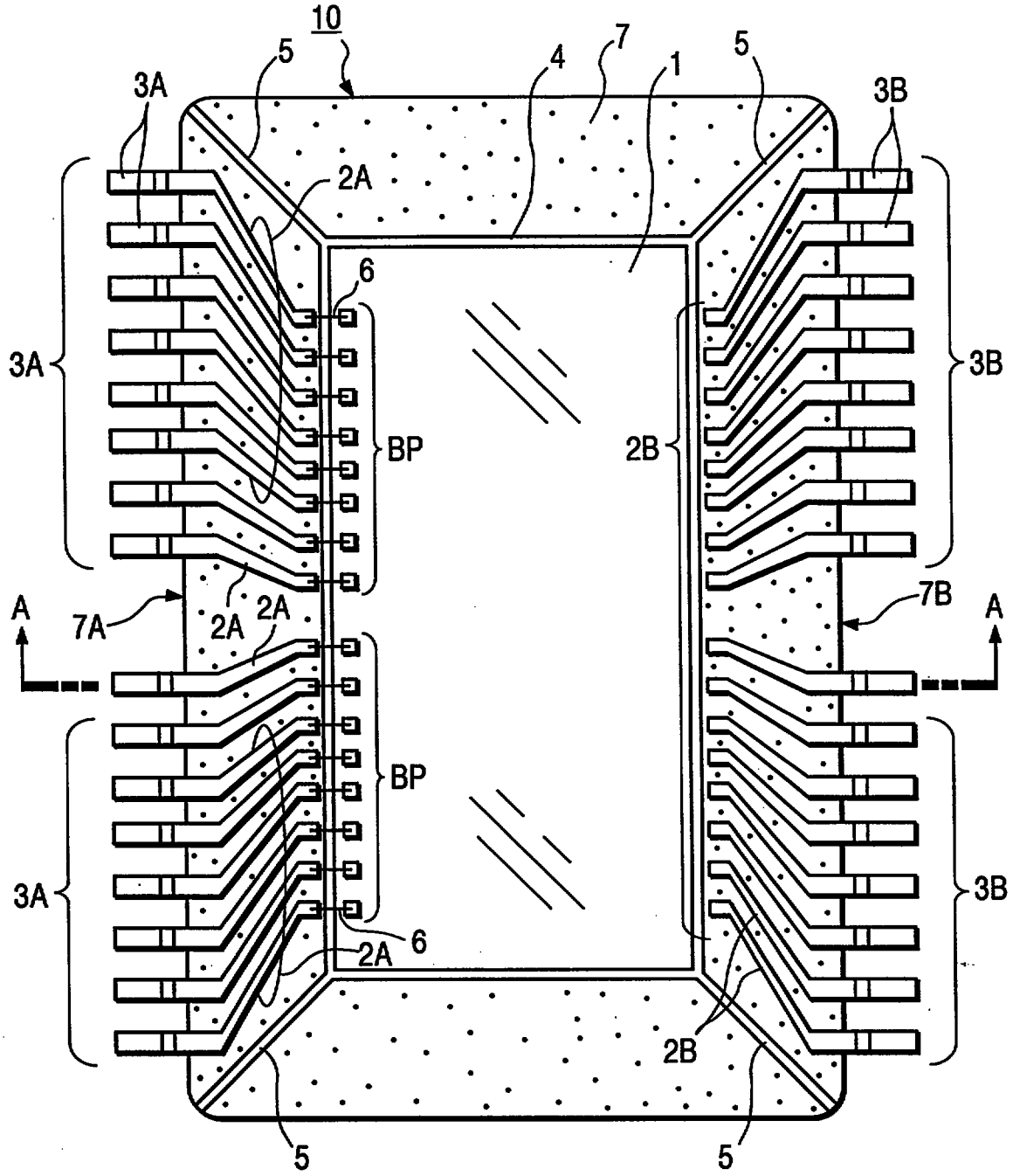
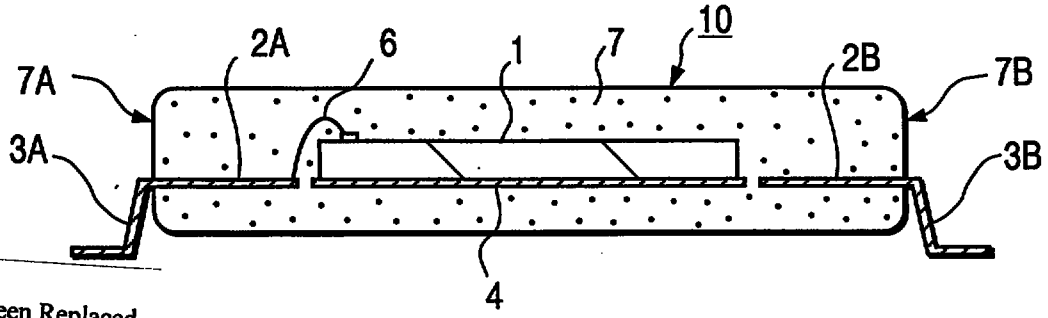


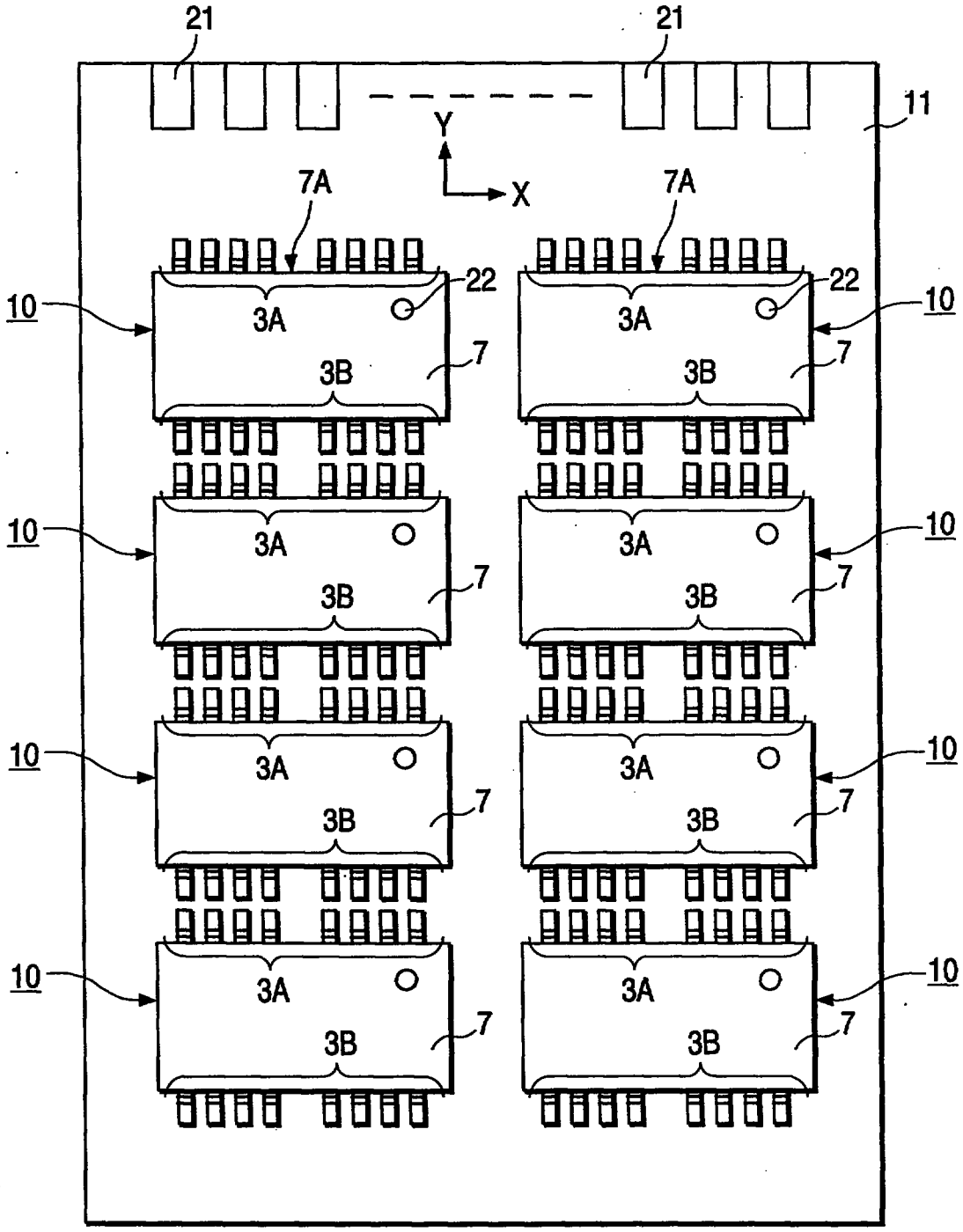
FIG. 2



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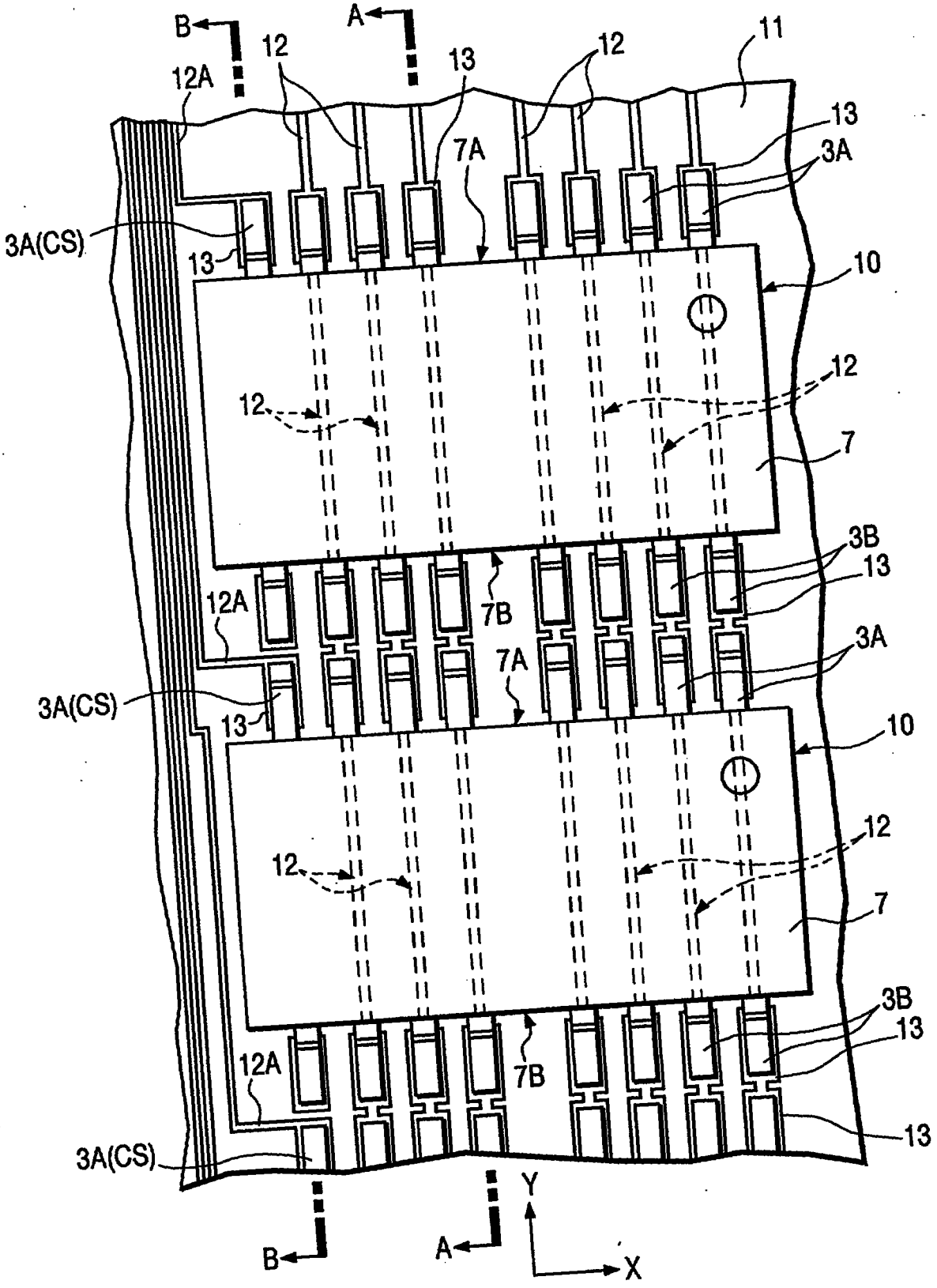
FIG. 3



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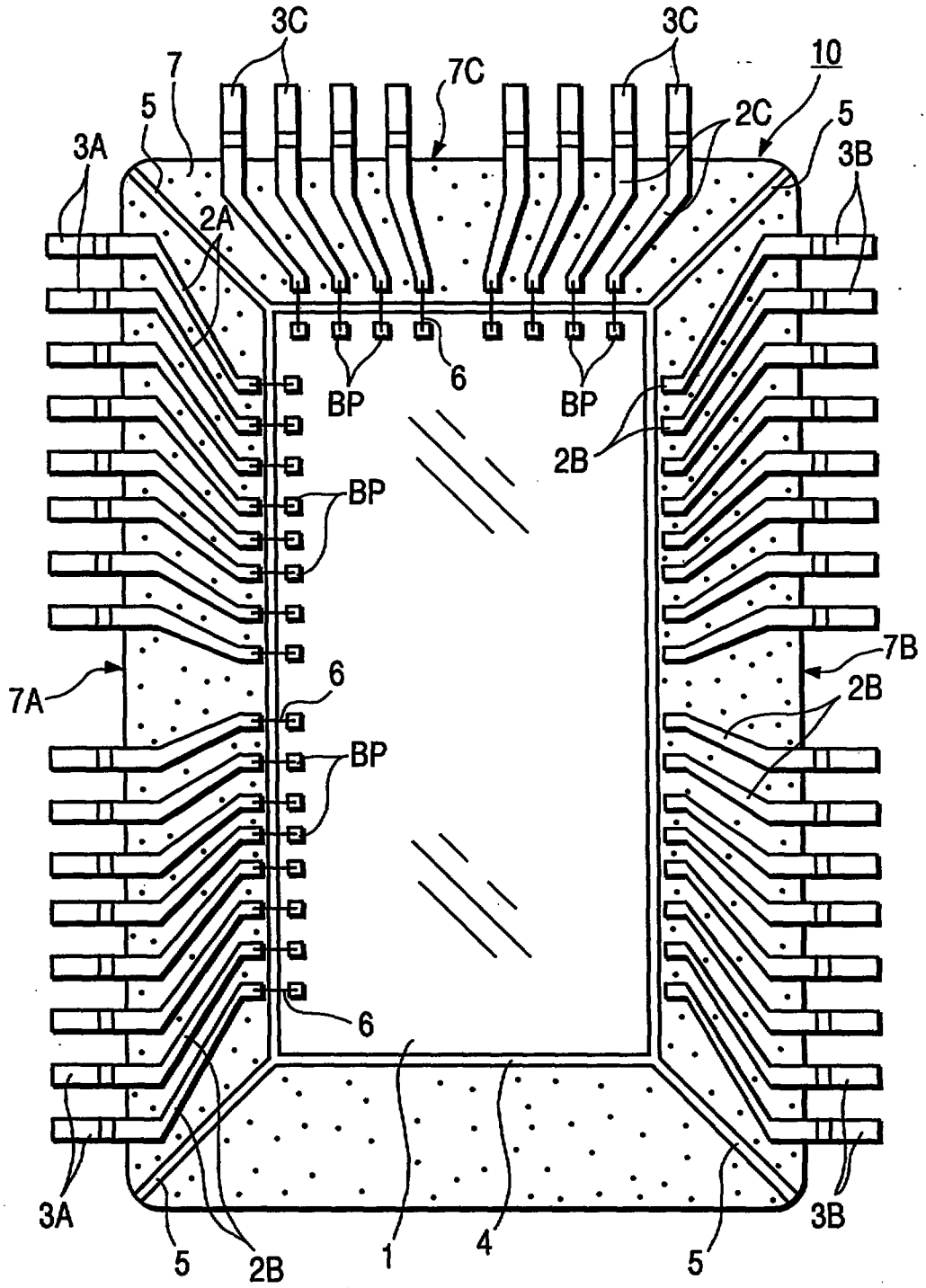
FIG. 4



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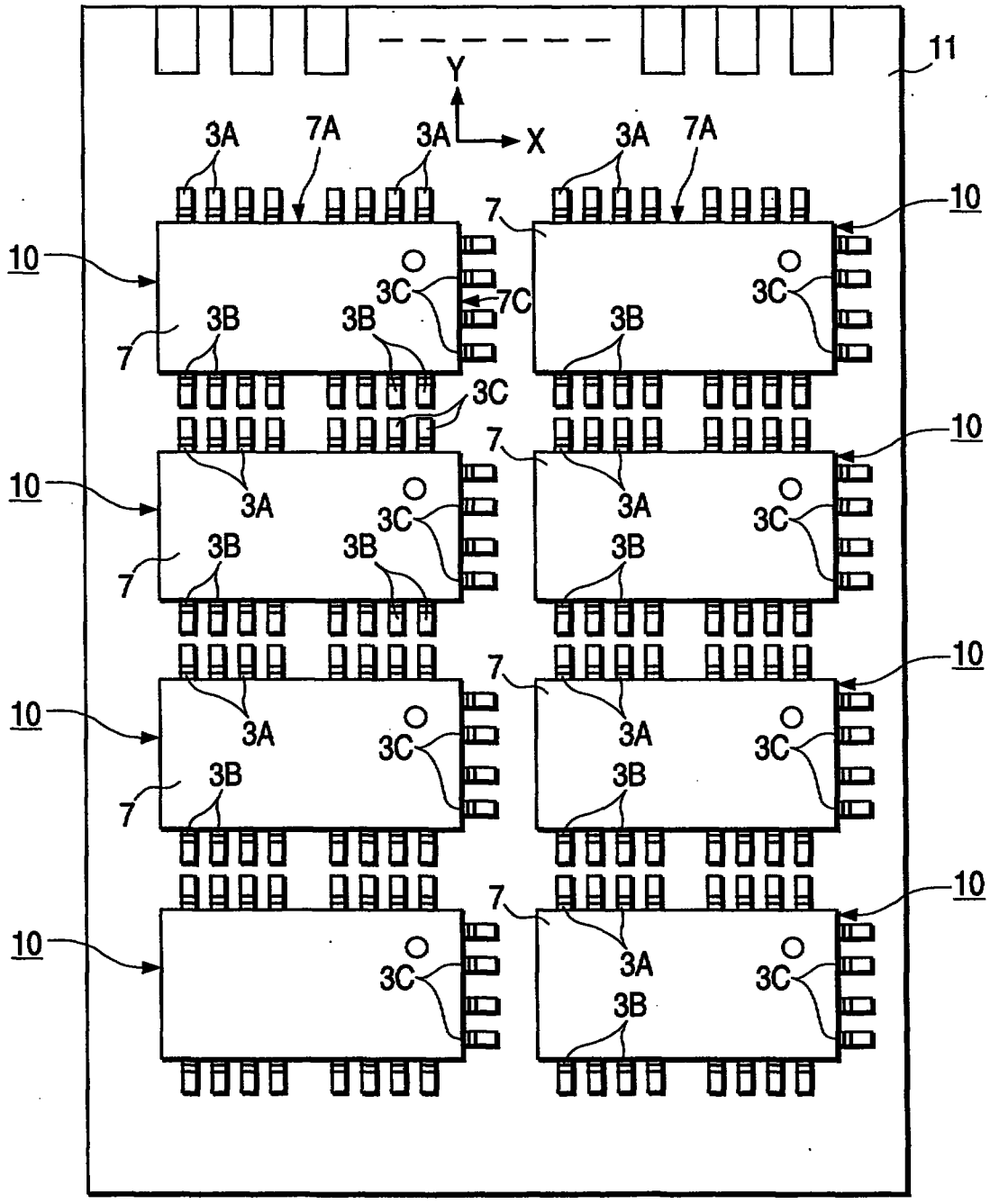
FIG. 5



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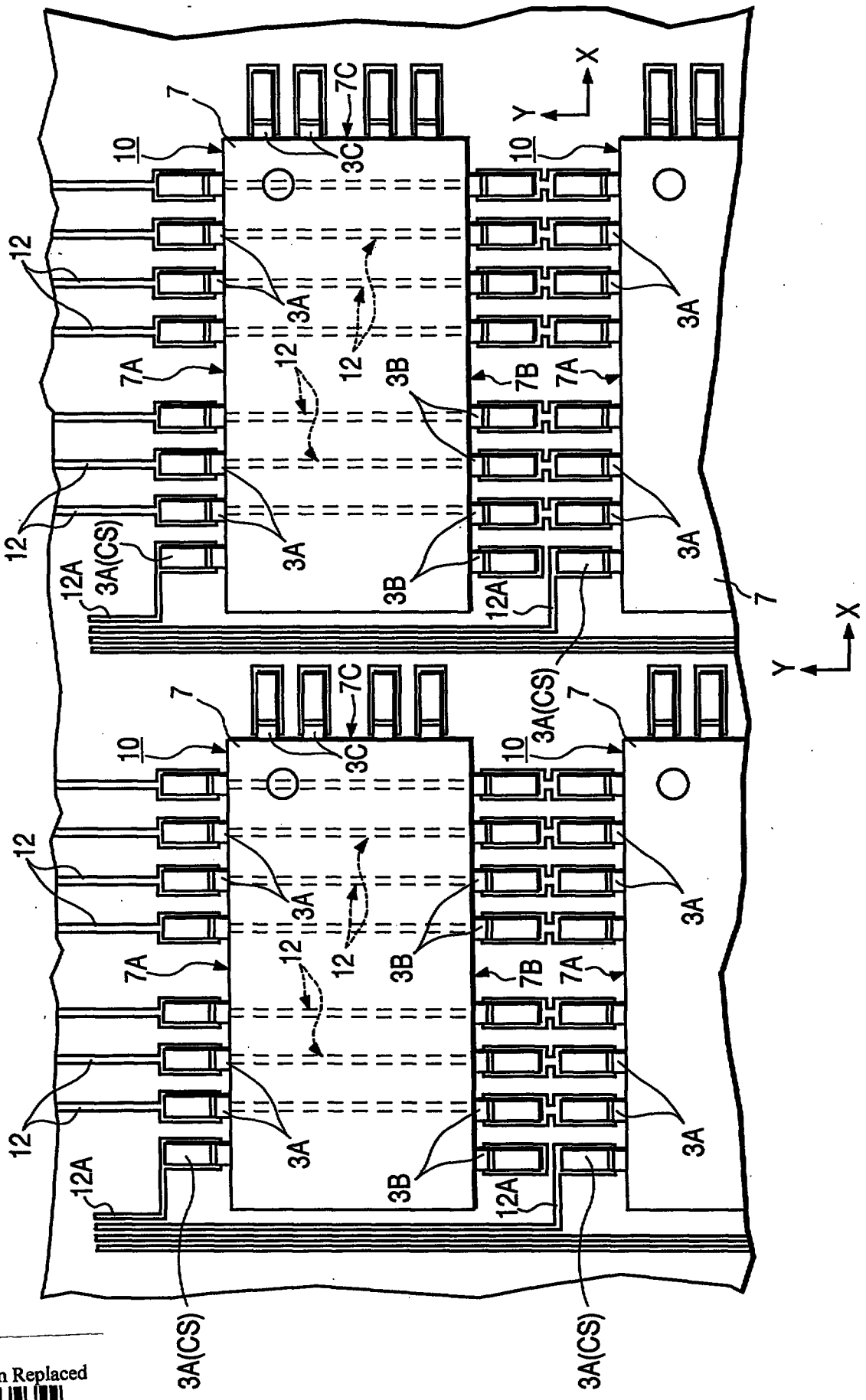
FIG. 6



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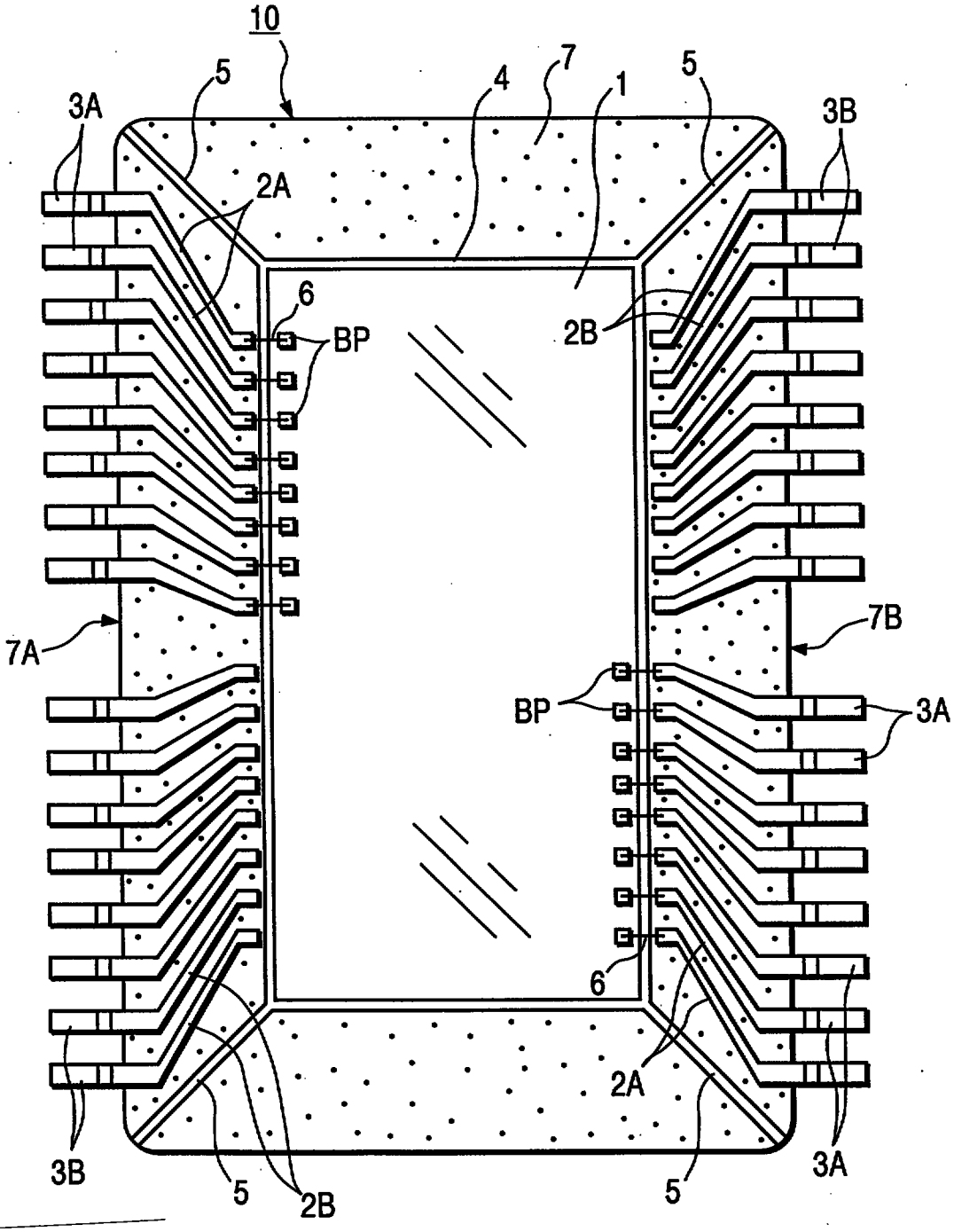
FIG. 7



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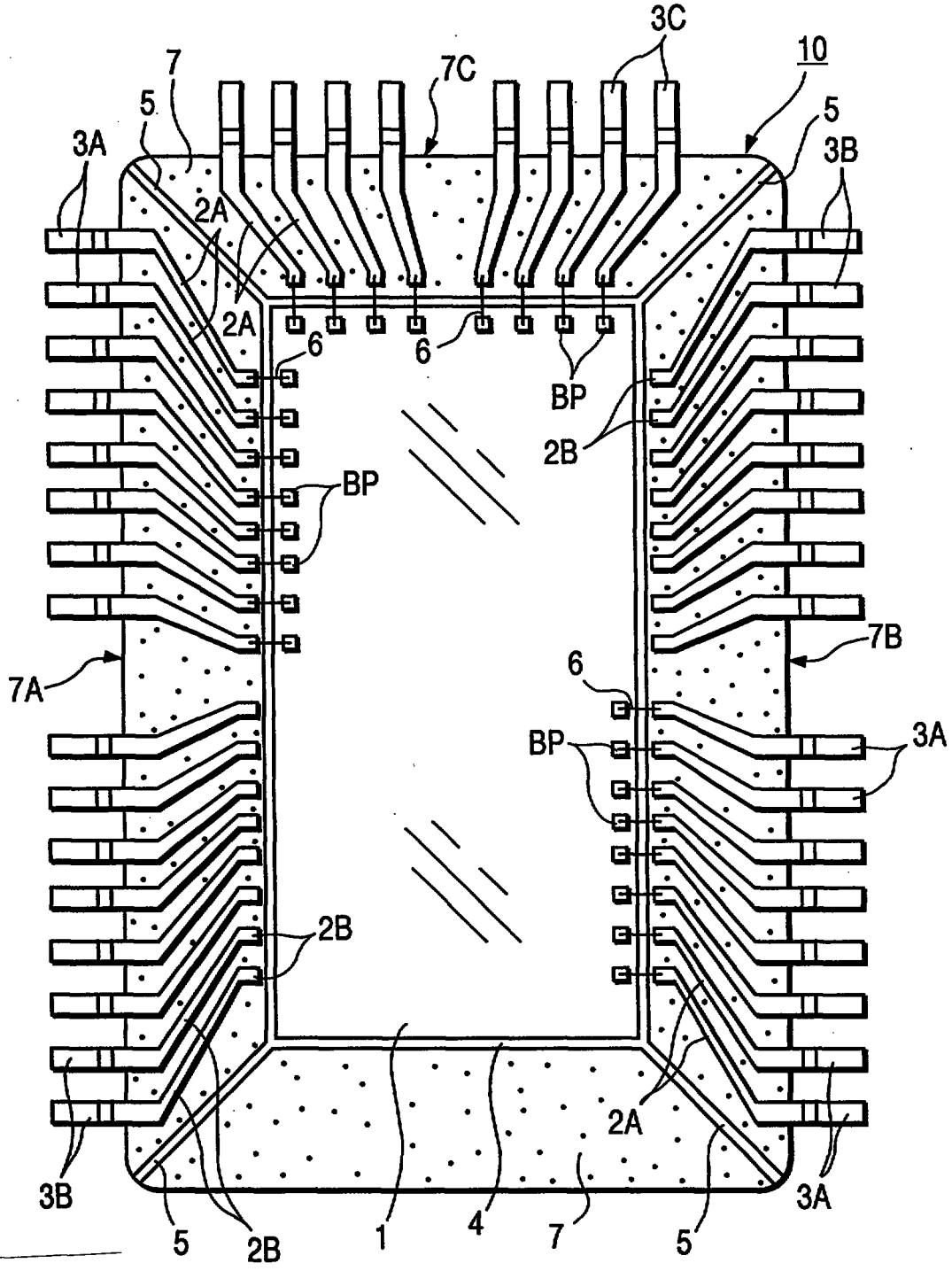
FIG. 8



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FIG. 9



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FIG. 10(A)

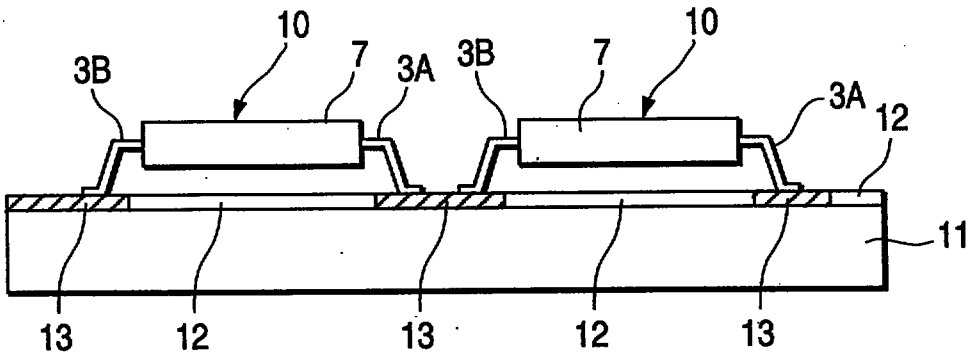


FIG. 10(B)

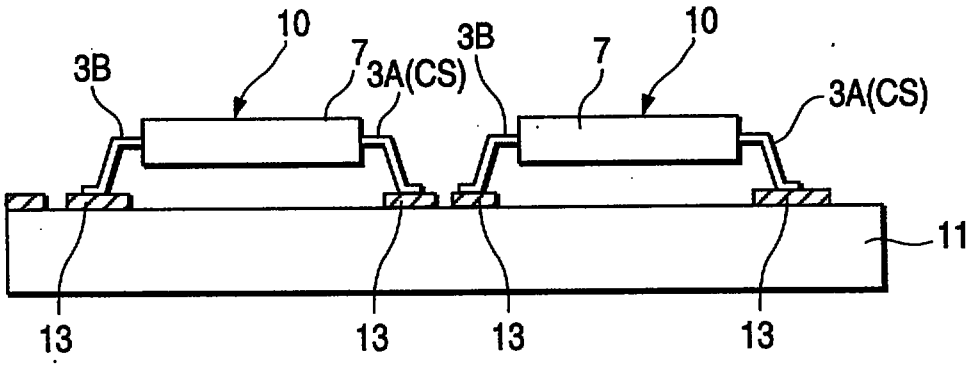
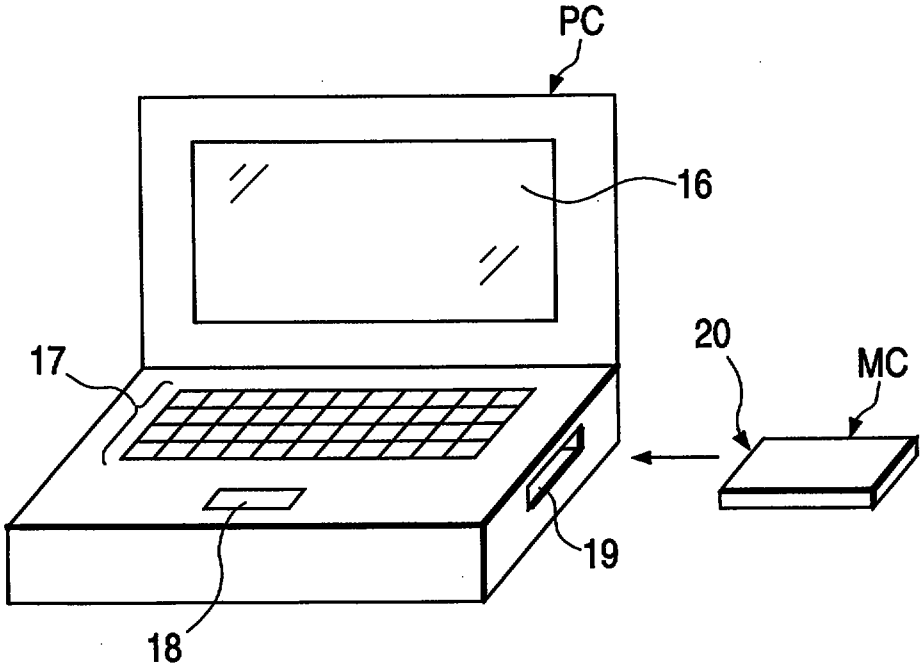


FIG. 11



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FIG. 12

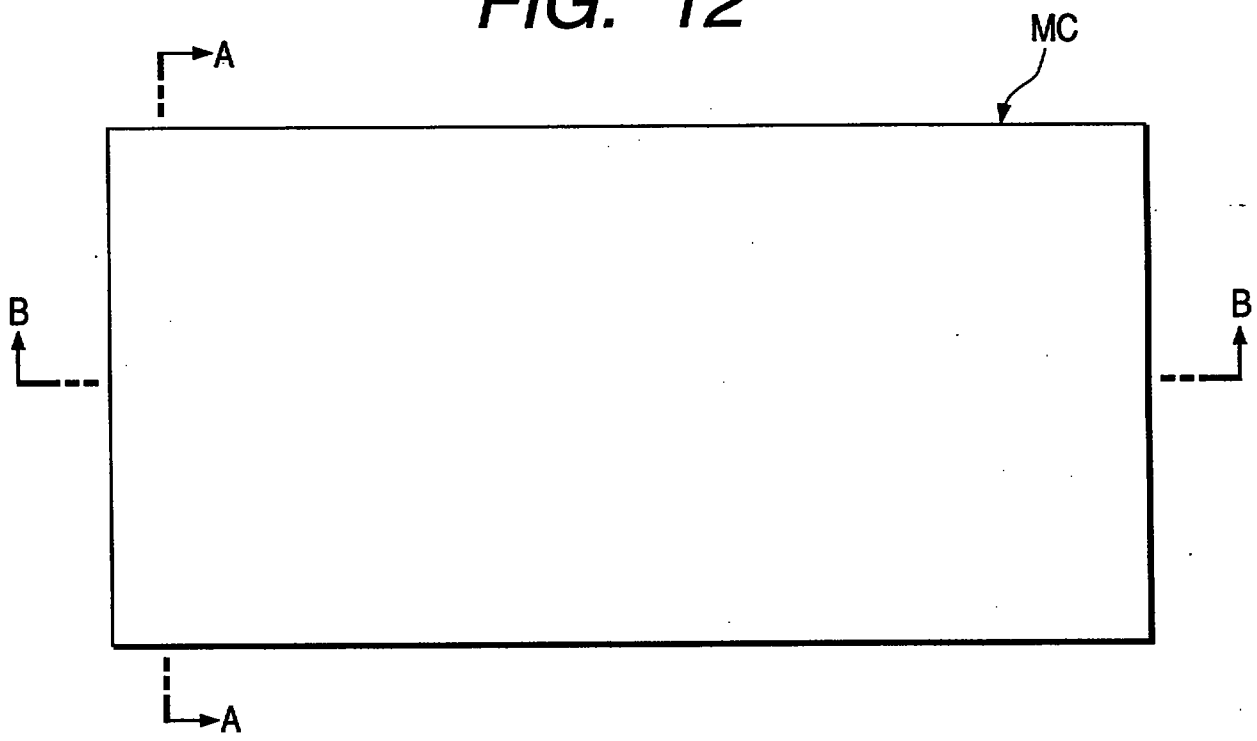


FIG. 13

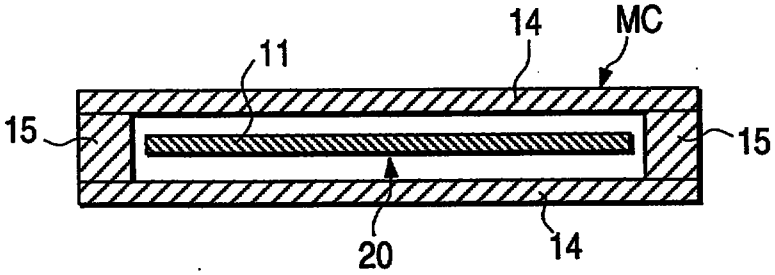
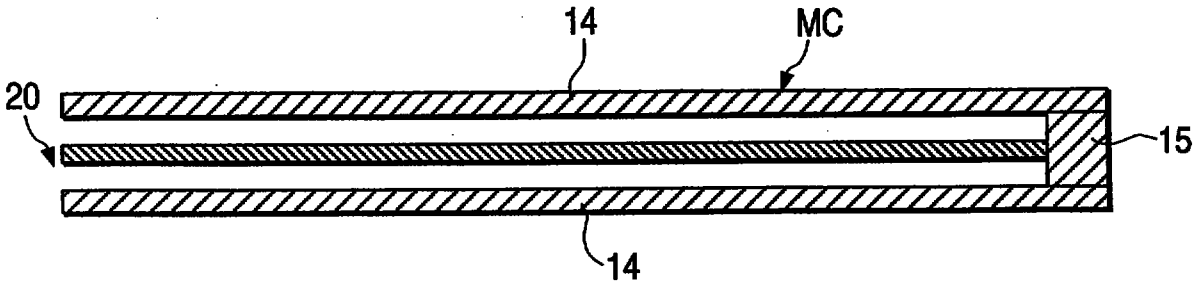


FIG. 14



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FIG. 15

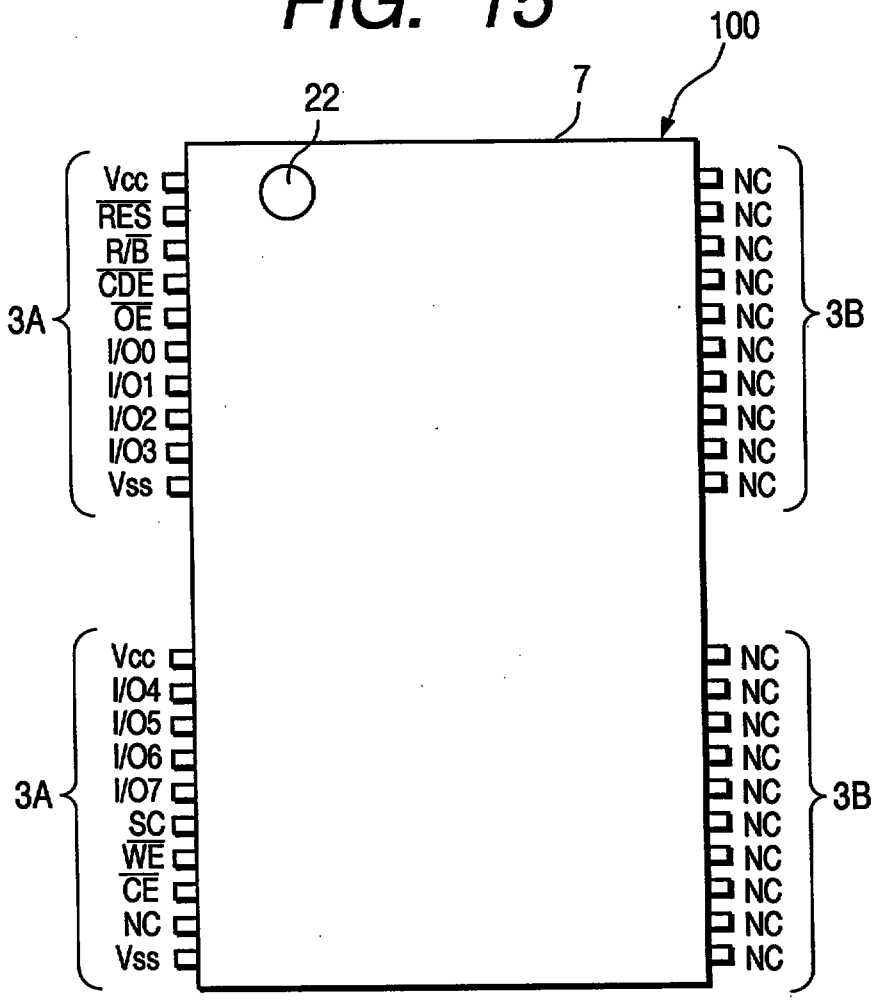


FIG. 16

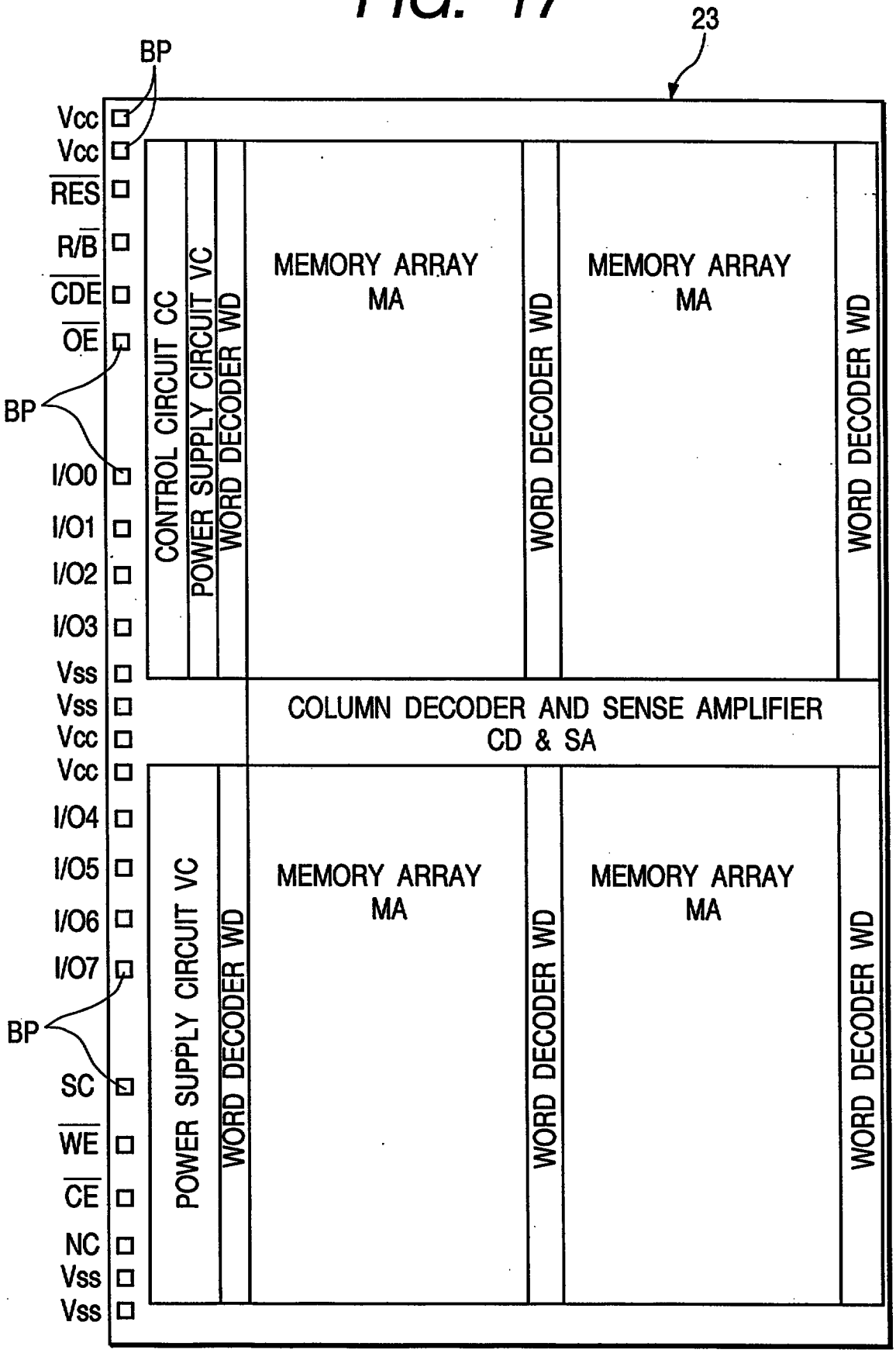
PIN DESCRIPTION	
PIN NAME	FUNCTION
I/O0-I/O7	INPUT / OUTPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
$\overline{CDE}$	COMMAND DATA ENABLE
Vcc	POWER SUPPLY
Vss	GROUND
R/$\overline{B}$	READY / $\overline{BUSY}$
$\overline{RES}$	RESET
SC	SERIAL CLOCK
NC	NO CONNECT

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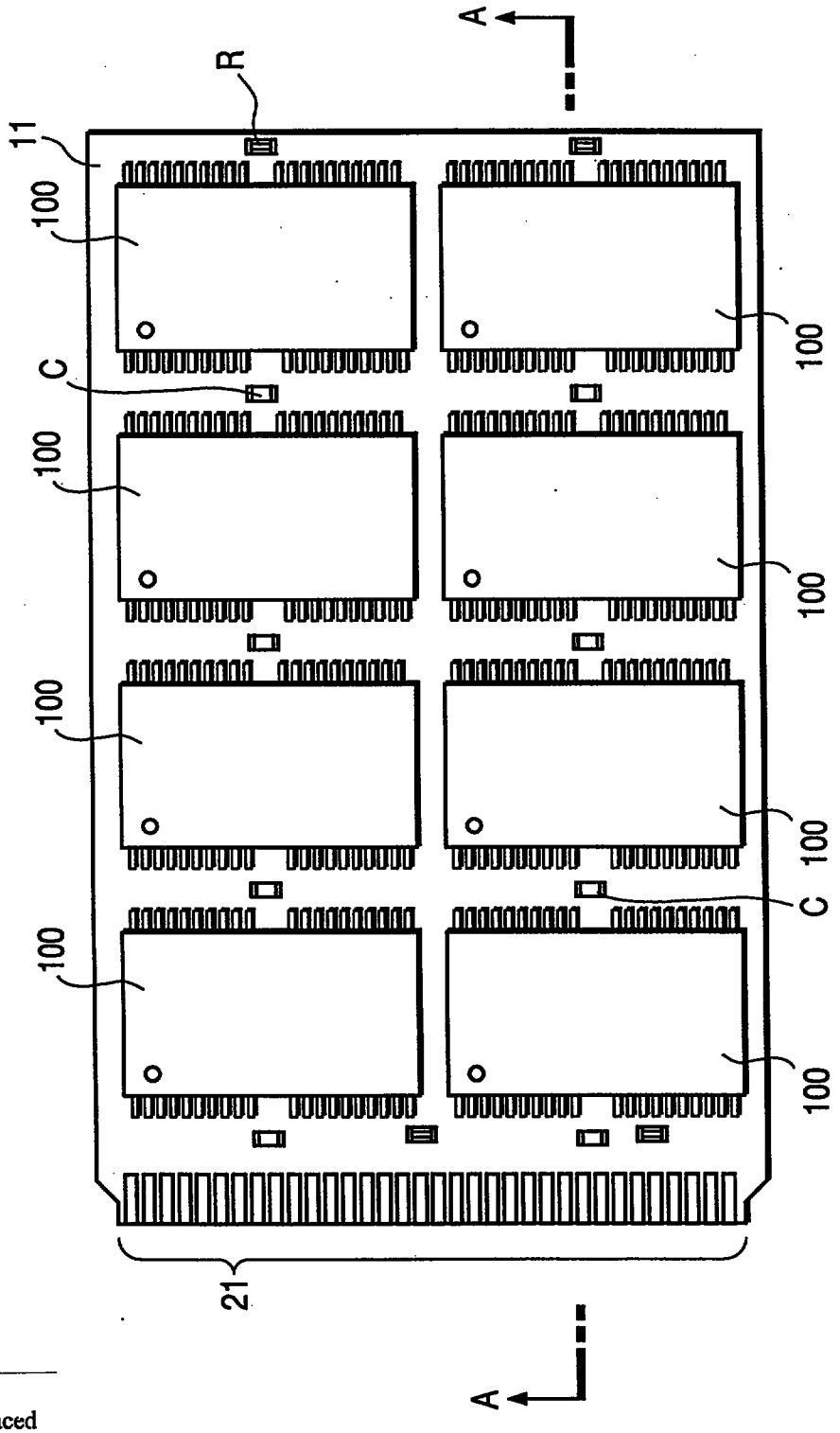
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FIG. 17



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FIG. 18



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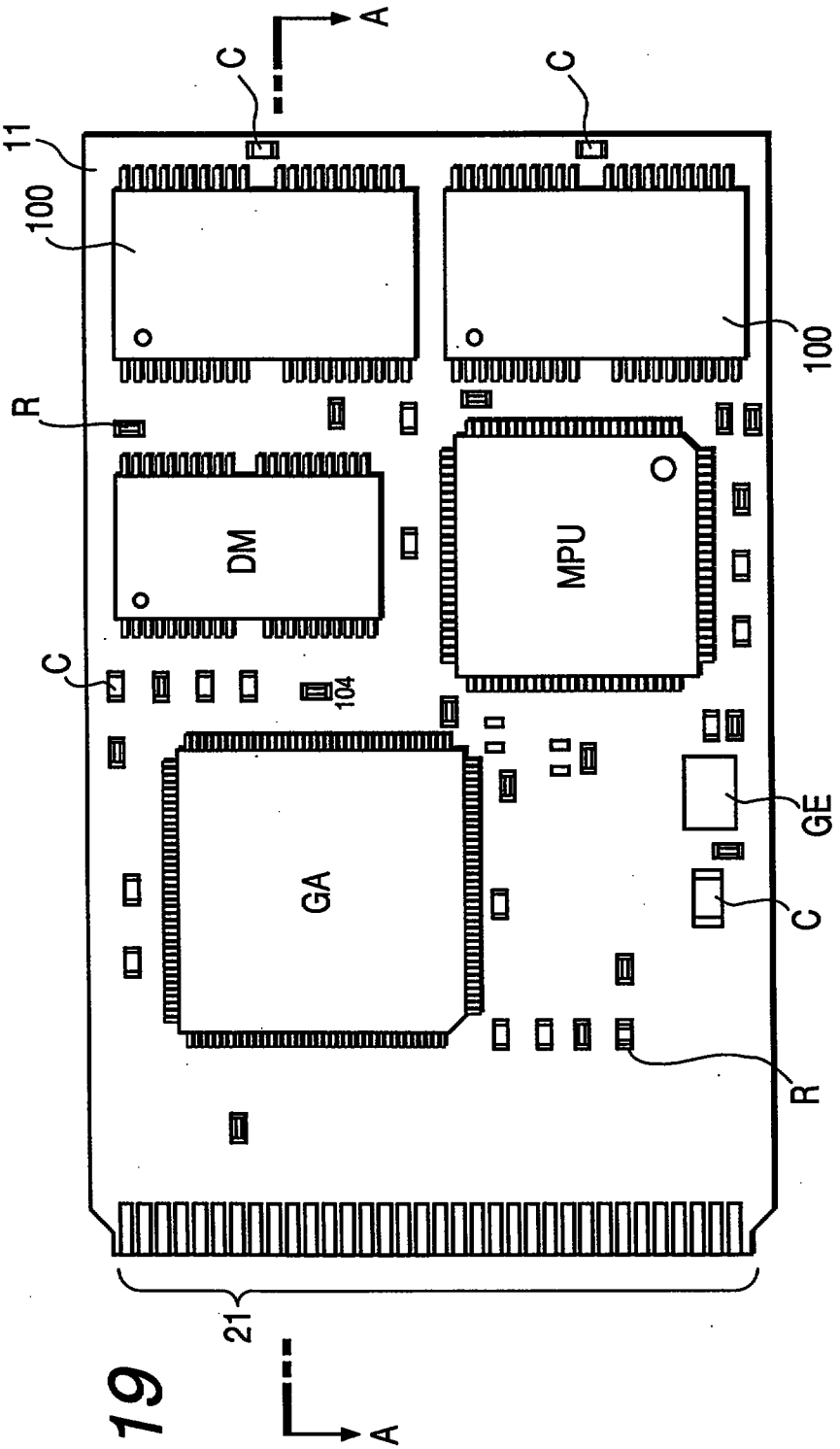


FIG. 19

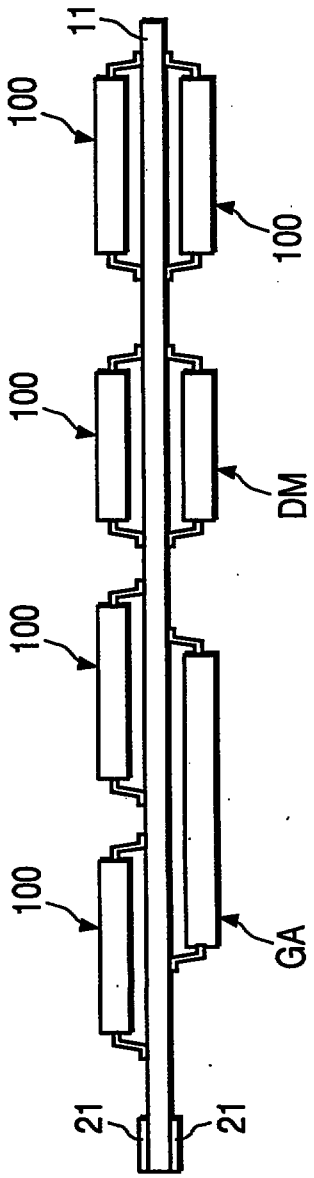


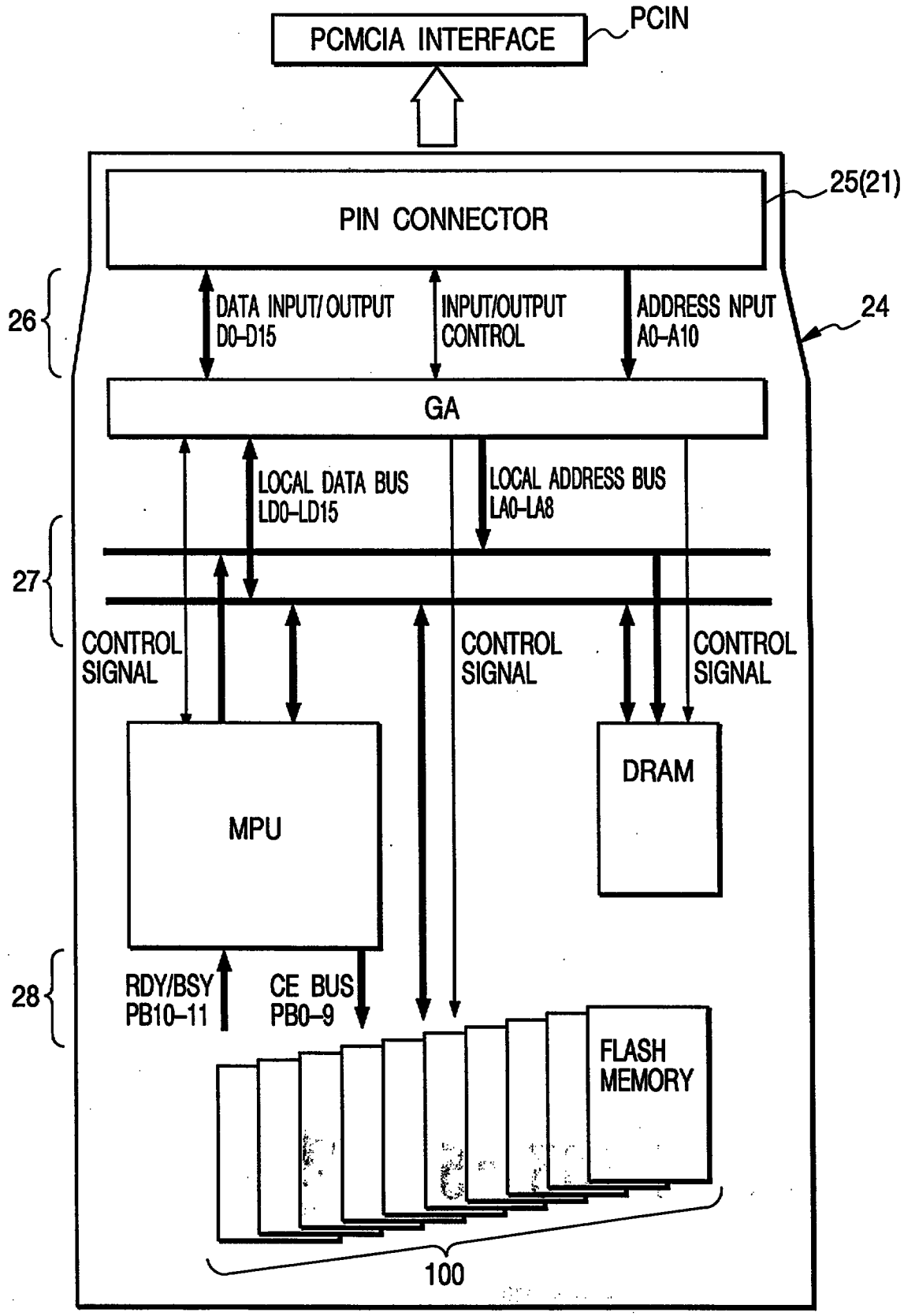
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FIG. 21



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SPECIFICATION

TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and, more particularly, to a technique which is effective when applied to the mounting of a plurality of semiconductor devices on the mounting face of a mounting board.

As a semiconductor device suitable for the reduced size or thickness of an electronic device, there is a semiconductor device having the TSOP (Thin Small Out-line Package) structure. In this semiconductor device of the TSOP structure, for example, a semiconductor chip, constituted of a DRAM (Dynamic Random Access Memory), is encapsulated in a package made of resin.

This package is so formed as to have a rectangular plane shape. At and along one side face of the package, there are arranged a plurality of outer leads. These outer leads are individually so formed as to have a gull-wing shape and are individually connected electrically to a plurality of external terminals (bonding pads) arrayed on one side

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of a major surface of the semiconductor chip. On the other side face opposed to the one side face of the package, moreover, there are arrayed a plurality of outer leads. These outer leads are individually so formed as to have a gull-wing shape and are individually connected electrically with a plurality of external terminals which are arrayed on the other side of the principal face of the semiconductor chip. In short, the semiconductor device of TSOP structure is constructed of a two-way lead array structure in which a plurality of outer leads electrically connected to the semiconductor chip are individually arrayed on the two side faces of the package, opposed to each other.

Semiconductor devices of the TSOP structure thus constructed are regularly mounted over the mounting board of a memory card which is additionally connected to an electronic device such as a personal computer or office computer. This mounting is usually performed by printing the electrode pads (the land regions of the wiring), arranged over the mounting face of the mounting board, with pasty solder by a screen printing method, and by fixing the electrode pads of the mounting board and the outer leads of the semiconductor devices with solder.

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Incidentally, a semiconductor device of the TSOP structure is disclosed in Nikkei Maikurodevaisu [pp. 34 to 45, the June issue, 1990] issued by NIKKEI BP.

SUMMARY OF THE INVENTION

The aforementioned semiconductor device of the TSOP structure has the following problems because a plurality of outer leads electrically connected to the external terminals of a semiconductor chip are individually arrayed on the two side faces, opposed to each other, of the package.

(1) When semiconductor devices of the TSOP structure are mounted over the mounting face of the mounting board in the direction perpendicular to one side face of the package, the outer leads, electrically connected to the external terminals of the semiconductor chip, are opposed to each other between the adjoining semiconductor devices. In a memory card, therefore, considering the displacement of the semiconductor devices and the extrusion of the solder at the mounting time, a spacing region is provided between the outer leads of one semiconductor device and the outer leads of the other semiconductor device to prevent the short-circuiting between the adjoining semiconductor devices. However, the spacing region

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has to be formed for every space between semiconductor devices so that the mounting density of the semiconductor devices over the mounting board drops by a value corresponding to the areas of the spacing regions.

(2) When a plurality of semiconductor devices of the TSOP structure are mounted in a direction perpendicular to one side face of the package, between the adjoining semiconductor devices, the outer leads arrayed on one side face of the package of one semiconductor device are present between the outer leads arrayed on the other side face of the package of the one semiconductor device, and the outer leads arranged on the one side face of the package of the other semiconductor device. In short, between the outer leads having the same functions, there are present the outer leads which have different functions. In the memory card, therefore, the wiring existing over the mounting board are routed in a roundabout way to electrically connect the outer leads of the same functions of the individual semiconductor devices. However, such wiring increases the area occupied by the wiring so that the mounting density of the semiconductor devices over the mounting board drops by a value corresponding to the increase in the

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area.

An object of the present invention is to provide a semiconductor device which can be mounting at a high density.

The aforementioned and other objects and novel features of the present invention will become apparent from the following description to be made with reference to the accompanying drawings.

The summary of a representative of the aspects of the invention to be disclosed will be briefly described in the following.

Semiconductor devices mounted on the mounting face of a mounting board have a structure in which each semiconductor chip is encapsulated in a package having a rectangular plane shape, in which a plurality of outer leads electrically connected to external terminals of the semiconductor chip are arrayed on the one side face of the package, and in which a plurality of outer leads not electrically connected to the external terminals of the semiconductor chip are arrayed on the other side face opposed to the one side face of the package.

According to the above-specified means, when these semiconductor devices are mounted on the mounting face of the mounting board and arranged in a

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direction perpendicular to one side face of the package, between the semiconductor devices adjoining in that direction, the outer leads arrayed on one side face of the package of one semiconductor device, and the outer leads arrayed on the other side face of the package of the other semiconductor device are opposed to each other. However, the outer leads of the one semiconductor device are electrically connected to the external terminals of the semiconductor chip, but the outer leads of the other semiconductor device are not electrically connected to the external terminals of the semiconductor chip, so that the outer leads electrically connected to the external terminals of the semiconductor chip are not opposed to each other. As a result, even if the spacing region between the outer leads of the one semiconductor device and the outer leads of the other semiconductor device is reduced or eliminated and if the semiconductor devices are displaced or have extrusion of solder at the packaging time, no short-circuiting takes place between the adjoining ones of the semiconductor devices which are mounted in the direction perpendicular to one side face of the package. As a result, the spacing region between the outer leads of one semiconductor device and the outer leads of the

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other semiconductor device can be reduced or eliminated to mount the semiconductor devices over the mounting board at an accordingly high density.

When semiconductor devices are mounted on the mounting face of the mounting board in a direction perpendicular to one side face of the package, between the adjoining semiconductor devices, there are arranged between the outer leads arrayed on one side face of the package of one semiconductor device, and the outer leads arrayed on one side face of the package of the other semiconductor device, the outer leads which are arrayed on the other side face of the package of the one semiconductor device. However, these outer leads arrayed on the other side face of the package of the one semiconductor device are not electrically connected to the external terminals of the semiconductor chip so that, there are no outer leads between the outer leads of the one semiconductor device and the outer leads of the other semiconductor device having different functions. Without routing the wiring extending over the mounting board in a roundabout way, therefore, it is possible to electrically connect the outer leads of the same functions of the individual semiconductor devices which are mounted in a direction perpendicular to one

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side face of the package. As a result, the wiring region can be reduced or eliminated to mounting the semiconductor devices in an accordingly high density.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a top plan view showing the state that the upper portion of the package of a semiconductor device of Embodiment 1 of the present invention is removed;

Fig. 2 is a section taken along line A-A shown in Fig. 1;

Fig. 3 is a top plan view showing a memory card in which the semiconductor devices are mounted on the mounting face of a mounting board;

Fig. 4 is an enlarged top plan view showing an essential portion of the memory card;

Fig. 5 is a top plan view showing the state that the upper portion of the package of a semiconductor device of Embodiment 2 of the present invention is removed;

Fig. 6 is a top plan view showing a memory card in which the semiconductor devices are mounted on the mounting face of a mounting board;

Fig. 7 is an enlarged top plan view showing an essential portion of the memory card;

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Fig. 8 is a top plan view showing the state that the upper portion of a package of a semiconductor device of Embodiment 3 of the present invention is removed;

Fig. 9 is a top plan view showing the state that upper portion of a package of a semiconductor device of Embodiment 4 of the present invention is removed;

Fig. 10(A) is a section taken along line A-A of Fig. 4;

Fig. 10(B) is a section taken along line B-B of Fig. 4;

Fig. 11 is a perspective view showing an electronic device to which is applied the memory card MC of the present invention;

Fig. 12 is a top plan view showing the memory card MC;

Figs. 13 and 14 are sections taken along lines A-A and B-B of Fig. 12;

Fig. 15 is an external view of a semiconductor device of Embodiment 5 of the present invention;

Fig. 16 is an explanatory view for explaining the names and functions of lead pins of Fig. 15;

Fig. 17 is a top plan block diagram showing a flash memory chip mounted in the semiconductor device of Fig. 15;

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Fig. 18 is a top plan view showing the front side of the memory card of the present invention;

Fig. 19 is a top plan view showing the back side of the memory card of the present invention;

Fig. 20 is a section taken along lines A-A of Figs. 18 and 19; and

Fig. 21 is a block diagram showing the system configuration of a memory card (ATA card) of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The embodiments of the present invention will be described in detail with reference to the accompanying drawings.

Incidentally, throughout all the drawings for illustrating the embodiments of the present invention, the parts and portions having the same functions will be designated by common reference numerals while omitting their repeated description.

(Embodiment 1)

Fig. 1 is a top plan view showing the state that the upper portion of the package of a semiconductor device of Embodiment 1 of the present invention is removed, and Fig. 2 is a section taken along line A-A shown in Fig. 1.

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As shown in Figs. 1 and 2, a semiconductor device 10 of the present embodiment has a TSOP (Thin Small Out-line Package) structure. This semiconductor device 10 has a semiconductor chip 1 mounted on one surface of a tab 4 which is supported by four tab-suspension leads 5. The semiconductor chip 1 is fixed, although not shown, to one surface of the tab 4 through an adhesive layer of Ag paste or the like.

The aforementioned semiconductor chip 1 is constructed mainly of a semiconductor substrate which is a single-crystal silicon substrate having a rectangular plane shape. In the major surface (element forming surface) of the semiconductor substrate, there is constructed a DRAM (Dynamic Random Access Memory) as a memory circuit system, for example. Over the major surface of the semiconductor substrate, moreover, there is formed a multilayer wiring layer in which plural stages of wiring layers and insulating layers are individually stacked.

On one side (one long side) of the major surface of the aforementioned semiconductor chip 1, there are arrayed a plurality of external terminals (bonding pads) BP along the one side. These external terminals BP are individually formed in the uppermost wiring layer of the multilayer wiring and are electrically

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connected to the memory circuit system.

Outside the one side of the semiconductor chip 1, there are arrayed a plurality of inner leads 2A along the one side. These inner leads 2A are individually connected electrically through bonding wires 6 to the external terminals BP which are arrayed on the one side of the major surface of the semiconductor chip 1.

Outside the other side (the other long side) opposed to the one side of the semiconductor chip 1, there are arrayed a plurality of inner leads 2B along the other side. These inner leads 2B are not individually connected electrically to the external terminals BP of the semiconductor chip 1.

The aforementioned semiconductor chip 1, inner leads 2A, inner leads 2B, tabs 4, tab suspension leads 5 and bonding wires 6 are encapsulated in a package 7 so formed as to have a rectangular plane shape. This package 7 is formed by a transfer molding method, for example, although not limited thereto. The transfer molding method is a technique for forming a package with an epoxy resin to which are added a phenol curing agent, silicone rubber and a filler.

On one side face 7A of the aforementioned package 7, there are arranged a plurality of outer leads 3A along the side face. On the other side face 7B

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opposed to the one side face 7A of the package 7, there are also arrayed a plurality of outer leads 3B along the side face. These outer leads 3A and 3B are individually formed into a gull-wing shape.

The aforementioned outer leads 3A are individually integrated with the inner leads 2A which are arrayed outside the one side of the semiconductor chip 1. Moreover, the aforementioned outer leads 3B are individually integrated with the inner leads 2B which are arrayed outside the other side of the semiconductor chip 1. In short, the semiconductor device 10 of the present embodiment is constructed of the bidirectional lead array structure in which the outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on and along the one side face 7A of the package 7 whereas the outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arranged at and along the other side face 7B opposed to the one side face of the package 7.

The aforementioned outer leads 3A, outer leads 3B and tab suspension leads 5 are individually integrated with the lead frame at a step of manufacturing the semiconductor device. These outer leads 3A and 3B and tab suspension leads 5 are individually cut from the

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lead frame after the inner leads 2A and 2B, the tabs 4, the tab suspension leads 5 and the bonding wires 6 are encapsulated in the package 7. After this, the outer leads 3A and 3B are individually formed into the gull-wing shape. Incidentally, the lead frame is made of a Cu alloy or an Fe-Ni (having 42 or 50 [%] of Ni content, for example) alloy, for example.

To the aforementioned outer leads 3A and outer leads 3B, there are applied an address signal, a row-address strobe signal, a column-address strobe signal, an output enable signal, a write enable signal and a data input/output signal.

A plurality of semiconductor devices 10 thus constructed are regularly arranged as one memory system, as shown in Fig. 11, on a mounting board of a memory card (an electronic unit) MC which is additionally connected to an electronic device PC such as a personal computer or an office computer. This mounting is usually carried out by applying pasty solder by a screen printing method to the electrode pads (the land regions of the wiring) which are arranged on the mounting face of the mounting board, and by fixing the electrode pads of the mounting board and the outer leads of the semiconductor device 10 with solder.

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The electronic device PC is equipped with a liquid crystal display 16, a keyboard 17, a control pad 18, and a slot 19 for receiving the memory card MC.

When the connector side 20 of the memory card MC is inserted into the slot 19, data such as graphic data are transferred between the electronic device PC and the memory card MC.

This memory card MC is formed, as shown in Figs. 12, 13 and 14, into a hollow structure having a generally rectangular plate shape, for example, by sandwiching an outer frame 15 of plastic between covers 14 of stainless steel. In this structure, there is arranged the mounting board 11, one edge of which is fixed to the outer frame 15. The body of the memory card MC is constructed by mounting a plurality of semiconductor devices, as will be described with reference to Figs. 3 and 4, on the mounting board 11.

In the aforementioned memory card (electronic unit), as shown in Fig. 3 (a top plan view), a plurality of semiconductor devices 10 are directionally arranged and mounted in a matrix shape on the mounting face of a mounting board 11. In order to recognize the mounting direction of the individual semiconductor devices 10, marks 22 are made on the

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surface of the package 7. Incidentally, reference numeral 21 designates connector terminals for connection with the electronic device PC. Of these semiconductor devices 10, the semiconductor devices 10 mounted in the direction (Y-direction) perpendicular to the one side face 7A of the package 7, are shown in Fig. 4 (an enlarged top plan view of an essential portion of Fig. 3). Between two adjoining semiconductor devices 10, the outer leads 3A arrayed on the one side face 7A of the package 7 of one semiconductor device 10, and the outer leads 3B arrayed on the other side face 7B of the package 7 of the other semiconductor device 10 are opposed to each other. However, the outer leads 3A of the one semiconductor device 10 are electrically connected to the external terminals BP of the same semiconductor device 10, but the outer leads 3B of the other semiconductor device 10 are not electrically connected to the external terminals BP of the same semiconductor chip 1, so that the outer leads 3A electrically connected to the external terminals BP of the semiconductor chips 1 are not opposed to each other. As a result, even if the spacing region between the outer leads 3A of the one semiconductor device 10 and the outer leads 3B of the other semiconductor device

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10 is reduced or eliminated and if the semiconductor devices 10 are displaced or extrusion of the solder occurs at the mounting time, no short-circuiting takes place between adjoining semiconductor devices 10 which are mounted in the direction perpendicular to the one side face 7A of the package 7. In other words, in order to electrically isolate the adjoining leads 3A and 3B between the adjoining semiconductor devices 10, lands 13 (foot prints) formed on the mounting board 11 are arranged, considering predetermined spacings (the positioning allowance of the leads and the extrusion width of solder). In the case of the present embodiment, as shown in Fig. 10(A) and 10(B), the adjoining lands 13 of the wiring 12 can be formed with spacings less than the aforementioned predetermined spacings or integrated with no spacing. Moreover, the wiring 12 can be generally linearly formed below the package 7 to improve the mounting efficiency.

Between the adjoining ones of the semiconductor devices 10 mounted in the direction (Y-direction) perpendicular to the one side face 7A of the package 7, the outer leads 3B arrayed on the other side face 7B of the package 7 of one semiconductor device 10 are provided between the outer leads 3A arrayed one the one side face 7A of the package 7 of the one semi-

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conductor device 10, and the outer leads 3A arrayed on the on side face 7A of the package 7 of the other semiconductor device 10. However, the outer leads 3B arrayed on the other side face 7B of the package 7 of the one semiconductor device 10 are not electrically connected to the external terminals BP of the same semiconductor chip 1, so that there is no such outer leads between the outer leads 3A of the one semiconductor device 10 and the outer leads 3A of the other semiconductor device 10 having functions different from those of the outer leads 3A. As a result, for the leads such as chip select leads 3A (CS) which must be electrically independent, roundabout routed wiring 12A is required. For the other common signal leads or power supply leads, however without roundabout routing of the wiring 12 extending over the mounting board 11, it is possible to electrically connect the outer leads 3A of the same functions of the individual semiconductor devices 10 mounted in the direction perpendicular to the one side face 7A of the package 7, through the generally straight wiring 12.

Thus, the following effects can be achieved in the present embodiment.

(1) Semiconductor devices 10 mounted on the mounting

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face of the mounting board 11 has a structure in which the semiconductor chip 1 is packaged in a package 7 having a rectangular plane shape, a plurality of outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed along the one side face of the package 7, and a plurality of outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed along the other side face 7B opposed to the one side face 7A of the package 7. When these semiconductor devices 10 are mounted on the mounting face of the mounting board 11 and arranged in a direction perpendicular to the one side face 7A of the package 7, between the semiconductor devices 10 adjoining in the direction, the outer leads 3A arrayed on the one side face 7A of the package 7 of the one semiconductor device 10, and the outer leads 3B arrayed on the other side face 7B of the package 7 of the other semiconductor device 10 are opposed to each other. However, the outer leads 3A of the one semiconductor device 10 are electrically connected to the external terminals BP of the semiconductor chip 1, but the outer leads 3B of the other semiconductor device 10 are not electrically connected to the external terminals BP of the semiconductor chip 1, so

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that the outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are not opposed to each other. As a result, even if the spacing region between the outer leads 3A of the one semiconductor device 10 and the outer leads 3B of the other semiconductor device 10 is reduced or eliminated and if the semiconductor devices 10 are displaced or extrusion of the solder occurs at the mounting time, no short-circuit takes place between the adjoining ones of the semiconductor devices 10 which are mounted in the direction perpendicular to the one side face 7A of the package 7. As a result, the spacing region between the outer leads 3A of the one semiconductor device 10 and the outer leads 3B of the other semiconductor device 10 can be reduced or eliminated to mount the semiconductor devices 10 on the mounting board 11 in an accordingly high density.

Moreover, when the semiconductor devices 10 are arranged in the direction perpendicular to the one side face 7A of the package 7 and mounted on the mounting face of the mounting board 11, between the semiconductor devices 10 adjoining in that direction, the outer leads 3B arrayed on the other side face 7B of the package 7 of one semiconductor device 10 are present between the outer leads 3A arrayed one the one

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side face 7A of the package 7 of the one semiconductor device 10, and the outer leads 3A arrayed on the on side face 7A of the package 7 of the other semiconductor device 10. However, the outer leads 3B arrayed on the other side face 7B of the package 7 of the one semiconductor device 10 are not electrically connected to the external terminals BP of the same semiconductor chip 1, so that there is not present such outer leads between the outer leads 3A of the one semiconductor device 10 and the outer leads 3A of the other semiconductor device 10 having functions different from those of the outer leads 3A. As a result, without roundabout routing of the wiring 12 extending in the Y-direction on the mounting board 11, it is possible to electrically connect the outer leads 3A of the same functions of the individual semiconductor devices 10 mounted in the direction perpendicular to the one side face 7A of the package 7. As a result, the wiring region can be reduced or eliminated to mount the semiconductor devices 10 at an accordingly high density on the mounting board 11.

By the outer leads 3A arranged on the one side face 7A of the package 7 and the outer leads 3B arrayed on the other side face 7B of the package 7, moreover, the semiconductor devices 10 can be stably

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fixed to the mounting board 11 thereby to enhance the shock resistance of the semiconductor devices 10.

(2) In the memory card (electronic unit), a plurality of semiconductor devices 10 each having a structure in which a semiconductor chip 1 is encapsulated in a package 7 having a rectangular plane shape, a plurality of outer leads 3A, as electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the one side face of the package 7, and a plurality of outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the other side face 7B opposed to the one side face 7A of the package 7 are mounted on the mounting face of the mounting board 11 in the direction perpendicular to the one side face 7A of the package 7. Between the adjoining semiconductor devices 10, therefore, the spacing region between the outer leads 3A of the one semiconductor device 10 and the outer leads 3B of the other semiconductor device 10 can be reduced or eliminated to reduce the plane size of the memory card correspondingly. Without roundabout routing of the wiring 12 extending on the mounting board 11, moreover, the outer leads 3A of the same functions of the individual semiconductor devices 10 arranged in

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the direction perpendicular to the one side face 7A of the package 7 can be electrically connected. As a result, the area of the wiring 12 can be reduced or eliminated to reduce the plane size of the memory card correspondingly.

(Embodiment 2)

Fig. 5 is a top plan view showing the state that the upper portion of the package of a semiconductor device of Embodiment 22 of the present invention is removed.

As shown in Fig. 5, a semiconductor device 10 of the present embodiment is constructed of a TSOP structure. In this semiconductor device 10 of the TSOP structure, a semiconductor chip 1 is mounted on one surface of a tab 4 which is supported by four tab suspension leads 5.

A plurality of inner leads 2A are arrayed outside and along one side of the semiconductor chip 1. These individual inner leads 2A are electrically connected through bonding wires 6 to external terminals BP which are arrayed on the one side of the major surface of the semiconductor chip 1.

A plurality of inner leads 2B are arrayed outside and the other side (the other long side) opposed to the one side of the semiconductor chip 1. These

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individual inner leads 2B are not electrically connected to the external terminals BP of the semiconductor chip 1.

Outside and along one of the two sides perpendicular to the one side of the semiconductor chip 1, there are arrayed a plurality of inner leads 2C. These individual inner leads 2C are electrically connected through bonding wires 6 to a plurality of external terminals BP which are arrayed on one of the two sides perpendicular to the one side of the major surface of the semiconductor chip 1.

The aforementioned semiconductor chip 1, inner leads 2A, inner leads 2B, inner leads 2C, tab 4, tab suspension leads 5 and bonding wires 6 are encapsulated in a package 7 which is so formed as to have a rectangular plane shape.

A plurality of outer leads 3A are arrayed on one side face 7A of the package 7. A plurality of outer leads 3B are arrayed on the other side face 7B opposed to the one side face 7A of the package 7. A plurality of outer leads 3s 3C are arrayed on one 7C of the two side faces perpendicular to the one side face of the package 7. These outer leads 3A, 3B and 3C are formed into a gull-wing shape.

The outer leads 3A are individually integrated

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with the inner leads 2A which are arrayed outside the one side of the semiconductor chip 1. Moreover, the outer leads 3B are individually integrated with the inner leads 2B which are arrayed outside the other side of the semiconductor chip 1. Moreover, the outer leads 3C are individually integrated with the inner leads 2C which are arrayed outside one of the two sides perpendicular to the one side of the semiconductor chip 1. In other words, the semiconductor device 10 of the present embodiment has a three-way lead array structure in which the outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the one side face 7A of the package 7, the outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1, are arrayed on the other side face 7B opposed to the one side face 7A of the package 7, and the outer leads 3C electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the one side face 7C of the two side faces perpendicular to the one side face 7A of the package 7.

A plurality of semiconductor devices 10 thus constructed are regularly arranged on the mounting board of the memory card (electronic unit) which is

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additionally connected to the electronic device such as a personal computer or an office computer.

In the aforementioned memory card (electronic unit), as shown in Fig. 6 (a top plan view), the semiconductor devices 10 are mounted in a matrix shape in the arrangement direction on the mounting face of the mounting board 11. Of these semiconductor devices 10, the semiconductor devices 10 mounting in the same direction (X-direction) as that of the one side face 7A of the package 7 are constructed, as shown in Fig. 7 (an enlarged top plan view of an essential portion of Fig. 6), such that the outer leads 3C arrayed on the side face 7C of the package 7 of the one semiconductor device 10, and the outer leads 3C arrayed on the side face 7C of the package 7 of the other semiconductor device 10 are not opposed to each other. As a result, when the one semiconductor device 10 and the other semiconductor device 10 are mounted in a packed state and even if they are displaced or extrusion of the solder occurs at the mounting time, no short-circuit takes place between the adjoining ones of the semiconductor devices 10 which are mounted in the direction perpendicular to the one side face 7A of the package 7. As a result, the semiconductor devices 10 can be mounted in the packed state in the

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same direction as that of the one side face 7A of the package 7 thereby to mounting them at an accordingly high density.

Of the semiconductor devices 10 mounted in the same direction (the X-direction in the drawing) as that of the one side face 7A of the package 7, moreover, between the adjoining semiconductor devices 10, there are no such other outer leads between the outer leads 3C arrayed on the side face 7C of the package 7 of the one semiconductor device 10, and the outer leads 3C arrayed on the side face 7C of the package 7 of the other semiconductor device 10 having functions different from those of the outer leads 3C. Without roundabout routing of the wiring (not-shown) extending in the X-direction inside the mounting board, therefore, it is possible to electrically connect the outer leads 3C of the same functions of the individual semiconductor devices 10 which are mounted in the same direction as that of the one side face 7A of the package 7. As a result, the wiring region of the wiring extending in the X-direction can be reduced or eliminated to mount the semiconductor devices 10 at an accordingly high density. In other words, the area where the wiring is routed in a roundabout way can be reduced to the minimum by

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linearly connecting the outer leads 3A of the semiconductor devices 10 adjoining each other in the Y-direction to each other through the surface wiring layer 12 of the mounting board and by linearly connecting the outer leads 3C of the semiconductor devices 10 adjoining each other in the X-direction to each other through only one specific layer of the internal wiring of the mounting board.

(Embodiment 3)

Fig. 8 is a top plan view showing the state that the upper portion of the package of a semiconductor device of Embodiment Mode is removed.

As shown in Fig. 8, the semiconductor device 10 of the present embodiment is constructed of a two-way lead array structure in which a semiconductor chip 1 is encapsulated in a package 7 having a rectangular plane shape, in which a plurality of outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on a part of the one side face 7A of the package 7 and along the one side face, a plurality of outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the other region of the one side face 7A of the package 7 and along the one side face, in which a plurality of outer

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leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on a part of the other side face 7B opposed to the partial region of the one side face 7A of the package 7 and along the other side face, and a plurality of outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the other region of the other side face 7B opposed to the other region of the one side face 7A of the package 7 and along the other side face.

When the semiconductor devices 10 thus constructed are mounted in plurality in a matrix shape in a direction on the mounting face of the mounting board, between the adjoining ones 10 of the semiconductor devices 10 mounted in the direction perpendicular to the one side face 7A of the package 7, like Embodiment 1, the outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are not opposed to each other. Between the adjoining ones 10 of the semiconductor devices 10 mounted in the direction perpendicular to the one side face 7A of the package 7, moreover, there are no such outer leads between the outer leads 3A of the one semiconductor device 10 and the outer leads 3A of the other semiconductor device 10 having functions

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different from those of the outer leads 3A. As a result, like Embodiment 1, the semiconductor devices 10 can be mounted at a high density.

(Embodiment 4)

Fig. 9 is a top plan view showing the state that the upper portion of the package of a semiconductor device of Embodiment 4 is removed.

As shown in Fig. 9, the semiconductor device 10 of Embodiment 4 is constructed of a three-way lead array structure in which a semiconductor chip 1 is encapsulated in a package 7 having a rectangular plane shape, in which a plurality of outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on a part of the one side face 7A of the package 7 and along the one side face, a plurality of outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on the other part of the one side face 7A of the package 7 and along the one side face, a plurality of outer leads 3B not electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed on a part of the other side face 7B opposed to a part of the one side face 7A of the package 7 and along the other side face, a plurality of outer leads 3A electrically

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connected to the external terminals BP of the semiconductor chip 1 are arrayed on the other part of the other side face 7B opposed to the other part of the one side face 7A of the package 7 and along the other side face, and a plurality of outer leads 3C electrically connected to the external terminals BP of the semiconductor chip 1 are arrayed along one side face 7C of the two side faces perpendicular to the one side face 7A of the package 7.

When the semiconductor devices 10 thus constructed are mounted in plurality in a matrix shape in a direction on the mounting face of the mounting board, between the adjoining ones 10 of the semiconductor devices 10 mounted in the same direction as that of the one side face 7A of the package 7, like the foregoing Embodiment Mode 2, the outer leads 3A electrically connected to the external terminals BP of the semiconductor chip 1 are not opposed to each other. As a result, like Embodiment 1, the semiconductor devices 10 can be mounted at a high density.

(Embodiment 5)

Fig. 15 is a top plan view showing a semiconductor device (package) of Embodiment 5.

A semiconductor device 100 is constructed, as in

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Embodiment 1, of a TSOP structure, and a semiconductor chip 23 mounted with a flash memory (EEPROM) shown in Fig. 17 is encapsulated in a package 7. Over the major surface of the semiconductor chip 23, there are formed four memory arrays MA each having a plurality of memory cells arranged in a matrix shape, word decoders WD, column decoders CD and sense amplifiers SA for selecting a predetermined memory cell from each memory array MA, a power supply circuit VC having a power voltage generator and a booster circuit, a control circuit CC serving as an interface with an external device such as an input/output circuit. Moreover, the bonding pads BP are arranged along only one long side of the semiconductor chip 23, and the peripheral circuits including the power supply circuit VC and the control circuit CC are positively arranged in the vicinities of the bonding pads BP to equalize the signal wiring lengths in the chip and to reduce the chip size. The individual bonding pads BP correspond to power supply pins and signal pins Vcc, Vss, I/O and so on, as shown in Figs. 15 and 16, and are connected through the wires 6 to the inner leads 2A of the corresponding power supply pins and signal pins. The individual pin functions are shown in Fig. 16, and the NC pins (3B) are in an electrically

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floating state in the package.

The aforementioned semiconductor devices 100 are mounted on the mounting board 11, as shown in Figs. 18 and 19, constituting the body of the memory card. Fig. 18 is a top plan view showing the front side of the mounting board 11, and Fig. 19 is a top plan view showing the back side, opposed to the surface side, of the mounting board 11. Fig. 20 is a section taken along lines A-A of Figs. 18 and 19.

On the back side of the mounting board 11, there are mounted a QFP package GA mounted with a gate array chip, a QFP package MPU mounted with microcomputer, and a TSOP package DM mounted with a DRAM chip. On the mounting board 11, moreover, there are mounted a chip capacitor C and a chip resistor R for matching the impedance, and a clock generator GE for feeding clock signals.

The packages thus mounted on the mounting board 11 constitutes an ATA (AT Attachment) card 24, as shown in Fig. 21. Here will be briefly described the system configuration of the ATA card 24.

The ATA (AT Attachment) card 24 of Fig. 21 conforms to the interface and protocol which are used when an AT compatible machine makes an access to a hard disk and is standardized by the PCMCIA (Personal

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Computer Memory Card International Association).

Numeral 25 designates a pin connector section of the ATA card, corresponding to the external terminals 21, through which signals are exchanged with a PC (Personal Computer) or a PDA (Personal Digital Assistant). The number, names and Nos. of the external terminals are determined by the PCMCIA.

The data and addresses from the outside are introduced at first through signal lines 26 into the gate array GA. This gate array GA controls the PCMCIA interface (PCIN), the microcomputer MPU, the DRAM (Dynamic Random Access Memory), the flash memory 100, and the data transfer between the flash memory 100 and the PCMCIA interface. The exchanges of the data and addresses between the individual elements in the card are executed through the local data bus and the local address bus designated by numeral 27.

The MPU controls the data according to commands from the outside. The data from the outside are fed through the DRAM to the flash memory 100 or from the flash member 100 to the DRAM so that they may be processed, i.e., written in or read out at high rate. Moreover, the MPU controlles through a CE (Chip Enable) bus 28 which flash memory 100 data are to be written in or read out. In order to improve the

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reliability of the data stored in the flash memory 100, moreover, the MPU controls the ECC (Error Check Correction) processing (control of the number of rewrites of the individual sectors, control of the access to defective sectors) and the ware leveling (averaging the number of rewrites of the individual sectors).

Although the invention made by us has been specifically described, taking the case of Embodiments, it should not be limited thereto but can naturally be modified in various manners without departing from the gist thereof.

For example, the present invention can be applied to a semiconductor device in which the semiconductor chip is encased in a package made of ceramic.

Moreover, the present invention can be applied to a semiconductor device having an LOC (Load On Chip) structure or a COL (Chip On Lead) structure.

Moreover, the present invention can be applied to a semiconductor device in which is mounted a semiconductor chip constructed of a memory circuit system made up of a SRAM (Static Random Access Memory), an EPROM (Electrically Programmable Read Only Memory), an EEPROM (Electrically Erasable Programmable ROM) and a flash memory (flash EEPROM).

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WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

(1) a generally rectangular semiconductor chip having a plurality of bonding pads and a plurality of semiconductor elements over its major surface,

said semiconductor chip having a pair of long sides extending in a first direction and a pair of short sides extending in a second direction generally perpendicular to said first direction, and

said bonding pads being arranged along one of said pair of long sides;

(2) a plurality of first leads arranged outside said semiconductor chip and along the one of said pair of long sides,

said first leads individually including inner lead portions and outer leads, and the leading end portions of said inner lead portions being electrically connected to the corresponding bonding pads by bonding wires;

(3) a plurality of second leads arranged outside said semiconductor chip and along the other of said paired long sides,

said second leads individually including inner lead portions and outer leads, and

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said second leads being not electrically connected to said semiconductor chip; and

(4) a package in which said semiconductor chip, the inner lead portions of said first leads, the inner lead portions of said second leads, and said bonding wires are packaged,

said package being formed into a generally rectangular shape having a pair of long sides extending in said first direction and a pair of short sides extending in said second direction,

wherein the outer leads of said first leads protrude from one of the paired long sides of said package whereas the outer leads of said second leads protrude from the other of said paired long sides, and wherein the outer leads of said first leads and the outer leads of said first leads arranged in positions opposed to each other are electrically connected outside said package.

2. A semiconductor device according to claim 1, wherein the outer leads of said first leads and the outer leads of said second leads protrude from said package in parallel with said second direction, and the outer leads of said opposed first and second leads are arranged generally linearly in said second

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direction.

3. A semiconductor device according to claim 1, wherein said opposed first and second leads are connected through wiring outside said package.

4. A semiconductor device according to claim 1, wherein said semiconductor chip includes a memory array formed on its major surface, and an input/output circuit arranged between said memory array and said bonding pads.

5. A semiconductor device comprising:

(a) a mounting board having a plurality of wirings on its major surface; and

(c) a plurality of semiconductor packages mounted on the major surface of said mounting board,

each of said semiconductor packages including:

(1) a generally rectangular semiconductor chip having a plurality of bonding pads and a plurality of semiconductor elements on its major surface,

said semiconductor chip having a pair of long sides extending in a first direction and a pair of short sides extending in a second direction generally perpendicular to said first direction, and

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said bonding pads being arranged along one of said pair of longer sides;

(2) a plurality of first leads arranged outside said semiconductor chip and along the one of said pair of long sides,

said first leads individually including inner lead portions and outer leads, and the leading end portions of said inner lead portions being electrically connected to the corresponding bonding pads by bonding wires;

(3) a plurality of second leads arranged outside said semiconductor chip and along the other of said paired long sides,

said second leads individually including inner lead portions and outer leads, and said second leads being not electrically connected to said semiconductor chip; and

(4) a package in which said semiconductor chip, the inner lead portions of said first leads, the inner lead portions of said second leads, and said bonding wires are packaged,

said package being formed into a generally rectangular shape having a pair of long sides extending in said first direction and a pair of short sides extending in said second direction,

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the outer leads of said first leads protruding from one of the pair of long sides of said package, and

the outer leads of said second leads protruding from the other of said pair of long sides,

wherein said semiconductor packages are so arranged at predetermined spacings in said second direction that the first leads and the second leads of the adjoining semiconductor packages are opposed to each other, and wherein the leading ends of the outer leads of the first leads and the second leads of said adjoining semiconductor packages are connected through the wiring which is formed on the major surface of said mounting board.

6. A semiconductor device according to claim 5, wherein the leading end portions of the first leads of said adjoining semiconductor packages are arranged on first land portions of said wiring whereas the leading end portions of the second leads of said adjoining semiconductor packages are arranged on second land portions of said wiring, and wherein the spacing between said first land portions and said second land portions is narrower than the spacing between said outer leads.

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7. A semiconductor device according to claim 5, wherein the leading end portions of the first leads of said adjoining semiconductor packages are arranged on first land portions of said wiring whereas the leading end portions of the second leads of said adjoining semiconductor packages are arranged on second land portions of said wiring, and wherein said first land portions and said second land portions are integrally formed.

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SEMICONDUCTOR DEVICE

ABSTRACT OF THE DISCLOSURE

Disclosed are a resin-encapsulated semiconductor package and a packaging structure, suited for a high density mounting. Specifically, outer leads are protruded from the two long sides of a rectangular package. The inner leads in the package, connected to the outer leads protruding from one long side, are connected through wires to the bonding pads of a semiconductor chip encapsulated in the package, whereas the inner leads in the package, connected to the outer leads protruding from the other long side, are in an electrically floating state in the package. The semiconductor packages are arranged in a direction on a card-shaped mounting board, and the opposed outer leads of adjoining semiconductor packages are electrically connected by wiring on the mounting board. The wiring is so laid below the semiconductor packages that they extend generally linearly.

Figure 1

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FIG. 1

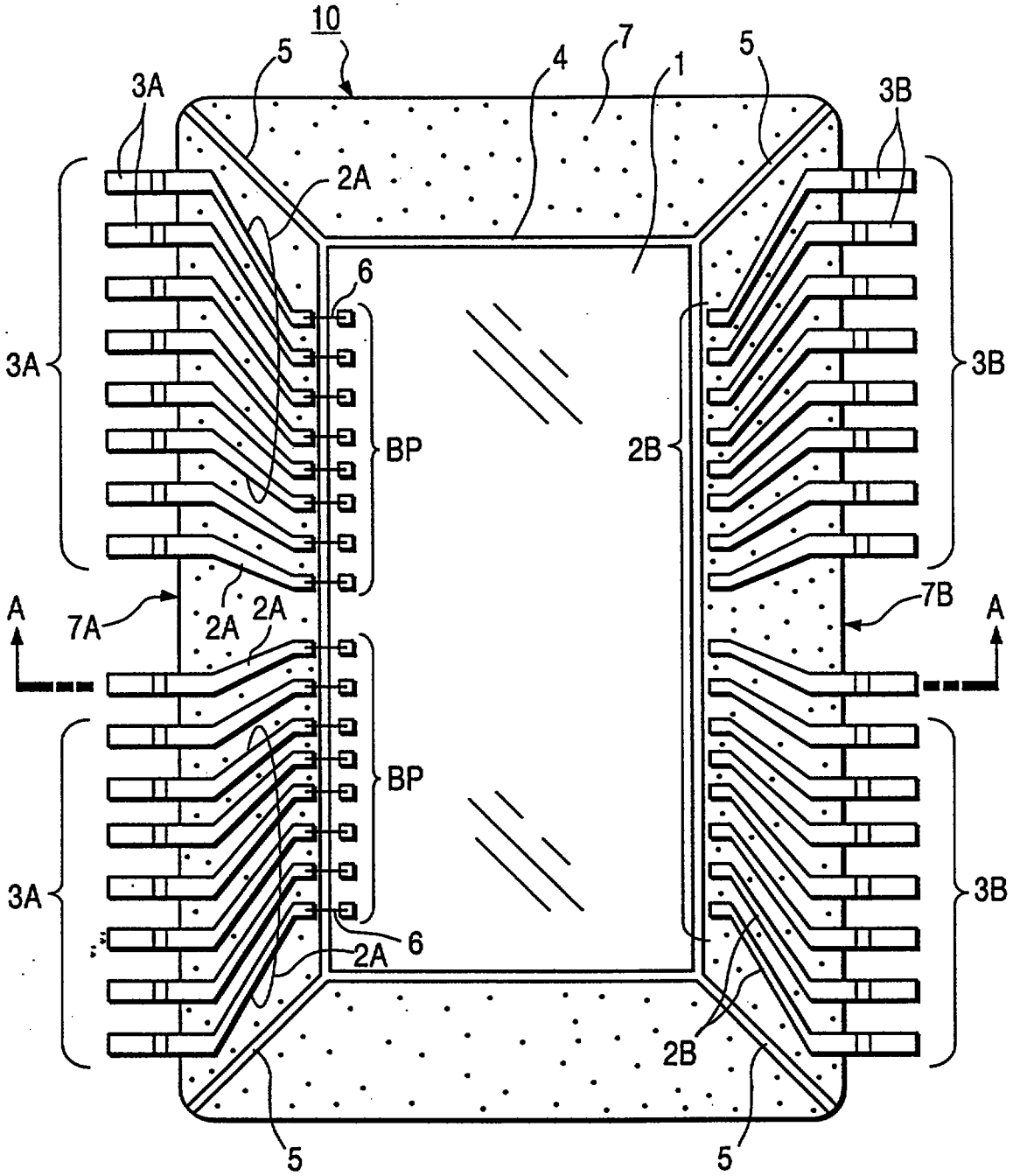
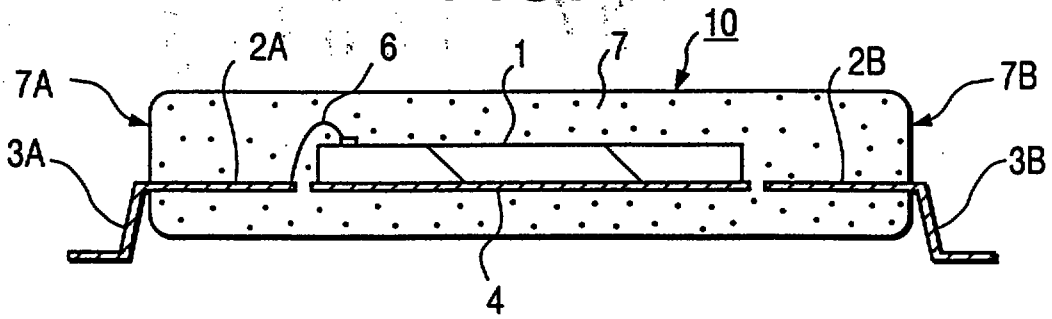
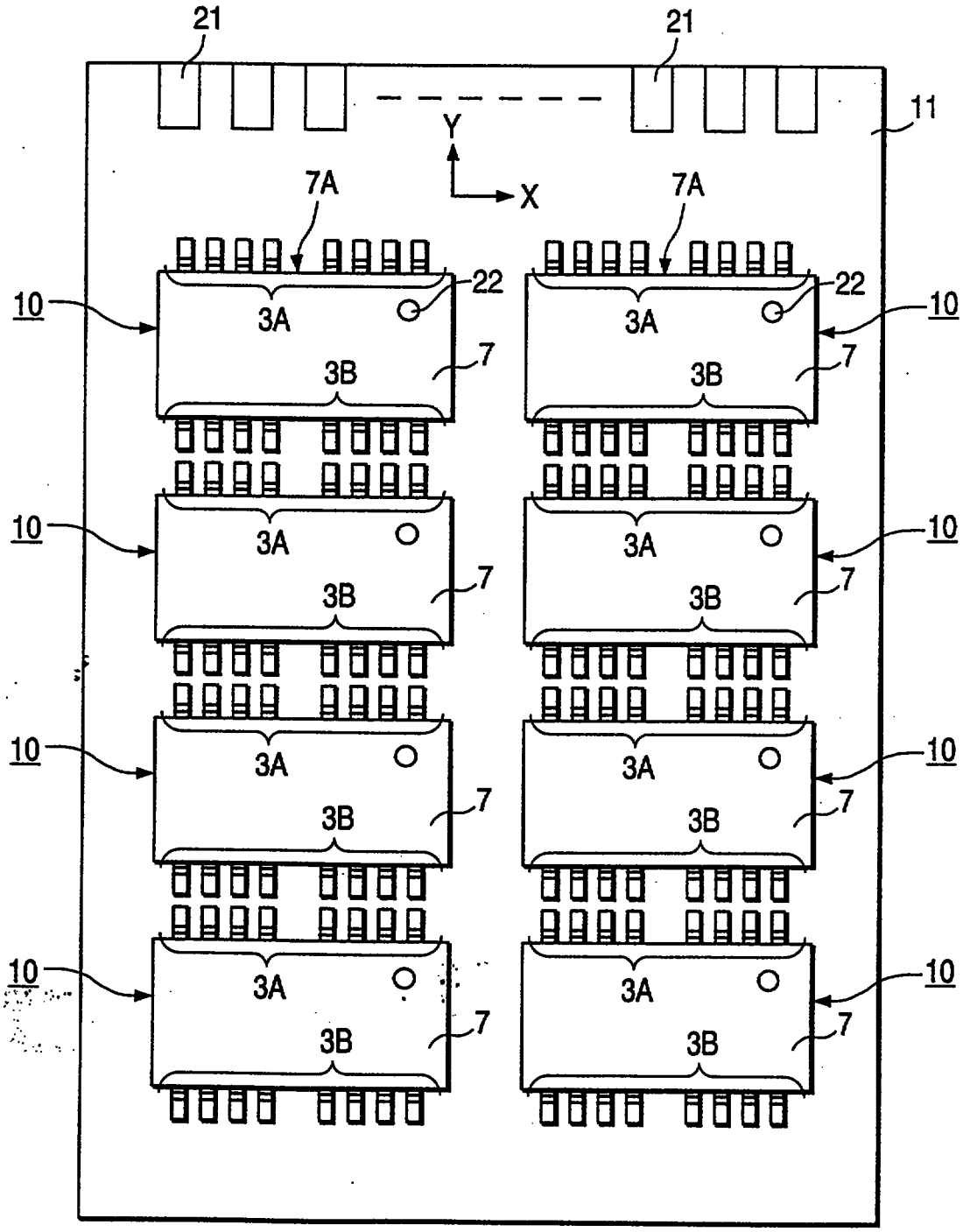


FIG. 2



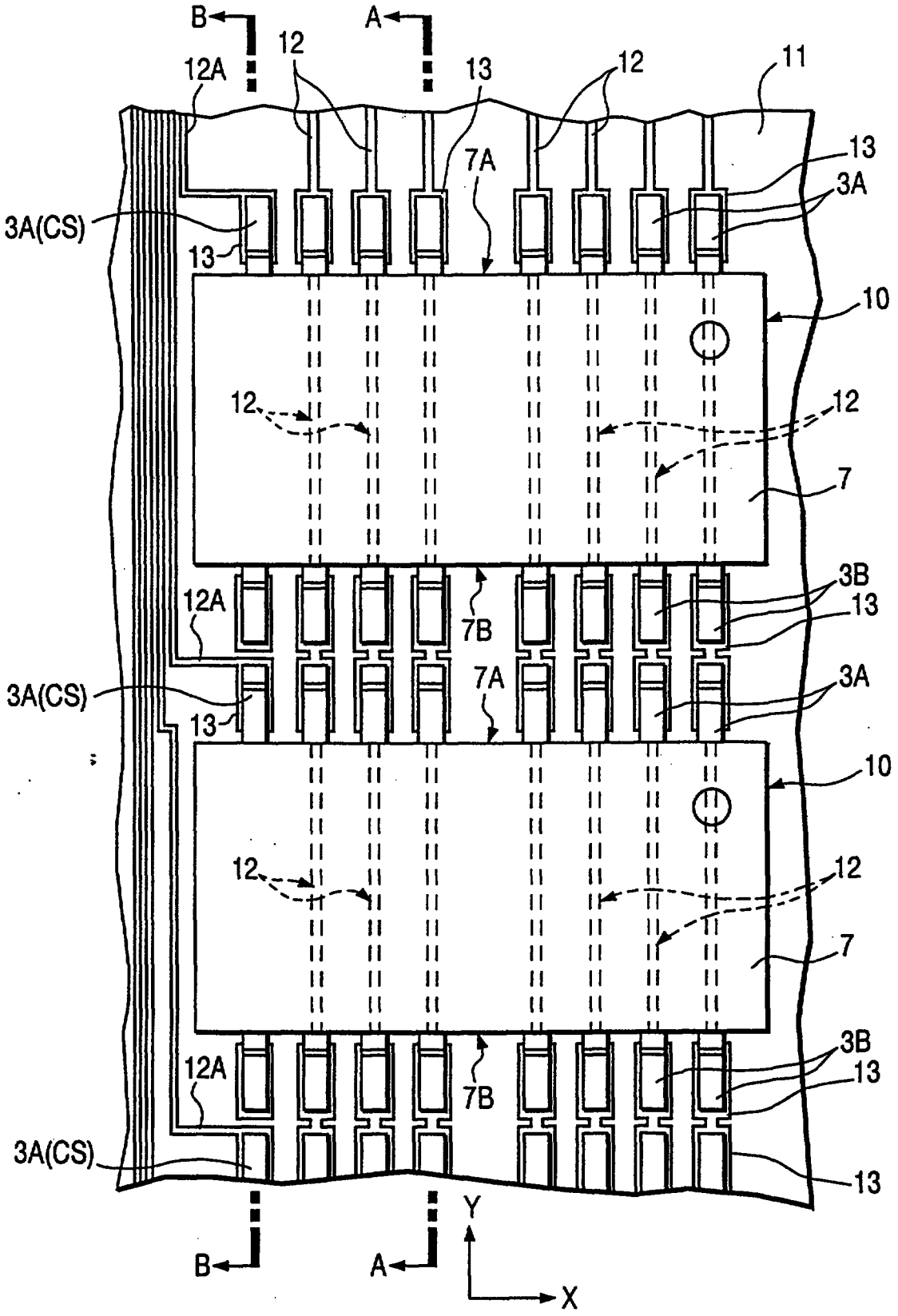
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FIG. 3



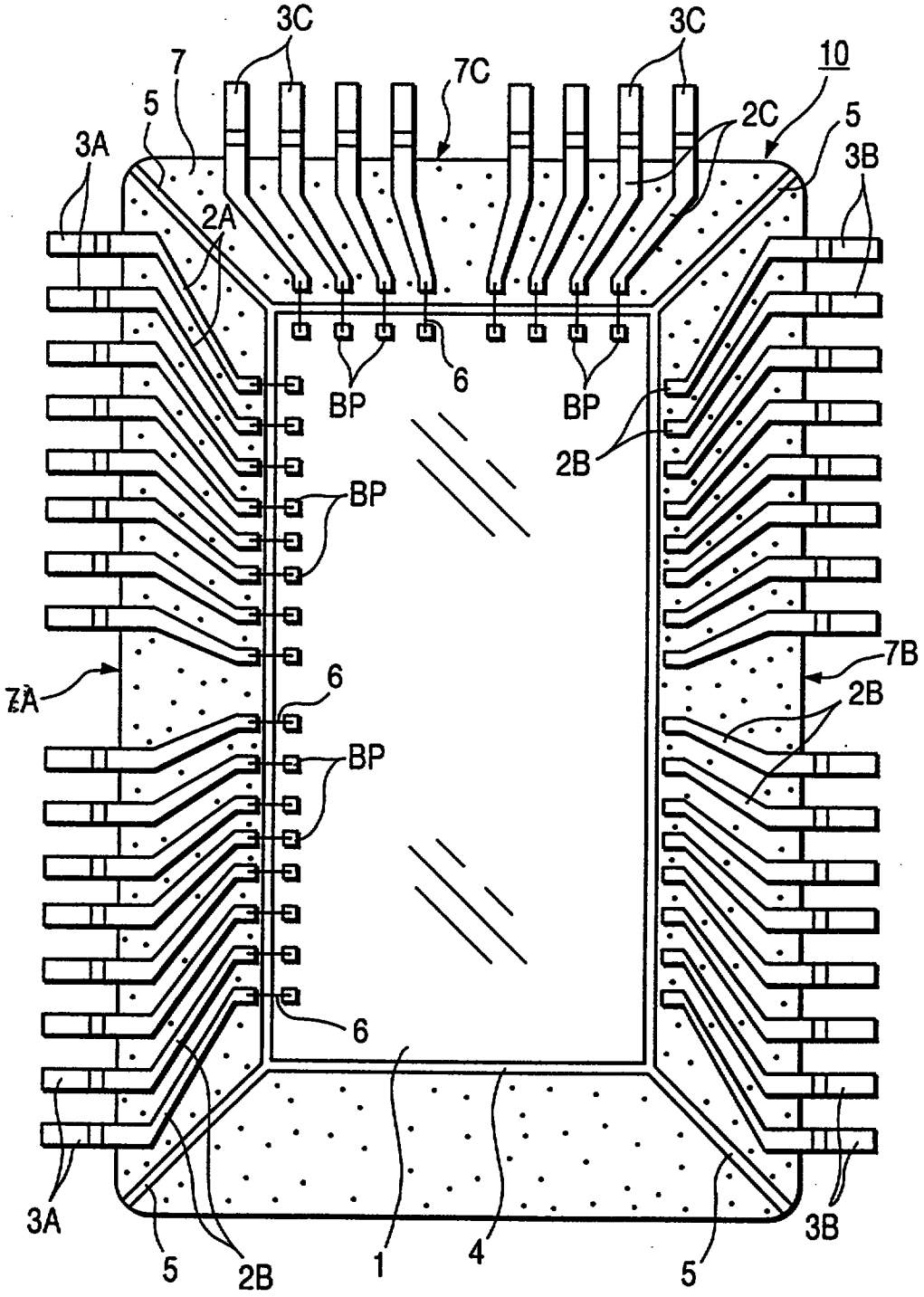
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FIG. 4



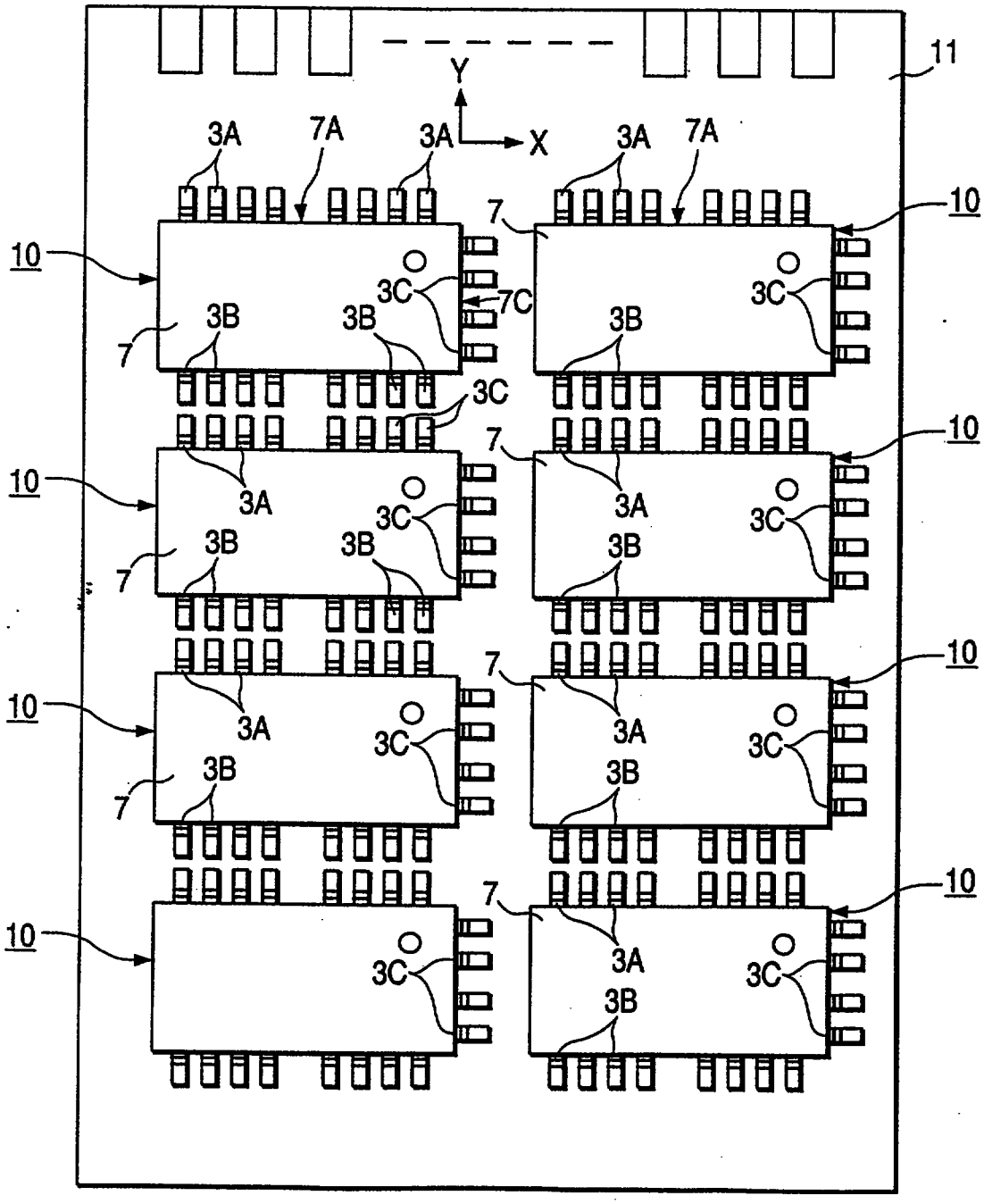
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FIG. 5



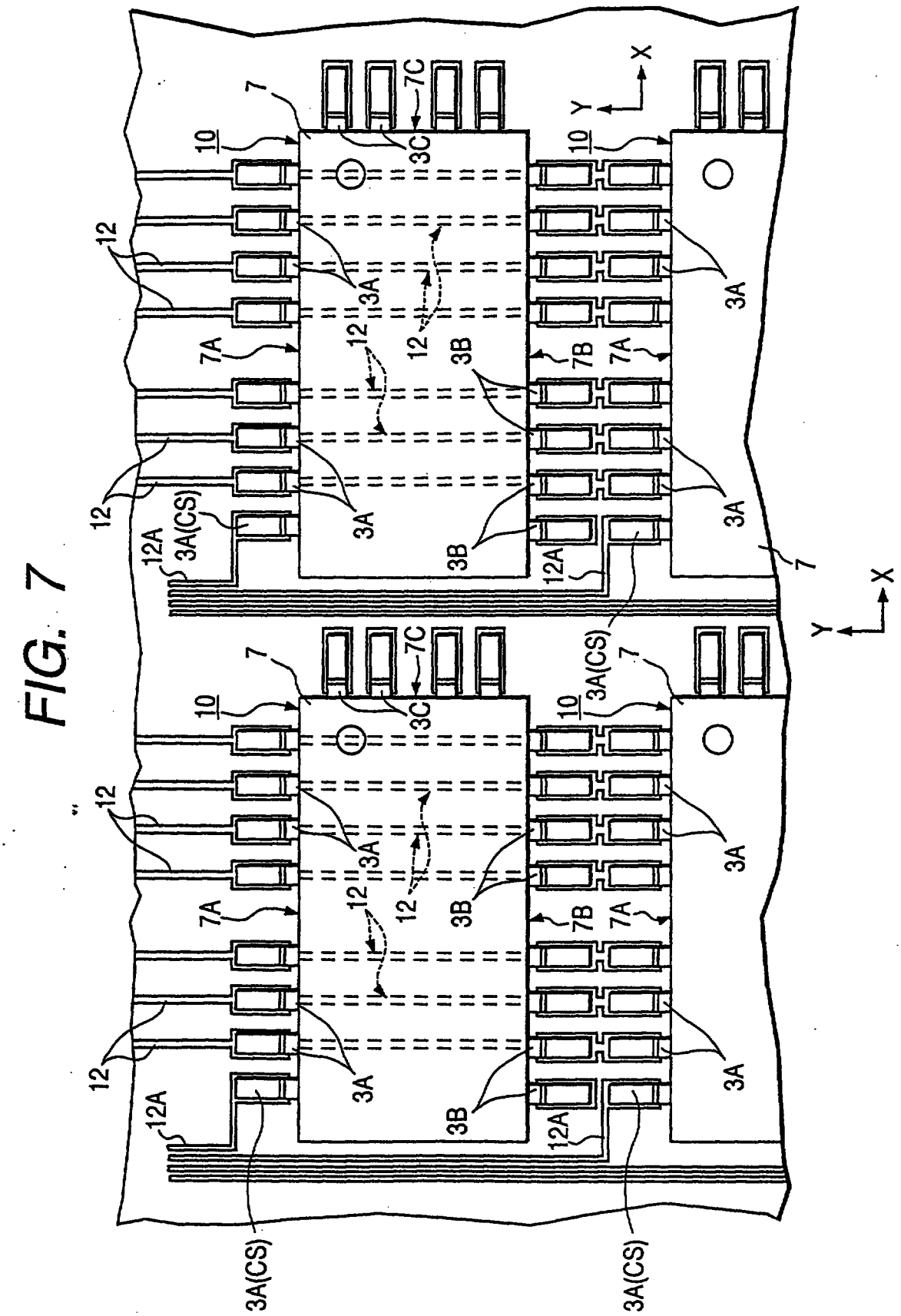
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FIG. 6



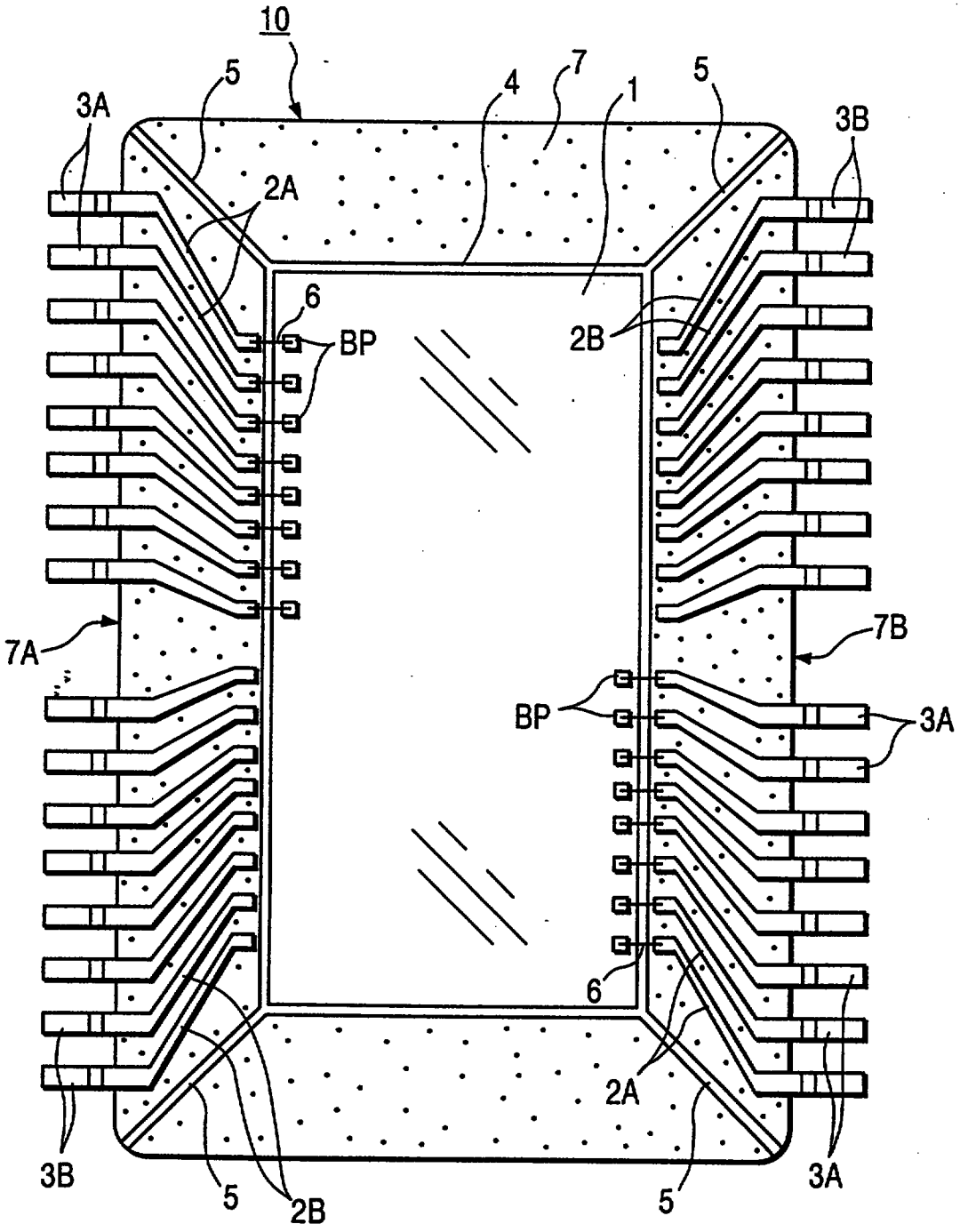
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FIG. 7



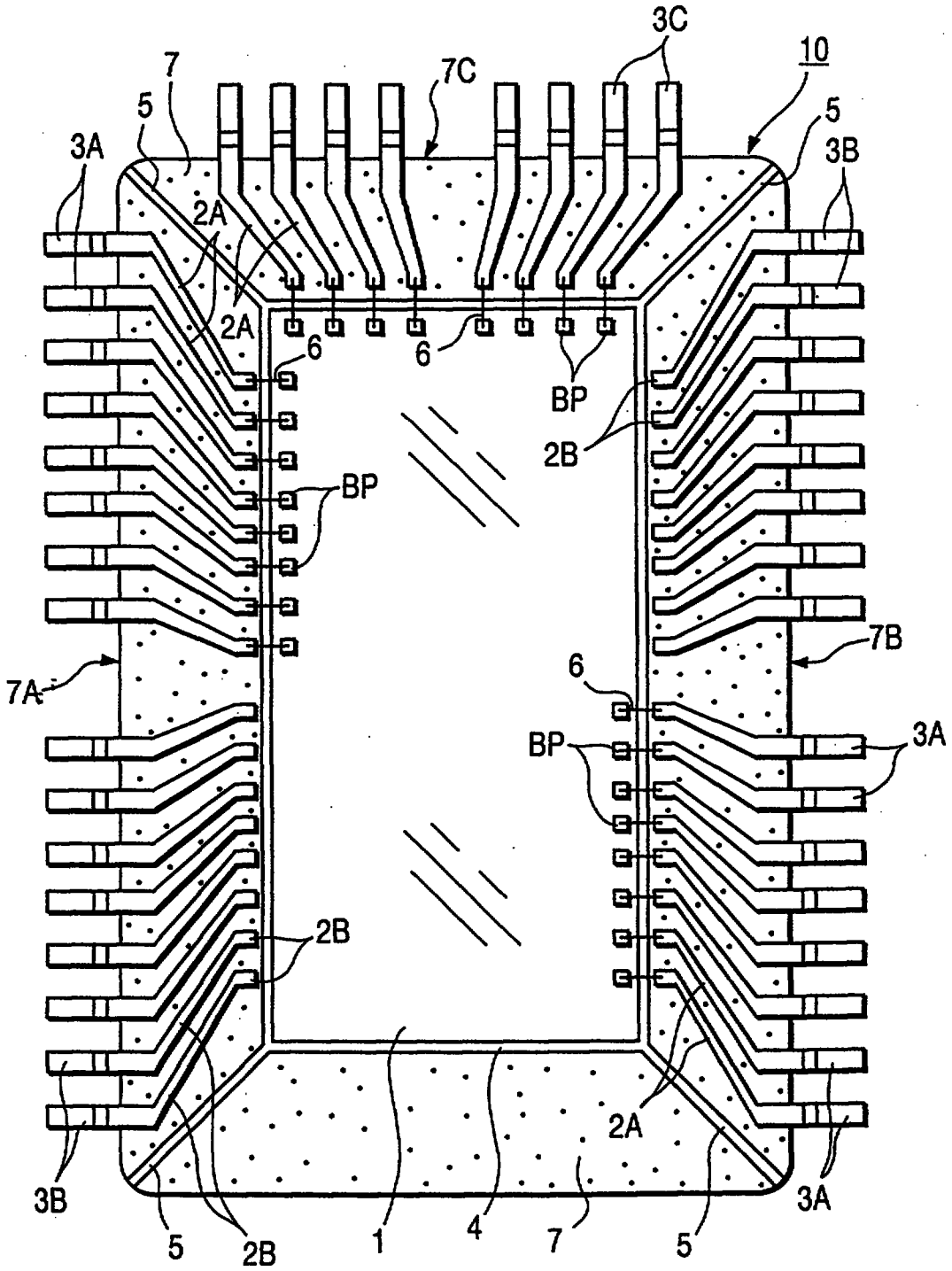
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FIG. 8



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FIG. 9



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FIG. 10(A)

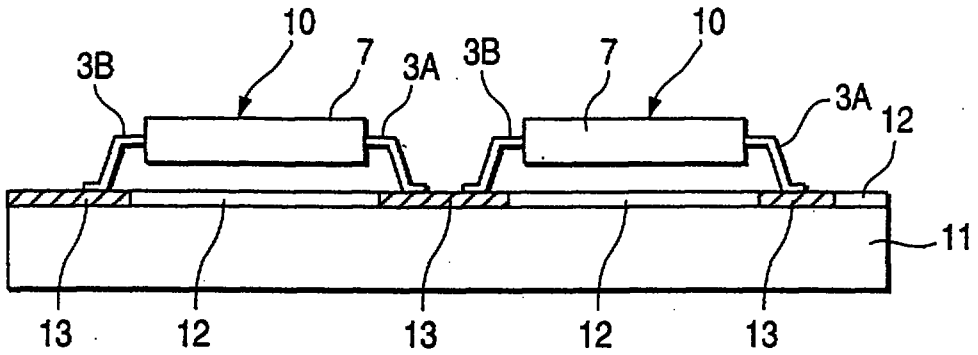


FIG. 10(B)

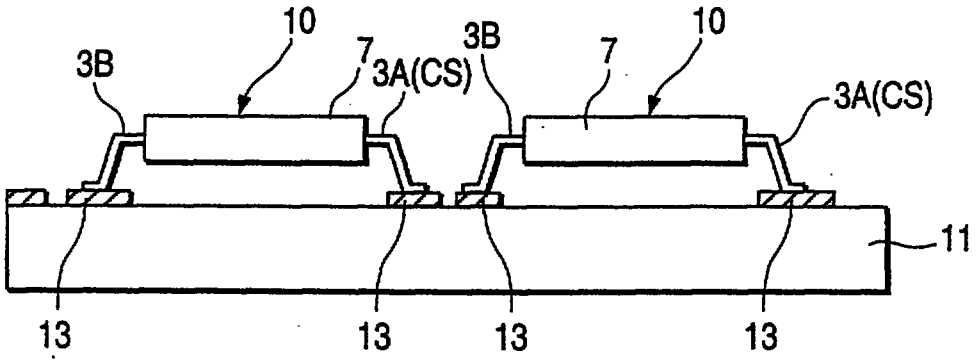
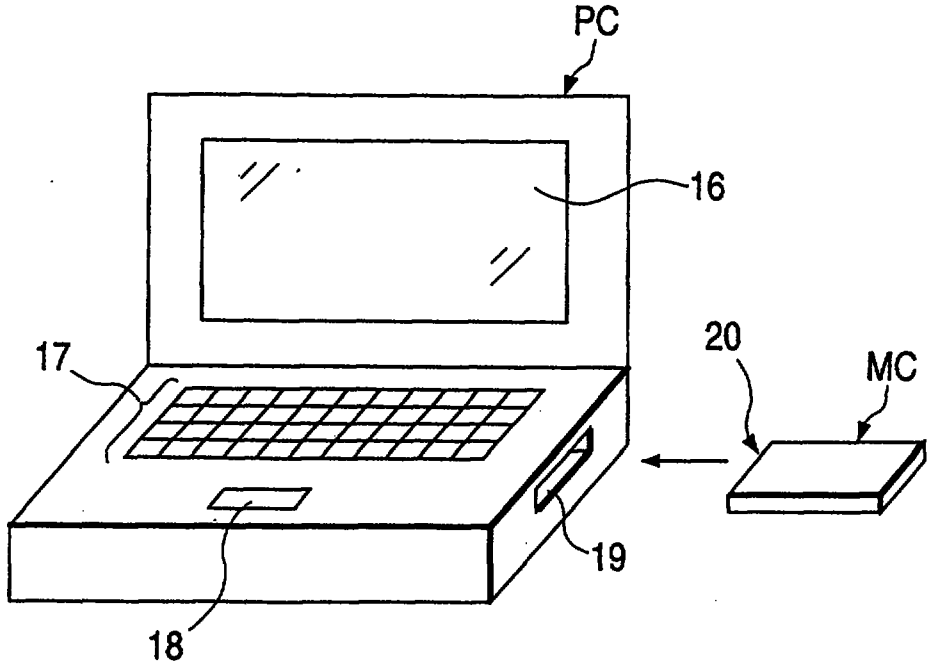


FIG. 11



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FIG. 12

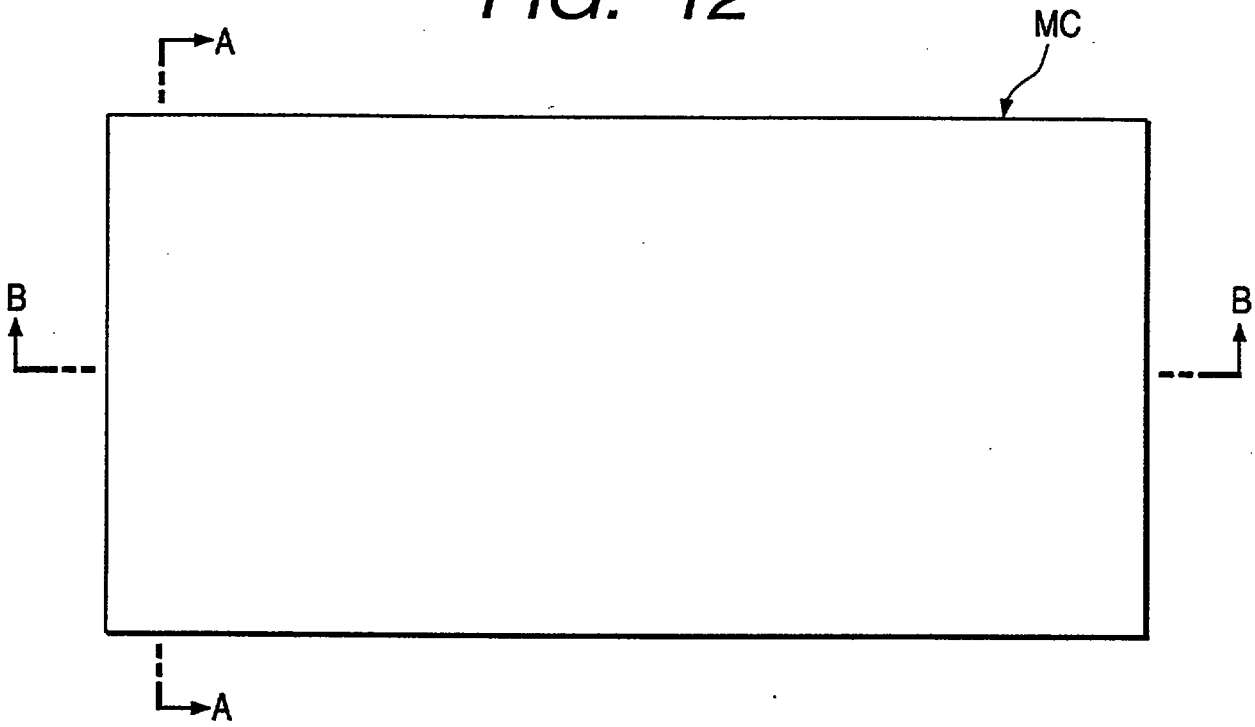


FIG. 13

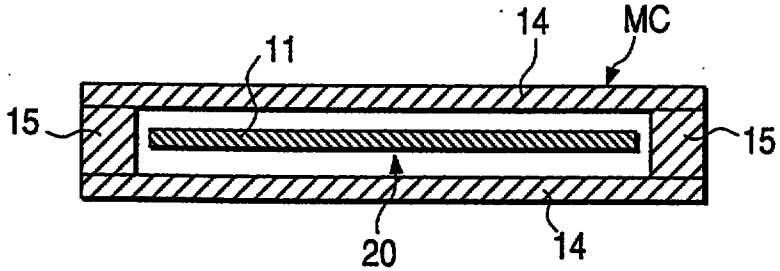
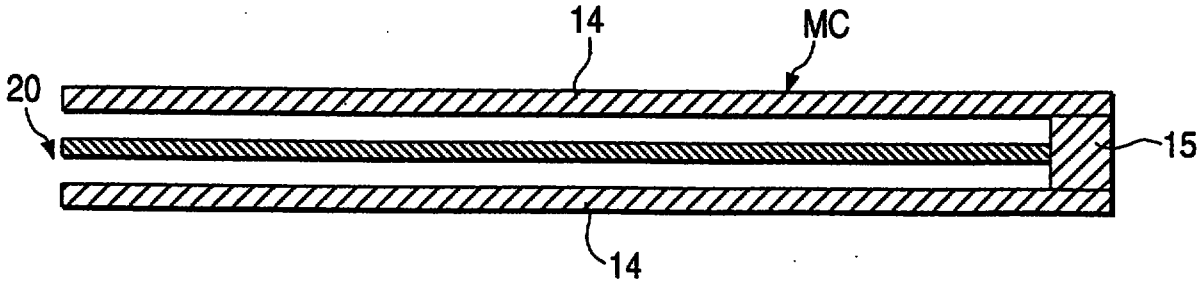


FIG. 14



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FIG. 15

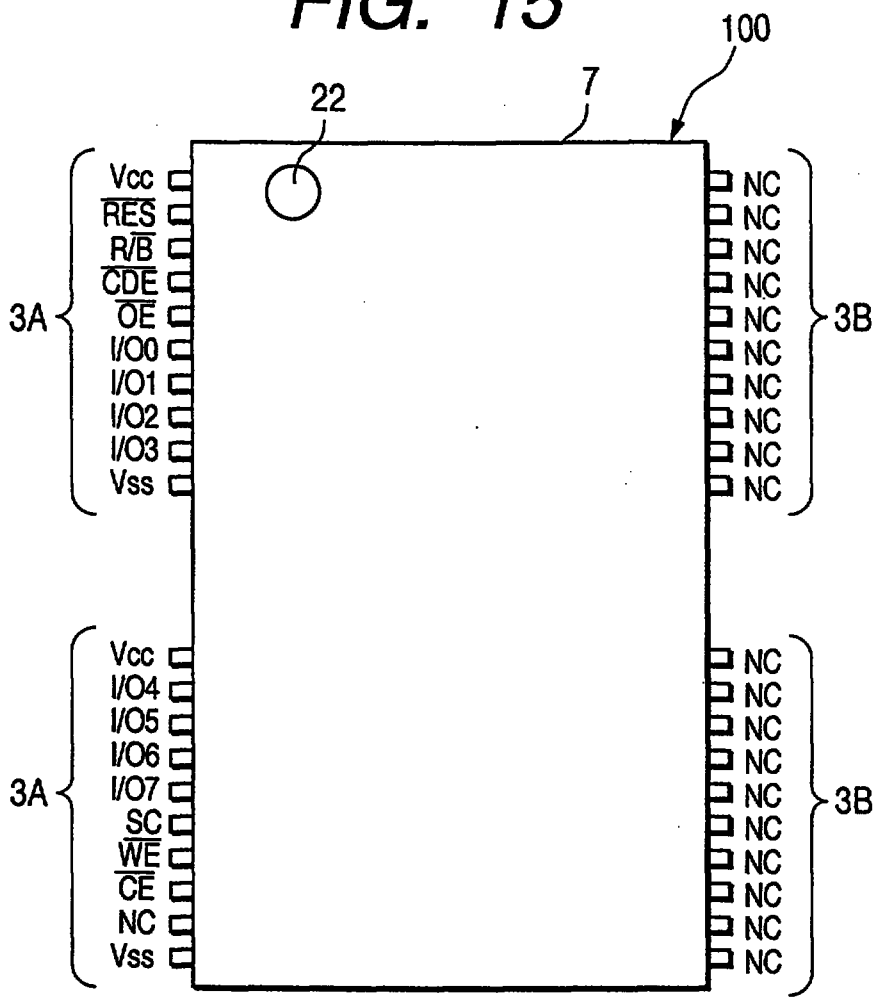
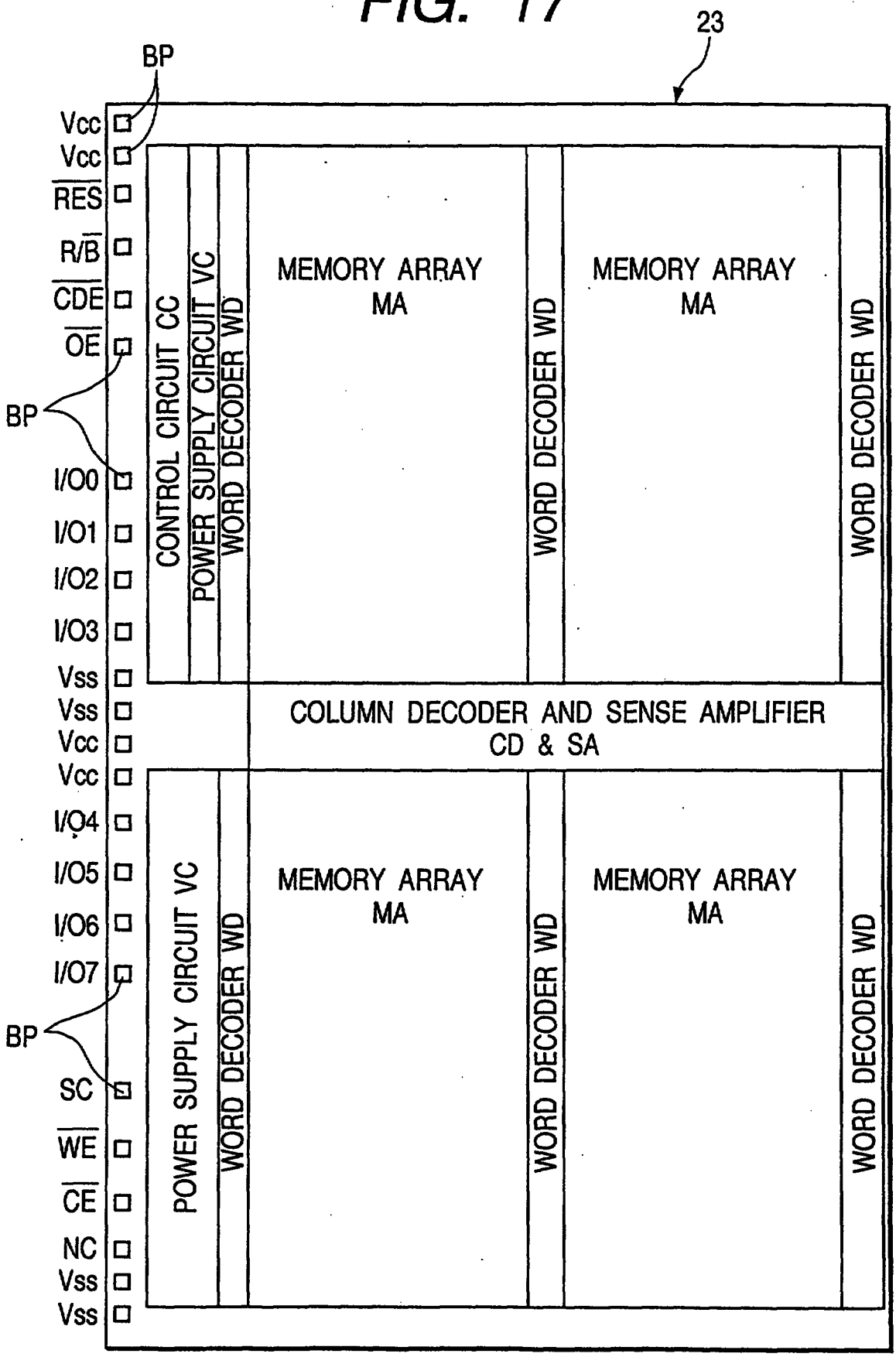


FIG. 16

PIN DESCRIPTION	
PIN NAME	FUNCTION
I/O0-I/O7	INPUT / OUTPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
$\overline{CDE}$	COMMAND DATA ENABLE
Vcc	POWER SUPPLY
Vss	GROUND
R/$\overline{B}$	READY / $\overline{BUSY}$
$\overline{RES}$	RESET
SC	SERIAL CLOCK
NC	NO CONNECT

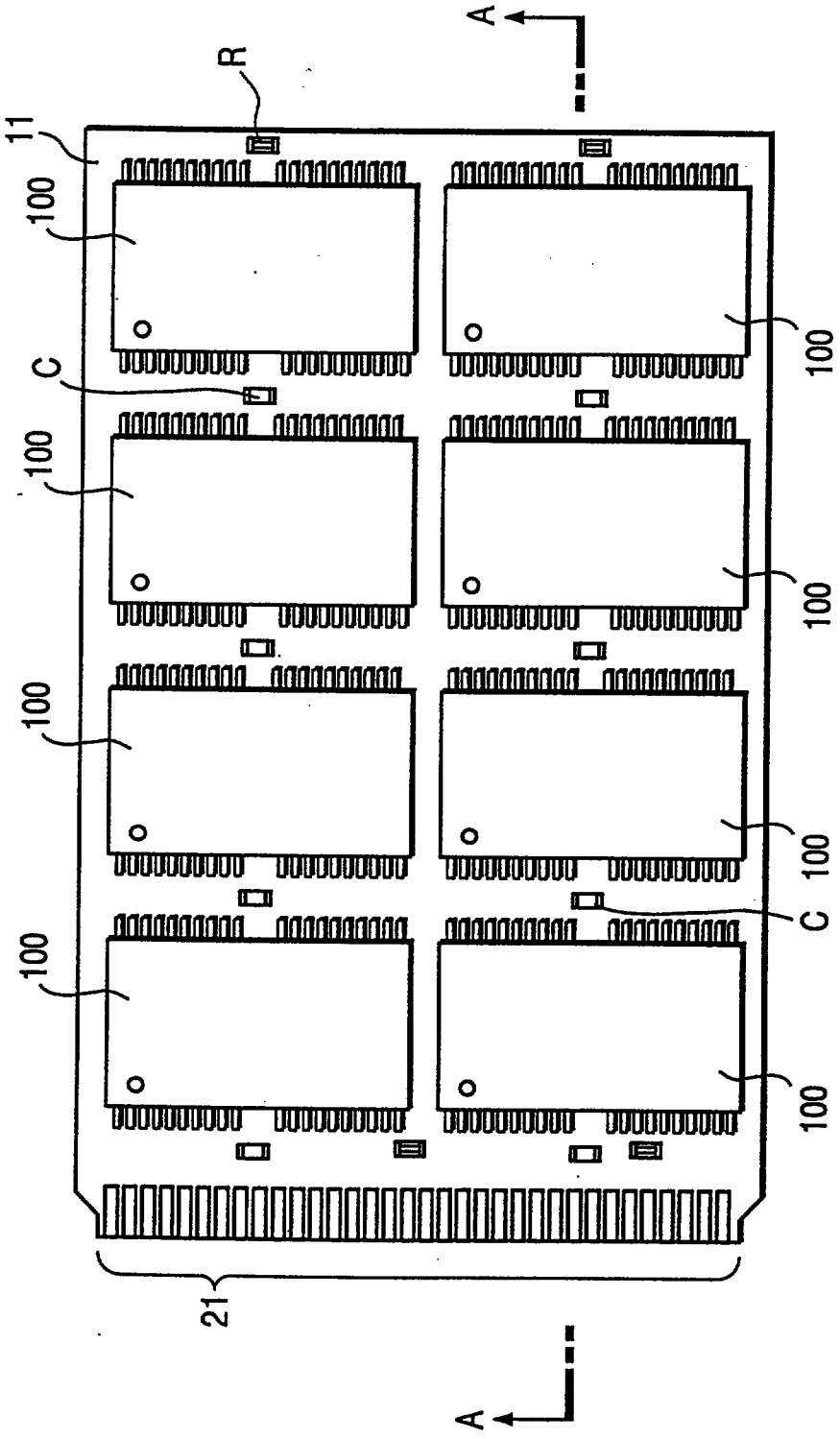
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FIG. 17



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FIG. 18



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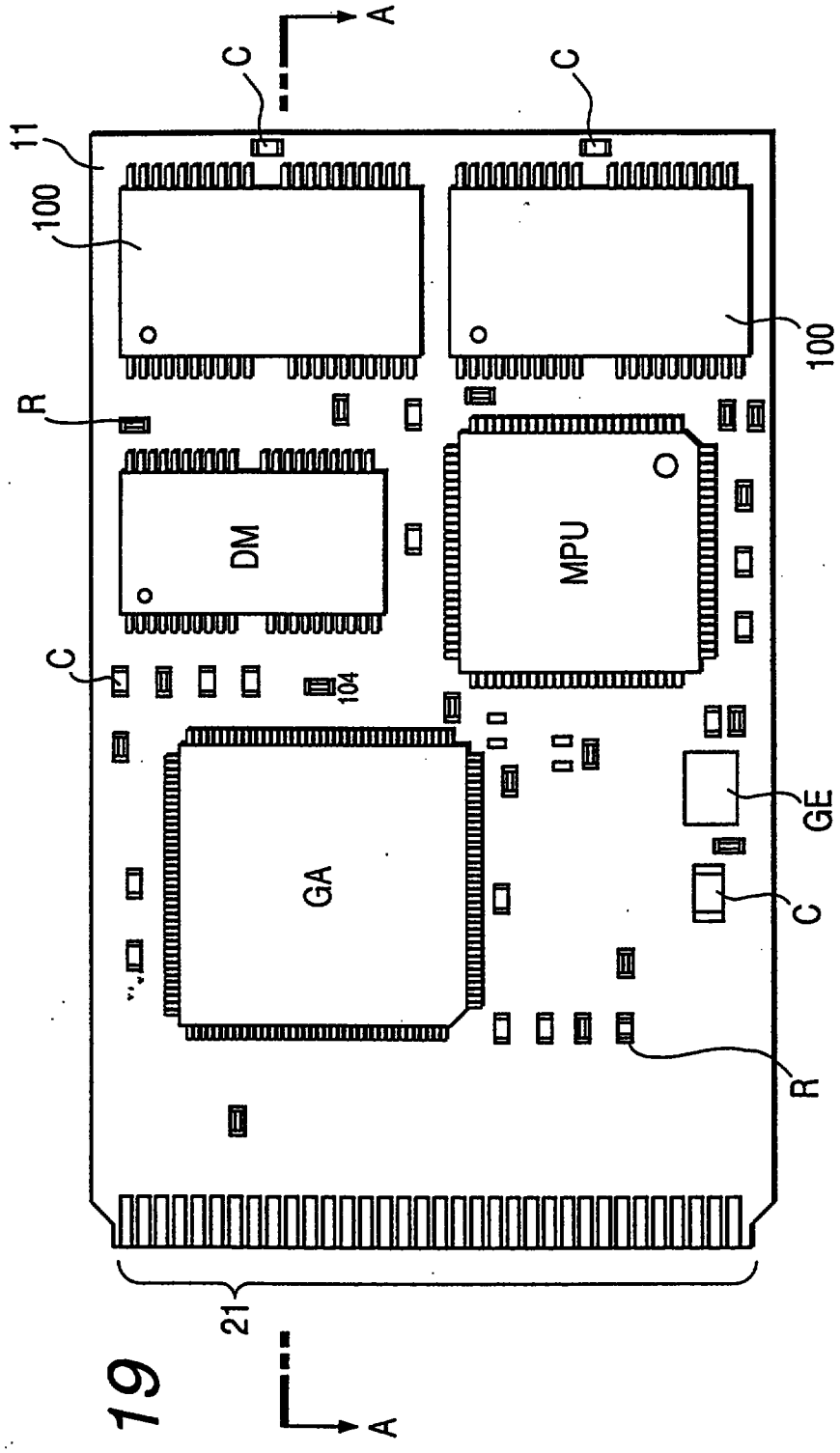


FIG. 19

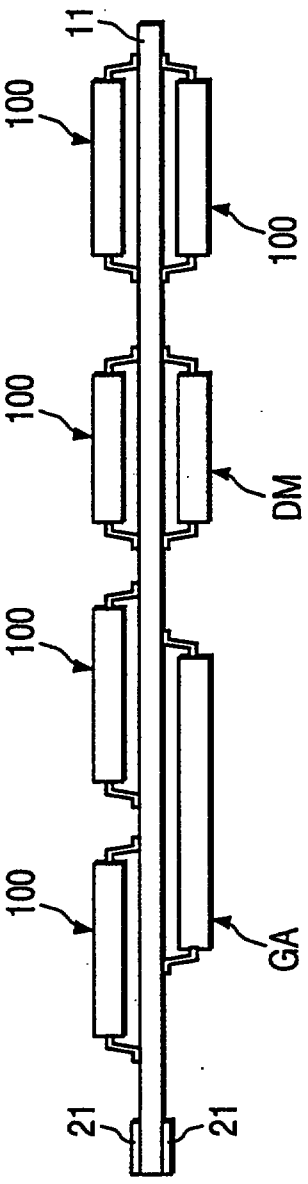
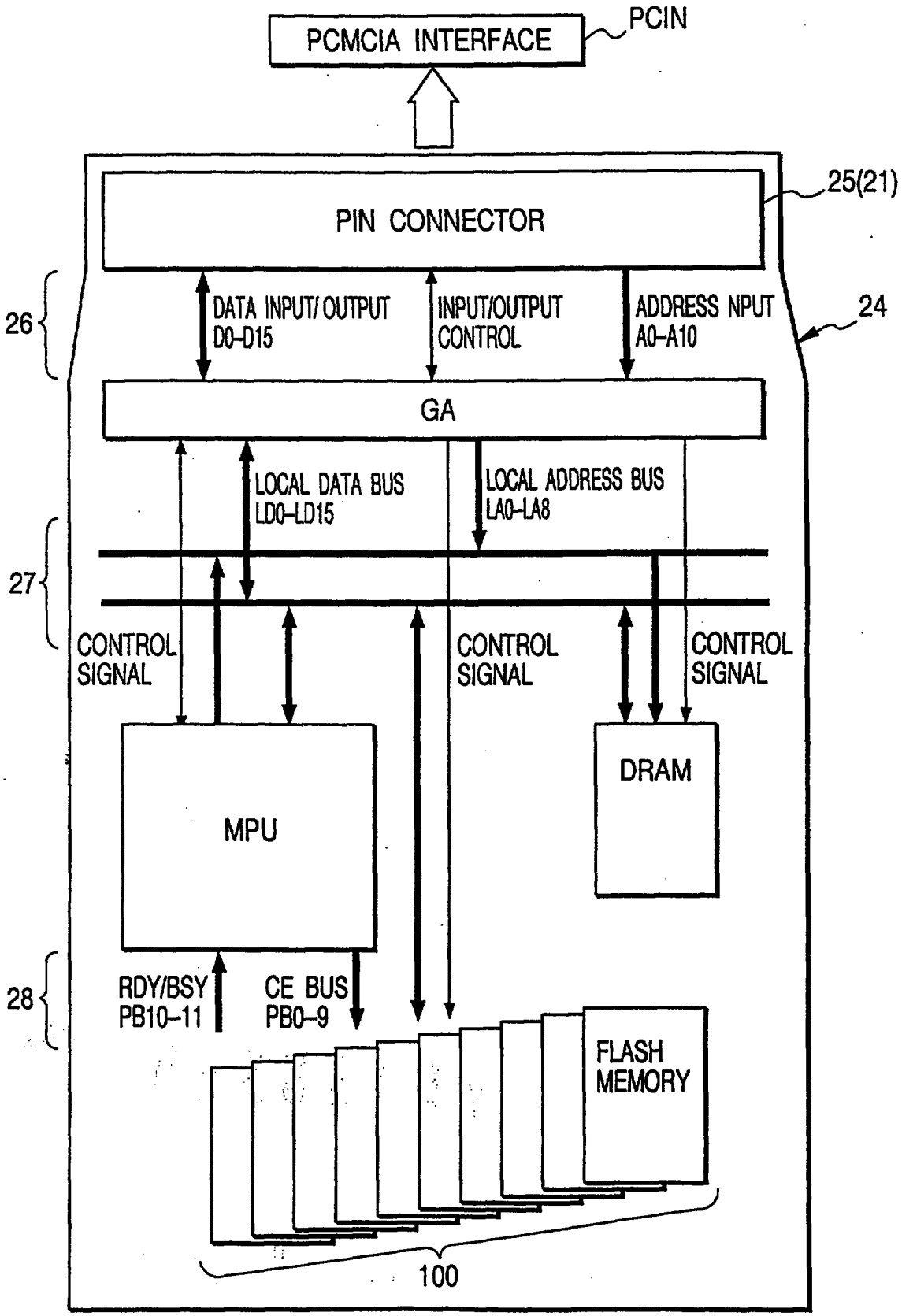


FIG. 20

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FIG. 21



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1. A semiconductor device comprising:

a rectangular-shaped mounting board consists of a pair of long sides and short sides extending perpendicular to said long sides and said mounting board having a plurality of wirings on its major surface, said wirings are extended along said long sides, respectively; and

a plurality of semiconductor memory devices mounted on said major surface of said mounting board, each of said semiconductor memory devices including:

a rectangular-shaped semiconductor chip having a plurality of external terminals on its major surface, said semiconductor chip having a pair of long sides extending in a first direction and a pair of short sides extending in a second direction generally perpendicular to said first direction;

said external terminals being arranged along one of said pair of long sides;

a plurality of first leads arranged along said one of said pair of long sides, said first leads each including inner lead portions and outer lead portions, and the end portions of said inner lead portions being electrically connected to corresponding external terminals;

a plurality of second leads arranged along the other of said pair of long sides, each said second lead are arranged opposite to said first lead respectively, and including inner lead portions and outer lead portions, and said second lead portions being not electrically connected to said semiconductor chip;

a sealing body in which said semiconductor chip, the inner lead portions of said first leads, the inner lead portions of said second leads are packaged, said sealing body being formed into a rectangular shape having a pair of long sides extending in said first direction and a pair of short sides extending in said second direction,

the outer leads of said first leads protruding from one of the pair of long sides of said sealing body, and the outer leads of said second leads protruding from the other of said pair of long sides,

wherein one of said first lead and one of said second lead are electrically connected by one of said wiring, respectively.

2. A semiconductor device according to claim 1, wherein said one of said second lead is arranged in opposite to said one of said first lead.

3. A semiconductor device according to claim 1, wherein all said second leads are arranged in opposite to said first leads, respectively.

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4. A semiconductor device according to claim 1, wherein said plurality of semiconductor memory devices are arranged along said long side of said mounting board.

5. A semiconductor device according to claim 4, wherein said plurality of wirings are extended under said plurality of semiconductor memory devices.

6. A semiconductor device according to claim 5, wherein said plurality of wirings are arranged to parallel each other.

7. A semiconductor device according to claim 1, wherein one of said semiconductor memory device and the other one of said semiconductor device are adjoined each other, said second leads of one of said semiconductor memory device and said first leads of the other one of said semiconductor memory device being arranged closely.

8. A semiconductor device according to claim 7, wherein said first leads and said second leads of said semiconductor memory devices are electrically connected by said one of said wiring.

9. A semiconductor device according to claim 1, wherein said plurality of first leads and said second leads are bonded to said mounting board by solder.

10. A semiconductor device according to claim 1, further comprising:
a plurality of connector terminals are arranged along one of said shorter sides of said mounting board.

11. A semiconductor device according to claim 1, wherein eight semiconductor memory devices are mounted on said mounting board.

12. A semiconductor device according to claim 1, wherein said one of said wiring commonly to said plurality of devices inputs a signal.

13. A semiconductor device comprising:
a mounting board having a plurality of wirings on its major surface; and
a plurality of semiconductor memory devices mounted on said major surface of said mounting board, each of said semiconductor memory devices including:
a rectangular-shaped semiconductor chip having a plurality of external terminals on its major surface, said semiconductor chip having a pair of long sides extending in a first direction and a pair of short sides extending in a second direction perpendicular to said first direction, and
said external terminals being arranged along one of said pair of long sides;
a plurality of first leads arranged along said one of said pair of long sides, said first leads each including inner lead

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portions and outer lead portions, and the end portions of said inner lead portions being electrically connected to corresponding external terminals;

a plurality of second leads arranged along the other of said pair of long sides, each said second lead are arranged opposite to said first lead respectively and including inner lead portions and outer lead portions, and said second lead portions being not electrically connected to said semiconductor chip;

a sealing body in which said semiconductor chip, the inner lead portions of said first leads and the inner portions of said second leads are packaged, said sealing body being formed into a rectangular shape having a pair of long sides extending in said first direction and a pair of short sides extending in said second direction;

the outer leads of said first leads protruding from one of the pair of long sides of said sealing body; and the outer leads of said second leads protruding from the other of said pair of long sides,

wherein one of said first lead and one of said second lead which is opposite to one of said first lead are electrically connected by the same wiring which is one of said wiring.

14. A semiconductor device according to claim 13, wherein all said second leads are arranged in opposite to said first leads, respectively.

15. A semiconductor device according to claim 13, wherein said plurality of wirings are extended under said plurality of semiconductor memory device and arranged along said second direction.

16. A semiconductor device according to claim 15, wherein said plurality of wirings are arranged to parallel each other.

17. A semiconductor device according to claim 13, wherein one of said semiconductor memory device and the other one of said semiconductor memory device are adjoined each other and mounted on said mounting board, said second leads of one of said semiconductor memory device and said first leads of the other one of said semiconductor memory device being arranged closely.

18. A semiconductor device according to claim 17, wherein said first leads and second leads of said semiconductor memory devices are electrically connected by said same wiring.

19. A semiconductor device according to claim 13, wherein said plurality of first leads and said second leads are bonded to said mounting board by solder.

20. A semiconductor device according to claim 13, wherein eight semiconductor memory devices are mounted on said mounting board.

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21. A semiconductor device according to claim 13, wherein said same wiring commonly to said plurality of devices inputs a signal.

22. A semiconductor device comprising:

a mounting board having a pair of long sides and a plurality of wirings on its major surface; and

a first and a second semiconductor memory devices are mounted on said major surface of said mounting board,

each of said first and said second semiconductor memory device including:

a rectangular-shaped semiconductor chip having a pair of long sides extending in a first direction and a pair of short sides extending in a second direction perpendicular to said first direction;

a plurality of external terminals are arranged on its major surface and along one of said pair of long sides;

a plurality of first leads arranged along one of said pair of long sides, said first leads each including inner lead portions and outer lead portions, and the end portions of said inner lead portions being electrically connected to corresponding said external terminals;

a plurality of second leads arranged along the other of said pair of long sides, each said second lead are arranged opposite to said first leads respectively, and including inner lead portions and outer lead portions, and said second leads being not electrically connected to said semiconductor chip;

a sealing body in which said semiconductor chip, the inner lead portions of said first leads, the inner lead portions of said second leads are packaged, said sealing body being formed into a rectangular shape having a pair of long sides extending in said first direction and a pair of short sides extending in said second direction;

the outer leads of said first leads protruding from one of the pair of long sides of said sealing body, and the outer leads of said second leads protruding from the other of said pair of long sides of said sealing body,

wherein one of said first leads of said first and second memory device are electrically connected by one of said wiring, and one of said second lead of said first memory device being electrically connected to said wiring.

23. A semiconductor device according to claim 22, wherein said wiring is extended along in a direction where said first semiconductor device and said second semiconductor device are arranged.

24. A semiconductor device according to claim 23, wherein said wiring is extended along said long sides, linearly.

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25. A semiconductor device according to claim 22, wherein said second lead of said first and said second semiconductor device are arranged in opposite to said first lead of said first and said second semiconductor device, respectively.

26. A semiconductor device according to claim 22, wherein said wirings are extended under said first and said second semiconductor devices.

27. A semiconductor device according to claim 26, wherein said plurality of wirings are arranged to parallel each other.

28. A semiconductor device according to claim 22, wherein said first and said second semiconductor memory devices are adjoined each other, said second leads of said first semiconductor memory device and said first leads of said second semiconductor memory device being arranged closely.

29. A semiconductor device according to claim 22, wherein said plurality of outer lead portions of said first and said second leads are bonded to said mounting board by solder.

30. A semiconductor device according to claim 22, further comprising:

a plurality of connector terminals are arranged along one of said shorter sides of said mounting board.

31. A semiconductor device according to claim 22, wherein said wiring commonly to said first and said second semiconductor memory devices inputs a signal.