

A DEFLECTION DRIVER IN A VIDEO APPARATUS

The invention relates to a transistor drive circuit for a deflection circuit output stage of a television or other such display device. In particular, the invention relates to a drive circuit of a horizontal deflection circuit output stage in which a switching output transistor, operating in a switching mode, produces a deflection current in a horizontal deflection winding.

US-A-4,323,825 discloses an electron beam deflection circuit useful in cathode ray tube displays which employ television scanning principles. The deflection circuit has transformer coupling between a source of horizontal drive signal and a switching transistor for the horizontal deflection coil. Energy stored in the transformer during the scan and retrace time is utilized during the scanning time to provide base current to the switching transistor. In addition, the transformer has a second primary winding connected in the emitter circuit of the switching transistor in a manner to allow positive feedback. The positive feedback enhances and sustains the base current during scanning time and controls its magnitude.

Another prior art horizontal deflection circuit that has been used in various color television receivers includes a driver stage having a transformer coupled to a control terminal of the output transistor of the deflection circuit output stage. The driver stage further includes a second switching transistor having a collector electrode that is coupled to a primary winding of the transformer. When the switching transistor of the driver stage is conductive, magnetic energy is stored in the inductance of the primary winding. At the same time, a transformer coupled voltage developed across a secondary winding of the transformer causes the switching output transistor of the output stage, driven by the voltage developed in the secondary winding of the transformer, to be non-conductive. When the switching transistor of the driver stage becomes

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non-conductive, the stored magnetic energy in the coupling transformer produces, in a flyback manner, a winding current that flows in the secondary winding of the coupling transformer to form a forward base current for the output
5 transistor. The winding current turns on the switching output transistor and maintains it turned-on until substantially the end of horizontal trace. Such forward base current is produced entirely from the magnetic energy previously stored in the transformer. Therefore, the
10 forward base current is, disadvantageously, a downramping current during the second half of trace; whereas, the deflection current and the collector current of the output transistor are upramping.

The deflection circuit output transistor is
15 typically a bipolar transistor that is driven hard enough to stay well in saturation until the end of trace, when the deflection current is at its peak. However, any excess drive current may, disadvantageously, lead to an increase in the turn-off time and, hence, to an increase in turn-off
20 losses of the deflection circuit output transistor. This problem is aggravated at higher scan rates.

Because the entire energy required for generating the forward base current that drives the output transistor is produced in the aforementioned prior art
25 driver stage, power losses in the driver stage may be, disadvantageously, high. Furthermore, as indicated before, the forward base current becomes increasingly smaller towards the end of the second half of trace; whereas, the forward base current requirement of the output transistor
30 becomes increasingly larger when the collector current is upramping. Moreover, any variation of the duty cycle of the driver transistor may, disadvantageously, affect the value of the forward base current of the output transistor.

It may be desirable to produce a current in the
35 secondary winding of the transformer having an upramping waveform, during the second half of trace, that tracks the upramping change in the collector current. In this way, the forward base current is upramping during the second half of trace.



In accordance with one aspect of the invention, there is provided a television deflection apparatus, comprising: a deflection winding; a first switching transistor coupled to said deflection winding and responsive to a switching control signal developed at a control terminal of said first switching transistor for generating a deflection current in said deflection winding such that, during a portion of a given deflection cycle, each of said deflection current and a transistor current flowing in a main current path of said first switching transistor varies in a ramping manner; a source of an input signal at a frequency that is related to a deflection frequency; and a transformer having a first winding responsive to said input signal, a second winding, and a third winding; characterized in that the second winding is responsive to one of said transistor and deflection currents and the third winding has a first terminal coupled between said second winding and said transistor, and a second terminal coupled to said control terminal for generating said control signal that varies, in a ramping manner during said trace interval of said deflection cycle, at a rate of change determined by the rate of change of said one of said transistor and deflection currents.

In accordance with another aspect, there is provided a television deflection apparatus, comprising: a deflection retrace resonant circuit including a deflection winding and a retrace capacitance; a first switching transistor responsive to a control signal and coupled to said retrace resonant circuit for performing a switching operation that generates a deflection current in said deflection winding, said retrace resonant circuit generating a first current that varies in a ramping manner during a trace portion of a given deflection cycle and that flows between a pair of main current conducting terminals of said transistor; a source of an input signal at a frequency that is related to a deflection



frequency; a transformer having a first winding that is coupled to said source of said input signal, a second winding that is coupled to a main current conducting terminal of said transistor, and a third winding coupled to a control terminal of said first switching transistor; characterized in that a first portion of the current that flows through said first switching transistor flows in said second winding, and a second portion of the current that flows through said first switching transistor flows in said third winding for transformer coupling each of said input signal and first current to said control terminal of said first switching transistor to develop said control signal at said control terminal, said control signal having a frequency that is determined by said input signal and a level that varies in accordance with the ramping manner variation of said first current during said trace portion of said deflection cycle.

In accordance with a further aspect, there is provided a television deflection apparatus, comprising: a deflection retrace resonant circuit including a deflection winding and a retrace capacitance; a first switching transistor responsive to a control signal at a frequency that is related to a deflection frequency and coupled to said retrace resonant circuit for performing a switching operation that generates a deflection current in said deflection winding; a transformer having a first winding that is coupled to a control terminal of said first switching transistor for developing said control signal at said control terminal; a source of an input signal at a frequency that is related to a deflection frequency; and a second switching transistor responsive to said input signal and coupled to a second winding of said transformer for generating a first current in said second switching transistor and in said second winding of said transformer that is transformer coupled via said



transformer to said control terminal of said first
switching transistor to develop said control signal at
said control terminal during normal operation,
characterized by means responsive to an on/off control
5 signal for maintaining said second switching transistor
conductive during a transition interval that precedes a
change from normal operation to a standby mode of
operation, such that said first current flows in said
second winding and in said transistor, during said
10 transition interval.

In the Drawing:

FIGURE 1 illustrates a driver stage, embodying
an aspect of the invention, of a horizontal deflection
circuit output stage;

15 FIGURES 2a-2f illustrate waveforms useful for
explaining the operation of the circuit of FIGURE 1;

FIGURES 3a-3f illustrate additional waveforms
useful for explaining the operation of the circuit of
FIGURE 1;

20 FIGURE 4 illustrates a driver stage similar to
that in FIGURE 1 that is used for driving a horizontal
output stage of a CRT having a 90° deflection angle;

FIGURE 5 illustrates a driver stage similar to
that in FIGURE 1 that is used for driving a horizontal
25 output stage having a diode modulator;

FIGURE 6 illustrates a driver stage similar to
that in FIGURE 1 that is used for driving a horizontal



output stage having a switched E-W raster correction circuit;

FIGURES 7a-7d illustrate waveforms useful for explaining the operation of each of the circuits of FIGURES 4 and 6; and

FIGURE 8 illustrates a driver stage of a deflection circuit operating at 32KHZ.

FIGURE 1 illustrates a driver stage 100, embodying an aspect of the invention, for driving a switching output transistor Q2 of a horizontal deflection circuit output stage 101 of a television receiver. A conventional horizontal oscillator 102, that produces, during normal power-on operation, an output signal V_{osc} , at a horizontal frequency f_H , that is approximately 16 KHZ during normal power-on operation, is coupled via a capacitor C2 and a resistor R2 to a base electrode of a driver transistor Q1. A diode D1 coupled to the base of transistor Q1 prevents the base voltage from becoming excessively negative. A collector of transistor Q1 is coupled to one end terminal of a primary winding W1 of a coupling transformer T1. The other end terminal of winding W1 is AC bypassed to ground by a filter capacitor C1, and coupled via a current limiting resistor R1 to a source of supply voltage $V+$ such that resistor R1 and capacitor C1 form a ripple filter.

A secondary winding W2 of transformer T1 is coupled across a base-emitter junction of transistor Q2 and across a resistor R4. A junction terminal 101a that is coupled at a junction of winding W2, resistor R4 and the emitter of transistor Q2, is coupled to one end terminal of a winding W3 of transformer T1. The other end terminal of winding W3 is coupled to ground.

The collector of transistor Q2 is coupled to a damper diode D2 of a conventional horizontal deflection circuit 103. Circuitry 103 further includes a horizontal deflection winding L_H , a retrace capacitor C4, a trace capacitor C_S , a linearity inductor L_{LIN} , and a linearity resistor R_5 , that are coupled in a well-known manner. A



supply voltage B+ is coupled to circuit 103 via a winding T2a of a transformer T2. During retrace, circuitry 103 forms a retrace resonant circuit.

FIGURES 2a-2f and 3a-3f illustrate waveforms useful for explaining the operation of the circuit of FIGURE 1. Similar symbols and numerals in FIGURES 1 and 2a-2f and 3a-3f indicate similar items or functions.

In operation, driver transistor Q1 of FIGURE 1 is conductive as a result of a signal V_{OSC} of FIGURE 2a being positive until time t_1 of FIGURE 2c that causes transistor Q2 to be nonconductive. The magnetic energy supplied by a collector current I_{c1} of transistor Q1 is stored in winding W1 of FIGURE 1. When transistor Q1 is turned off, during interval t_1-t_3 of FIGURE 2a, the stored energy produces in winding W2 of FIGURE 1 a forward base current I_{b2} of transistor Q2. Current I_{b2} is sufficient to turn on deflection transistor Q2 and to maintain it in saturation prior to time t_2 of FIGURE 2e.

The amplitude of current I_{b2} of FIGURE 2d remains substantially constant during the first half of trace, interval t_1-t_2 . This is so because windings W2 and W3 are short circuited by the low impedance of the base-collector junction of transistor Q2 that is coupled in series with the forward biased damper diode D2. At time t_2 , a deflection current I_H in deflection winding L_H of FIGURE 1 reversed polarity. As a result of current reversals in deflection winding L_H of circuitry 103 of FIGURE 1 and in a fly back transformer winding T2a collector current I_{c2} starts flowing in transistor Q2 of FIGURE 1 after time t_2 of FIGURE 2e in an upramping manner.

In accordance with a feature of the invention, upramping collector current I_{c2} that flows as an emitter current through winding W3 of FIGURE 1 is transformer coupled through current transformer T1 to the base of transistor Q2 in accordance with a turns ratio $N2:N3$ of windings W2 and W3, respectively. Transformer coupled current I_{c2} provides a major portion of upramping forward base current I_{b2} of transistor Q2, during the second half



of trace, interval t_2 - t_3 , when collector current I_{c2} is upramping. The base-emitter junction of transistor Q2 forms a very low impedance across winding W2. Therefore, a performance similar to that of an ideal current transformer operation is obtained in transformer T1 for coupling the current in winding W3 to winding W2. The required turns ratio is selected in accordance with a current gain parameter h_{FE} of transistor Q2. For example, when parameter h_{FE} is equal to 4, the selected turns ratio, N2:N3, may be equal to 4. The turns ratio between windings W2 and W3 is determined by the current gain h_{FE} of transistor Q2. Should the core selected for transformer T1 provide tight magnetic coupling, such as for example, when an E-type core is utilized, such turns ratio may be equal to the value of current gain h_{FE} of transistor Q2. On the other hand, if the magnetic coupling is not tight, a lower turn ratio may be chosen.

Upramping base current that is proportional to current I_{c2} is induced in winding W2 of FIGURE 1 only after time t_2 of FIGURE 2d. Transformer coupled upramping current I_{c2} of FIGURE 2e is added to the aforementioned current already provided by the stored magnetic energy in transformer T1 to form upramping base current I_{b2} . The rate of change of current I_{b2} of FIGURE 1, advantageously, closely tracks the base current requirement of deflection transistor Q2, having upramping collector current I_{c2} , in a manner that maintains transistor Q2 in saturation without significantly overdriving the base of transistor Q2, during the second half of trace interval, t_2 - t_3 . In contrast, in the aforementioned prior art driver stage, a base current that is provided is downramping during trace. Consequently, the base current may be unnecessarily high during an interval that is analogous to interval t_1 - t_3 of FIGURE 2d, as shown in dashed line waveform of FIGURE 2d.

Cut-off of transistor Q2 of FIGURE 1 is initiated at time t_3 of FIGURE 2e, when transistor Q1 of FIGURE 1 is switched into saturation. The level of collector voltage V_{c1} of FIGURE 2b at time t_3 and the turns



ratio between windings W1 and W2 of FIGURE 1 determine the amplitude of the negative turn-off voltage developed across the base-emitter junction of transistor Q2. This voltage and the leakage inductance of transformer T1 determine the negative slope dI_{b2}/dt of FIGURE 2d during a storage or turn-off delay interval t_3-t_4 of transistor Q2 of FIGURE 1. By selecting a proper turns ratio of windings W1 and W2, that is, for example, between 5 and 10, the desired negative slope dI_{b2}/dt for optimizing the base carrier discharge can be obtained. This is so because the turns ratio between windings W1 and W2 of transformer T1 determines the leakage inductance of transformer T1. The waveform of collector current I_{c1} of FIGURE 2c shows the peak negative base current used for turning off transistor Q2 at time t_4 of FIGURE 2c, the start of horizontal retrace.

During a substantial portion of the second half of trace, interval t_2-t_3 of FIGURE 2d, the increasing forward base current causes an increasing base-emitter voltage of transistor Q2 of FIGURE 1, which is transformer coupled across winding W3. This transformer coupled voltage is coupled across winding W3 and is coupled in series with deflection transistor Q2. Such series coupled voltage, however, is negligibly small. Therefore, the voltage across winding W3 does not appreciably impair the linearity of the deflection current and of current I_{c2} of FIGURE 2c.

Advantageously, resistor R3 of FIGURE 1 serves to supply a base current that drives transistor Q1 into saturation immediately after oscillator 102 is turned off or made inoperative. Oscillator 102 may be turned off in response to an output signal ON/OFF of a remote receiver, not shown, that is used for turning off the television receiver to operate the receiver in a stand-by mode operation. Advantageously, by being conductive, transistor Q1 prevents self-oscillation of deflection circuit output stage 101 during the transition to standby mode operation. Such self oscillation might have occurred in the absence of



drive pulses from the oscillator 102 and might have caused harmful high current and voltage peaks in output stage 101. Such high peaks might have occurred if driver transistor Q1 were not held in conduction as long as energy is

5 circulating in deflection circuit output stage 101 following the transition to standby mode. The stored energy in the driver transformer might have caused output transistor Q2 to turn on, but not to turn off properly. Transistor Q2 might not turn off properly because the
10 negative going slope of base current I_{b2} , that in normal operation causes transistor Q2 to turn off, is not produced after oscillator 102 ceases operation. By maintaining transistor Q1 conductive during the transition to standby
15 mode of operation, any lengthening of the last deflection cycle, occurring after oscillator 102 ceases operation, is avoided. Such lengthening, disadvantageously, might have overstressed deflection transistor Q2.

Resistor R1 limits the collector current and power dissipation in transistor Q1, during the transition
20 to stand-by mode of operation. The use of a rather high value for resistor R1 such as, for example, 180 ohm is, advantageously, possible. This is so because driver transistor Q1 operates at a lower power level than the analogous transistor in the aforementioned prior art
25 circuit. Consequently, the collector current in transistor Q1, that is in saturation during a transition to standby mode, will not harm transistor Q1. Because resistor R1 has a high value, collector current and power dissipation in transistor Q1 are limited, in the case of a failure in
30 oscillator 102.

Advantageously, a main portion of forward base current I_{b2} of deflection transistor Q2 is derived from its collector current I_{c2} and rises linearly. In contrast, in the aforementioned prior art driver circuit, the entire
35 drive current is supplied by the energy stored in the driver transformer. Therefore, a lower dissipation occurs in driver stage 100 of FIGURE 1. The result is that the



required level of voltage V_+ may be, advantageously, lower than in such prior art driver circuit.

Controlling the wave shape and peak amplitude of base current I_{b2} in a precise manner is desirable to insure
5 saturation of deflection transistor Q2 during the second half of trace. This feature, advantageously, is achieved in the circuit of FIGURE 1 by transformer coupling the emitter current of transistor Q2 that is linearly upramping via winding W3. In comparison, in the aforementioned prior
10 art circuit, an R-C damping network coupled across a primary winding of the coupling transformer is typically used for controlling the waveform of the drive current. However, tolerances of the R-C damping network produce, disadvantageously, a corresponding tolerance spread in the
15 values of the drive current.

FIGURES 3a and 3c illustrate waveforms of signal V_{osc} of FIGURE 1 having different duty cycles and the same frequency and the resulting waveforms of base current I_{b2} of FIGURES 3b and 3f, respectively. As can be seen, the
20 peak amplitude of base current I_{b2} is the same in both cases. The collector current I_{c2} of FIGURE 3c is also unaffected by the duty cycle variation of signal V_{osc} .

FIGURE 4 illustrates a deflection circuit for a pin-free 90° CRT that includes a driver stage similar to
25 that shown in FIGURE 1. The corresponding waveforms are shown in FIGURES 7a-7d. Similarly, FIGURE 5 illustrates a deflection circuit for a 110° CRT using a diode modulator. The corresponding waveforms are shown in FIGURES 2a-2f and 3a-3f.

30 FIGURE 6 illustrates a deflection circuit for a 110° CRT using a switched East-West raster correction circuit. The applicable waveforms are shown in FIGURES 7a-7d. Similar symbols and numerals in FIGURES 1, 2a-2f, 3a-3f, 4-6 and 7a-7d indicate similar items or functions.

35 The reason that the waveforms of FIGURES 7b and 7c are different from those in FIGURES 2d and 2e, respectively, and from those in FIGURES 3b and 3c, respectively, is that in FIGURES 4 and 6 the damper diode



is coupled across transistor Q2. The damper diode of FIGURE 4, for example, forms with transistor Q2 an integrated circuit. This results in the deflection current in winding L_H to flow also through winding W3, during the first half of trace. In contrast, in FIGURE 1, deflection current I_H does not flow through winding W3 during the first half of trace because the cathode of diode D2 is coupled to ground directly and not via winding W3.

Transformer T1 of FIGURE 6, may, preferably, have a lower primary winding inductance and a slightly higher turns ratio between windings W2 and W3 than in the circuit of FIGURE 1 having a discrete damper diode D2.

In an arrangement where initiating standby mode of operation is obtained by switching off voltage $V+$ of FIGURE 1, resistor R3 may, preferably, be coupled to a positive voltage $V+'$, as shown in broken line. Voltage $V+'$ is derived from a secondary winding T2b of a flyback transformer T2, rectified by a diode 77 and filtered by a capacitor 78. This will ensure a fail safe transition from normal to standby operation by maintaining transistor Q1 in saturation during the aforementioned transition to standby mode operation.

FIGURE 8 illustrates a deflection circuit for a CRT operating at a deflection frequency of $2xf_H$, that is approximately 32 KHz. Similar symbols and numerals in FIGURES 1 and 8 indicate similar items or functions. The driver stage of FIGURE 8 is similar to that shown in FIGURE 1.

As shown in FIGURES 1, 4-6 and 8, driver stage 100 can be easily adapted to many types of horizontal output transistors and to different yoke impedances and is well suited for higher scan rate applications. The component count required for producing the upramping base current is reduced relative to that required in some prior art circuits. The upramping base current improves the efficiency of the driver stage. The well controlled base driver waveform produces a lower dissipation in the output stage and an increased reliability.





CLAIM:

1. A television deflection apparatus, comprising:
a deflection retrace resonant circuit (C_4, C_S, L_{IN}, L_H) including a deflection winding (L_H) and a retrace capacitance (C_4);

a first switching transistor (Q2) responsive to a control signal (I_{b2}) at a frequency that is related to a deflection frequency and coupled to said retrace resonant circuit for performing a switching operation that generates a deflection current (I_H) in said deflection winding (L_H);

a transformer (T1) having a first winding (W2) that is coupled to a control terminal of said first switching transistor (Q2) for developing said control signal at said control terminal;

a source (102) of an input signal (V_{osc}) at a frequency that is related to a deflection frequency; and

a second switching transistor (Q1) responsive to said input signal and coupled to a second winding (W1) of said transformer (T1) for generating a first current (I_{c1}) in said second switching transistor and in said second winding of said transformer that is transformer coupled via said transformer to said control terminal of said first switching transistor (Q2) to develop said control signal at said control terminal during normal operation, characterized by means (R3, T26) responsive to an on/off control signal, which turns off said source (102) of said input signal (V_{osc}) to initiate a standby mode of operation, for maintaining said second switching transistor conductive during a transition interval that precedes a change from normal operation to said standby mode of operation, such that said first current flows in said second winding and in said transistor, during said transition interval.

