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(74) Agent: **BACHAND, Richard A.**; 5775 Morehouse Drive,
San Diego, California 92121 (US).

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(71) Applicant (for all designated States except US): **QUALCOMM Incorporated** [US/US]; Attn: International IP Administration, 5775 Morehouse Drive, San Diego, California 92121 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **DAI, Liang** [CN/US]; 5775 Morehouse Drive, San Diego, California 92121 (US). **LEWIS, Brandon Wayne** [US/US]; 5775 Morehouse Drive, San Diego, California 92121 (US). **BRIDGES, Jeffrey Todd** [US/US]; 5775 Morehouse Drive, San Diego, California 92121 (US). **CHEN, Weihua** [CN/US]; 5775 Morehouse Drive, San Diego, California 92121 (US).

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— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

[Continued on next page]

(54) Title: METHODS AND APPARATUS FOR DYNAMIC FREQUENCY SCALING OF PHASE LOCKED LOOPS FOR MICROPROCESSORS

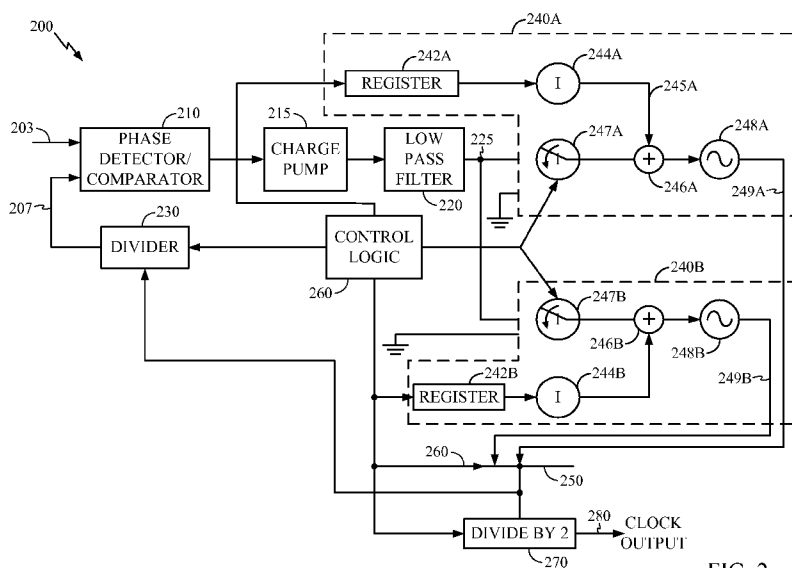


FIG. 2

(57) Abstract: A phase-locked loop employing a plurality of oscillator complexes is disclosed. The phase-locked loop includes a clock output and a plurality of oscillator complexes operable to generate output signals. The phase-locked loop further includes control logic which is configured to selectively couple an output signal of one of the plurality of oscillator complexes to the clock output.

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