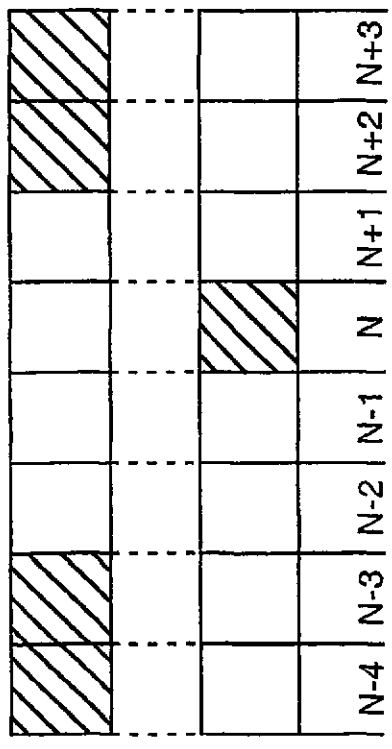

MS RECEIVER
MS TRANSMITTER
N-4
N-3
N-2
N-1
N
N+1
N+2
N+3

FIG. 6

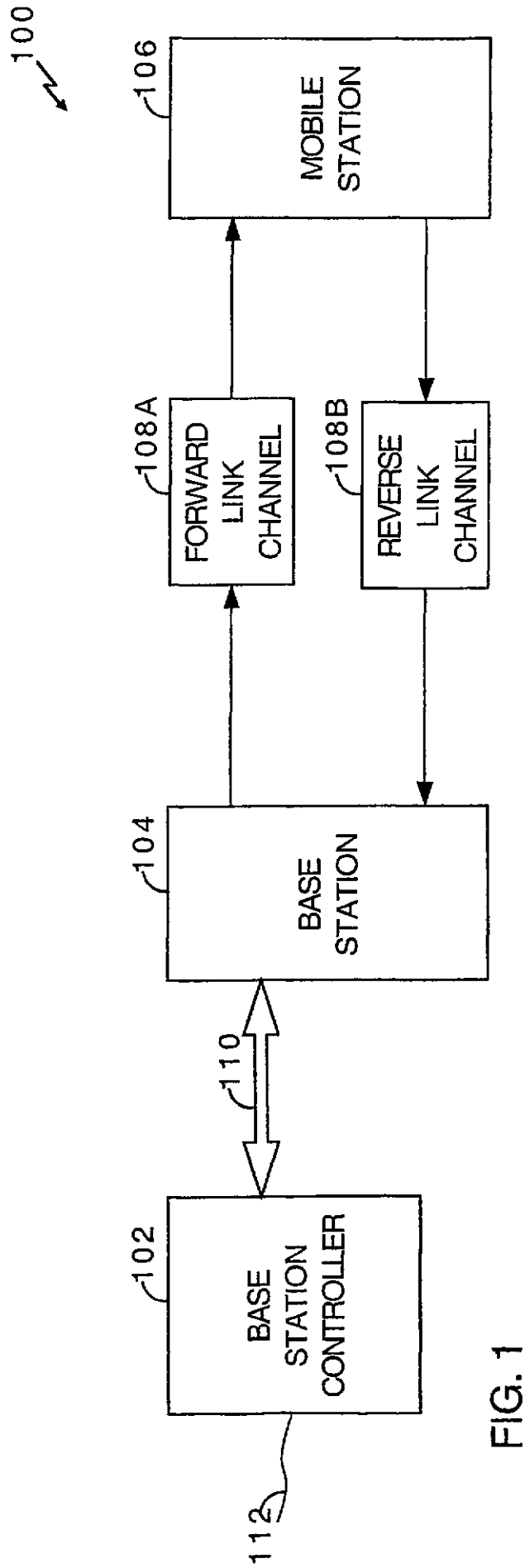

100
106
MOBILE STATION
108A
FORWARD LINK CHANNEL
108B
REVERSE LINK CHANNEL
104
BASE STATION
110
102
BASE STATION CONTROLLER
112

FIG. 1

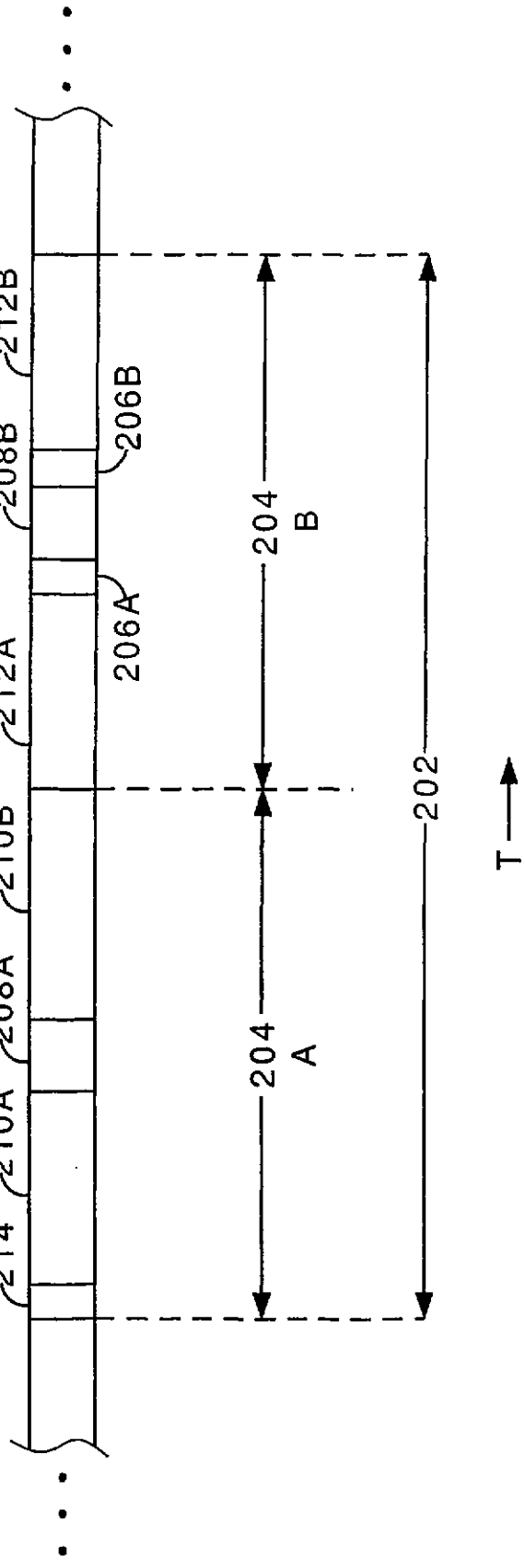



FIG. 2

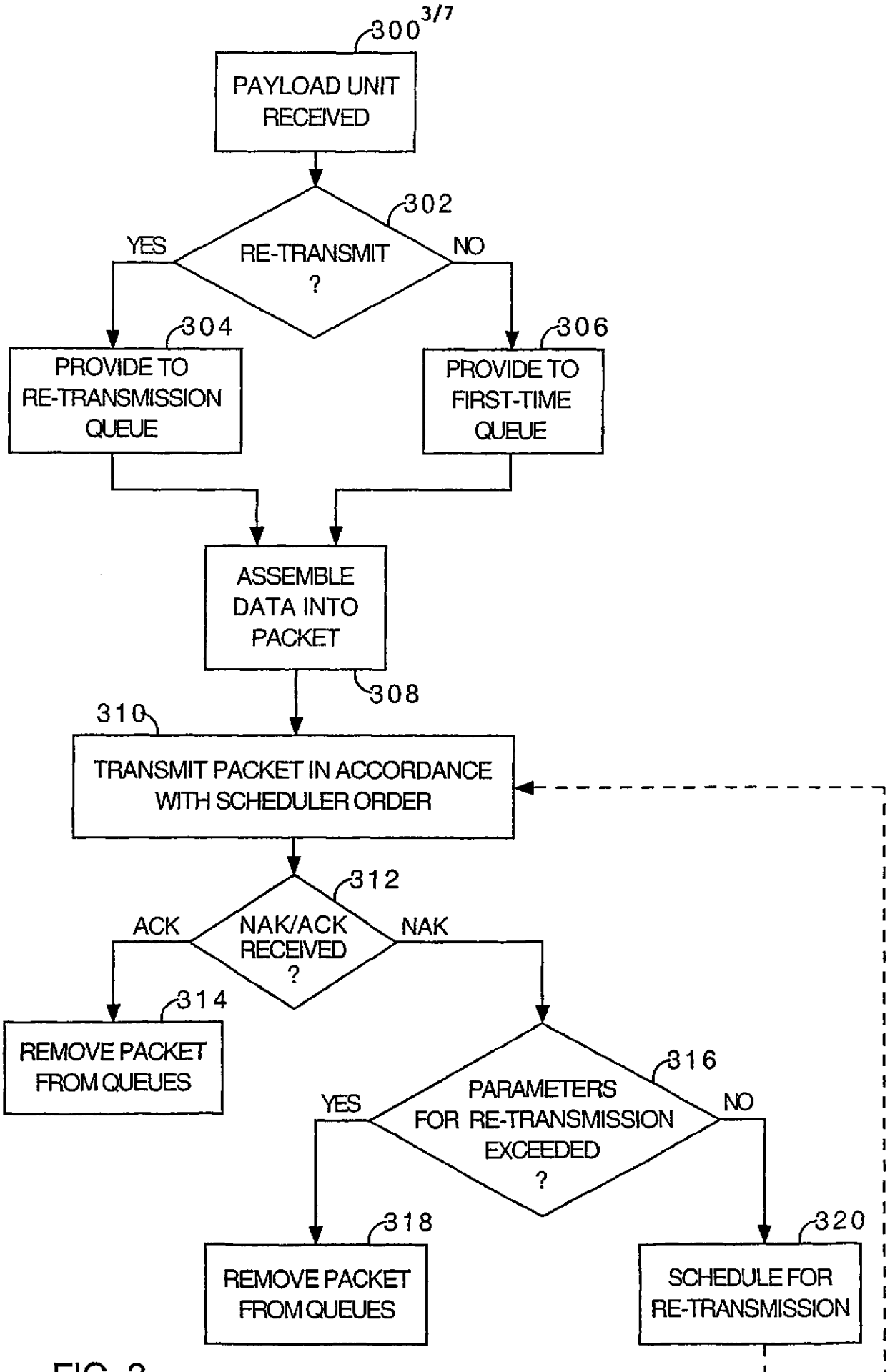

300
PAYLOAD UNIT RECEIVED
302
RE-TRANSMIT ?
YES
NO
304
PROVIDE TO RE-TRANSMISSION QUEUE
306
PROVIDE TO FIRST-TIME QUEUE
ASSEMBLE DATA INTO PACKET
308
310
TRANSMIT PACKET IN ACCORDANCE WITH SCHEDULER ORDER
312
NAK/ACK RECEIVED ?
ACK
NAK
314
REMOVE PACKET FROM QUEUES
316
PARAMETERS FOR RE-TRANSMISSION EXCEEDED ?
YES
NO
318
REMOVE PACKET FROM QUEUES
320
SCHEDULE FOR RE-TRANSMISSION

FIG. 3

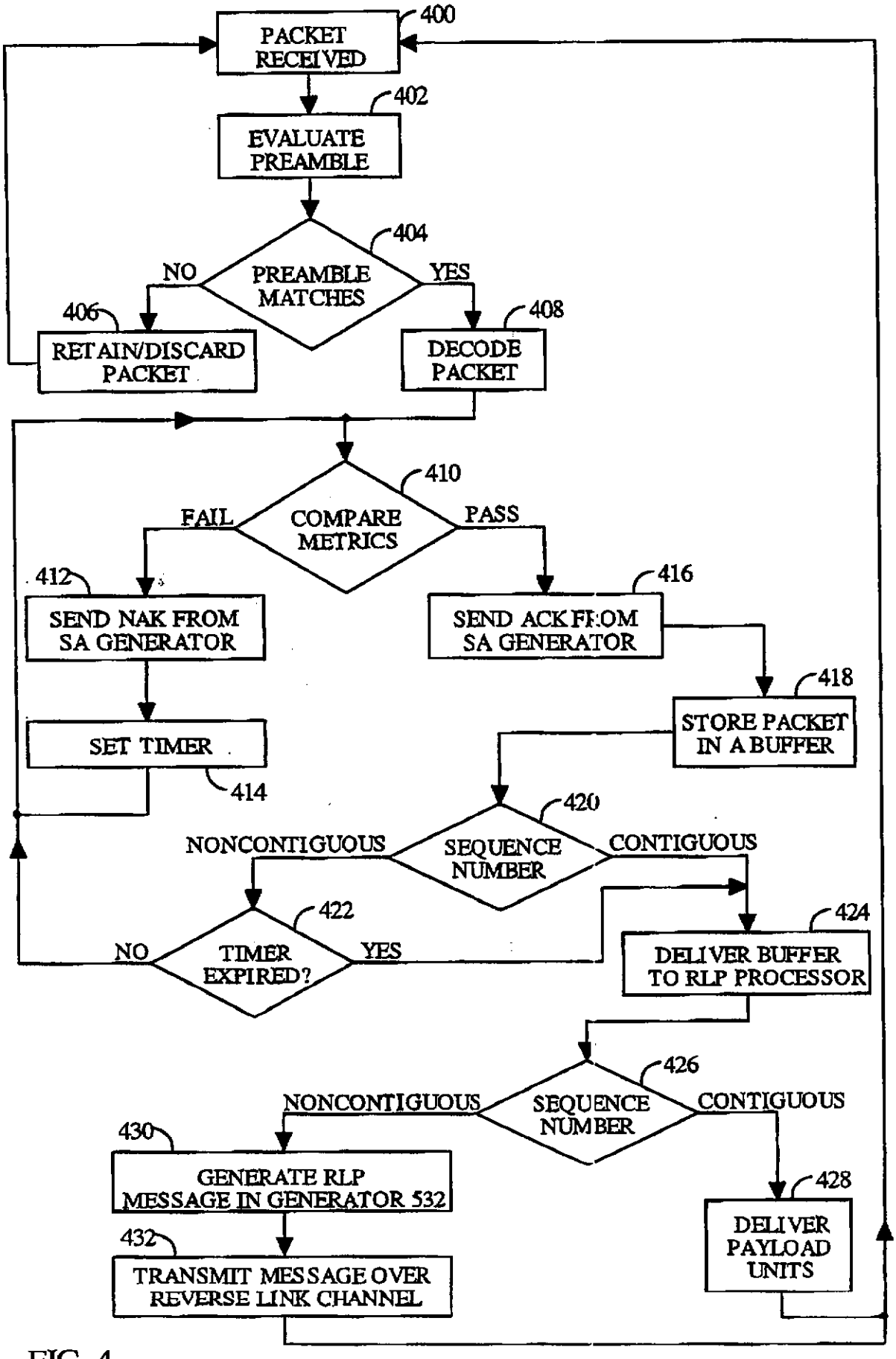

PACKET RECEIVED
400
EVALUATE PREAMBLE
402
PREAMBLE MATCHES
404
NO
YES
RETAIN/DISCARD PACKET
406
DECODE PACKET
408
COMPARE METRICS
410
FAIL
PASS
SEND NAK FROM SA GENERATOR
412
SEND ACK FROM SA GENERATOR
416
SET TIMER
414
STORE PACKET IN A BUFFER
418
SEQUENCE NUMBER
420
NONCONTIGUOUS
CONTIGUOUS
TIMER EXPIRED?
422
NO
YES
DELIVER BUFFER TO RLP PROCESSOR
424
SEQUENCE NUMBER
426
NONCONTIGUOUS
CONTIGUOUS
GENERATE RLP MESSAGE IN GENERATOR 532
430
DELIVER PAYLOAD UNITS
428
TRANSMIT MESSAGE OVER REVERSE LINK CHANNEL
432

FIG. 4

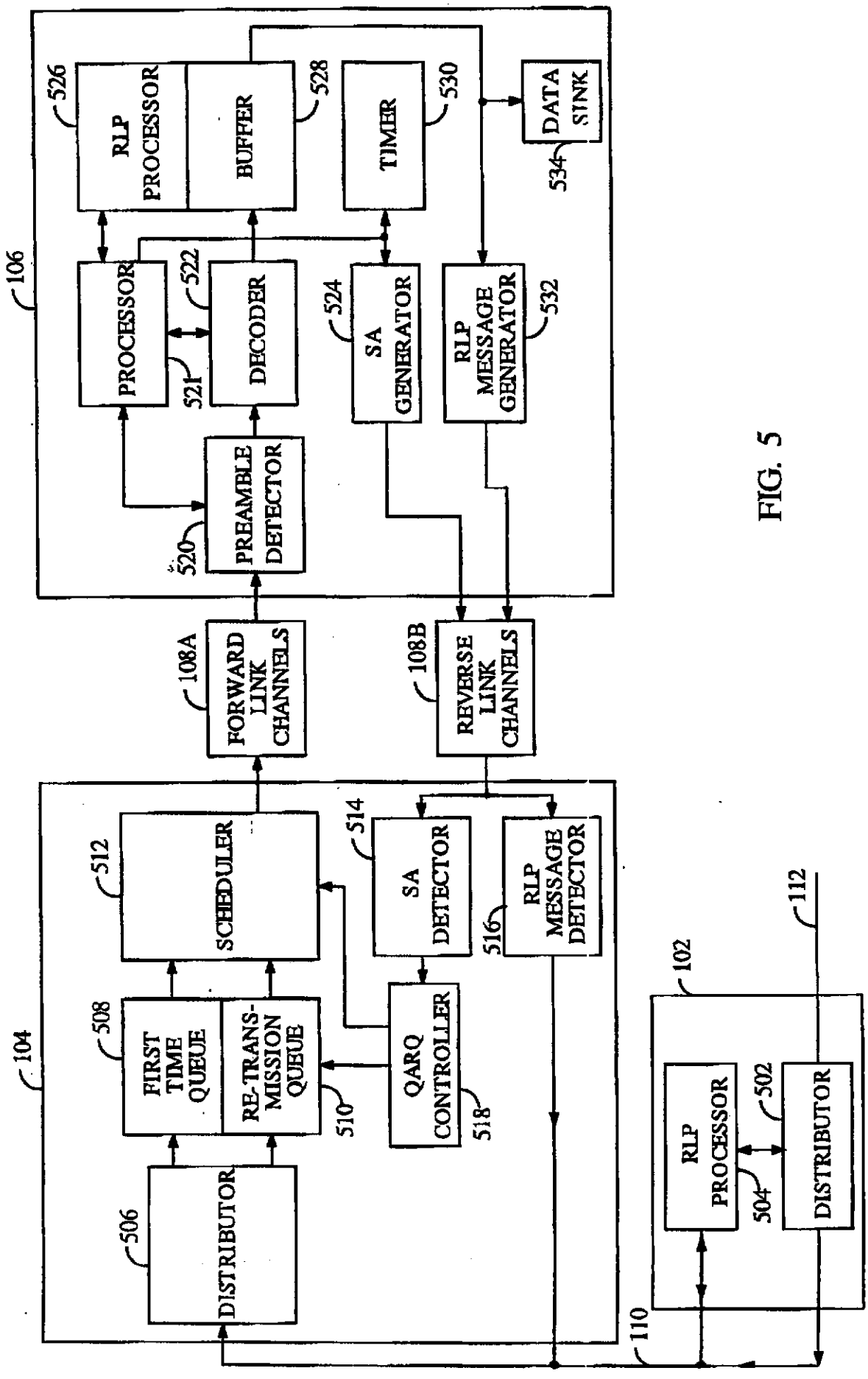

106
RLP PROCESSOR
526
BUFFER
528
TIMER
530
DATA SINK
534
PROCESSOR
521
DECODER
522
SA GENERATOR
524
RLP MESSAGE GENERATOR
532
PREAMBLE DETECTOR
520
108A
FORWARD LINK CHANNELS
108B
REVERSE LINK CHANNELS
104
SCHEDULER
512
SA DETECTOR
514
RLP MESSAGE DETECTOR
516
FIRST TIME QUEUE
508
RE-TRANS-MISSION QUEUE
510
QARQ CONTROLLER
518
DISTRIBUTOR
506
102
RLP PROCESSOR
504
DISTRIBUTOR
502
112
110

FIG. 5

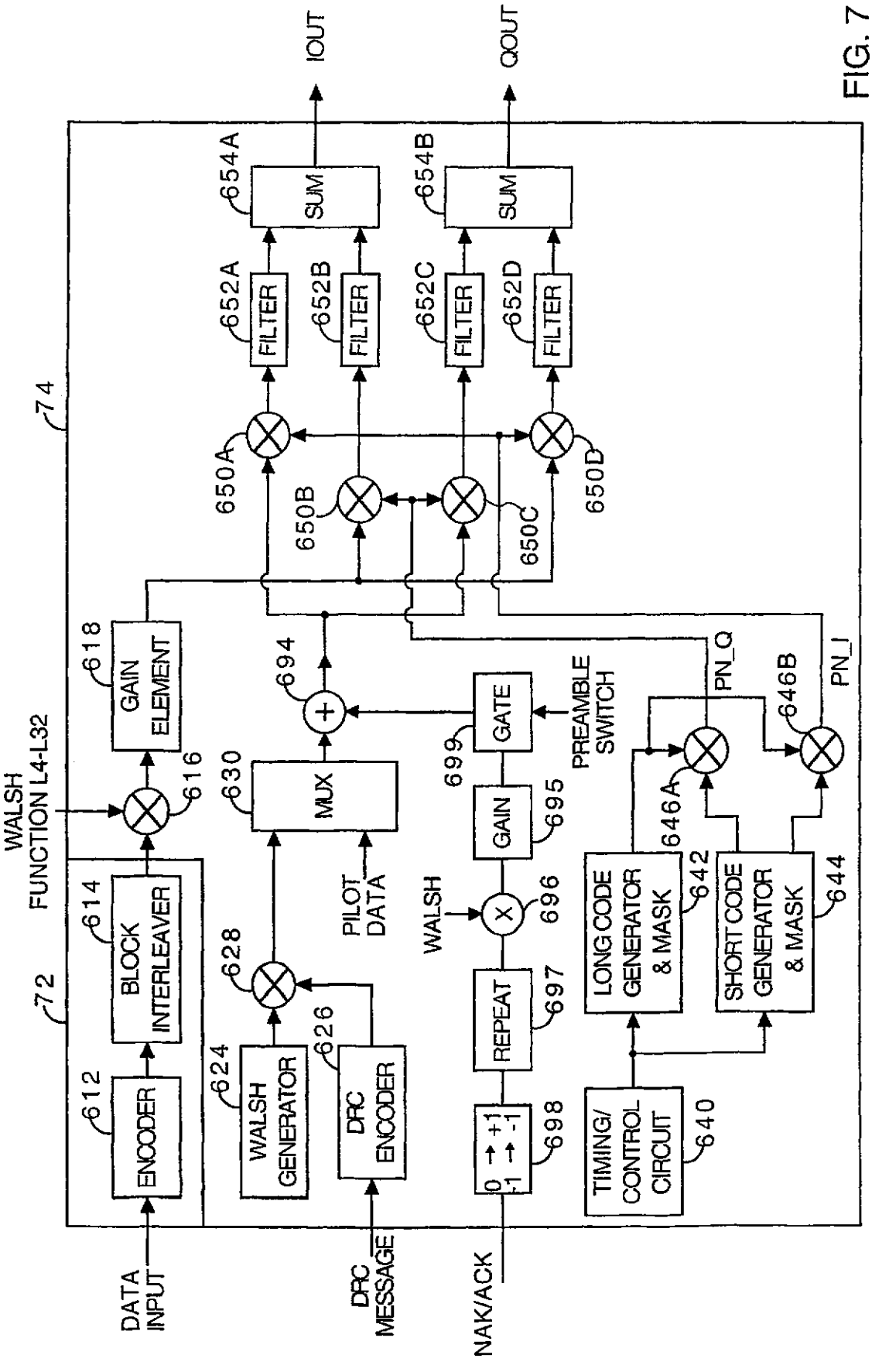

IOUT
QOUT
654A
654B
SUM
SUM
652A
652B
652C
652D
FILTER
FILTER
FILTER
FILTER
650A
650B
650C
650D
74
618
GAIN ELEMENT
694
699
GATE
PREAMBLE SWITCH
PN_Q
PN_I
646B
646A
WALSH FUNCTION L4-L32
616
630
MUX
695
GAIN
696
WALSH
697
REPEAT
698
0 → +1
-1 → -1
642
LONG CODE GENERATOR & MASK
644
SHORT CODE GENERATOR & MASK
640
TIMING/ CONTROL CIRCUIT
72
614
BLOCK INTERLEAVER
612
ENCODER
628
626
624
WALSH GENERATOR
DRC ENCODER
PILOT DATA
DATA INPUT
DRC MESSAGE
NAK/ACK

FIG. 7

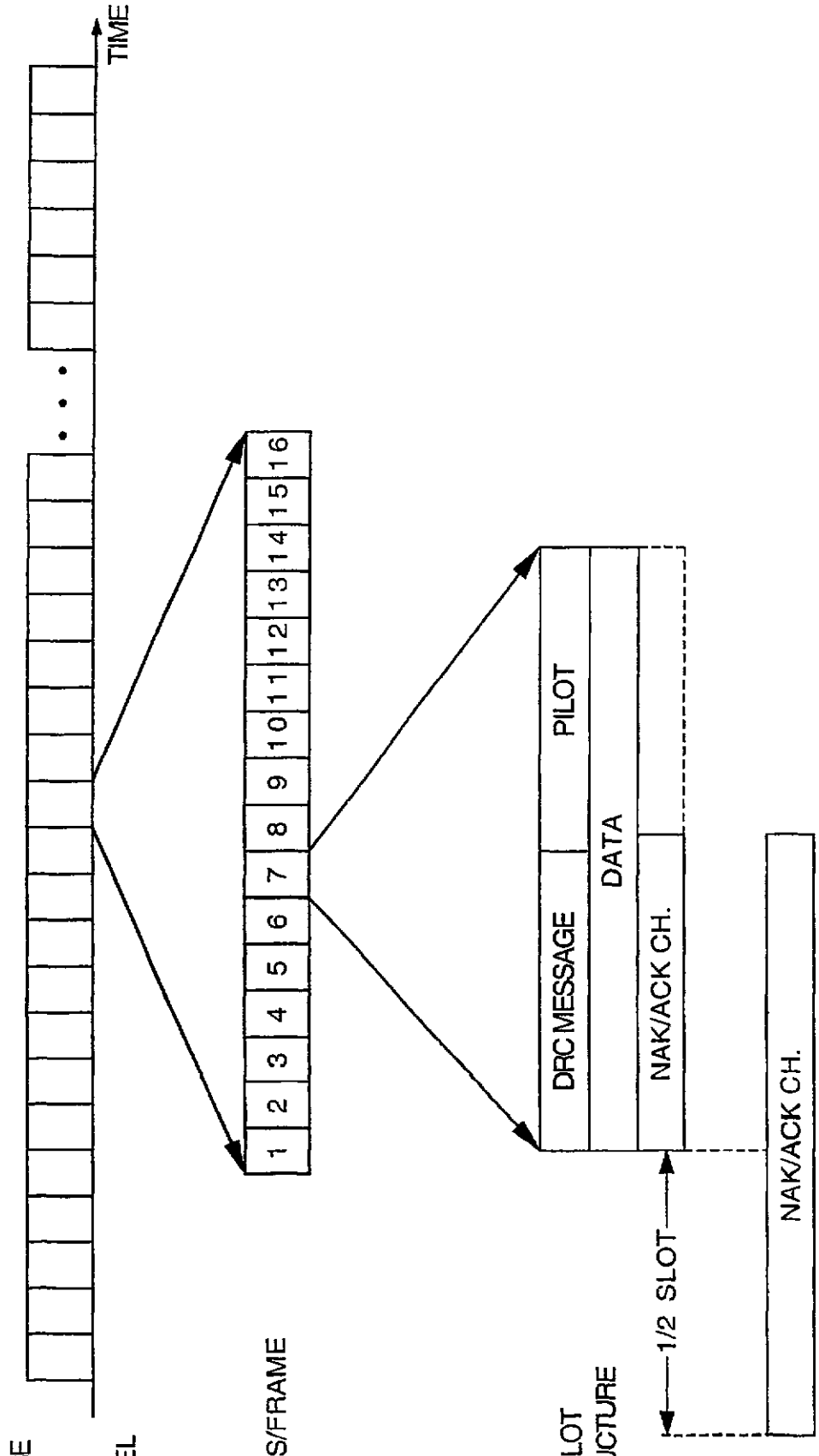

REVERSE LINK DATA CHANNEL
TIME
16 SLOTS/FRAME
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
SLOT STRUCTURE
DRC MESSAGE
PILOT
DATA
NAK/ACK CH.
1/2 SLOT
NAK/ACK CH.

FIG. 8