radiator, a beamformer supporting the radiator dilation layer, a beamformer dilation layer supporting the beamformer, and a substrate support layer supporting the beamformer dilation layer. At least one of the radiator, the radiator dilation layer, the beamformer, the beamformer dilation layer and the substrate support layer is fabricated at least in part by an AMT process.

Embodiments of the wave phased array further may include the radiator embodying a spiral antenna. The radiator further may include a vertical launch surrounding feed lines for the spiral antenna. The radiator further may include Faraday walls disposed around the feed lines and the vertical launch. The wave phased array may be configured to produce an electromagnetic signal having a frequency in the range of 24 GHz to 75 GHz. The wave phased array may be configured to produce an electromagnetic signal having a frequency of approximately 30 GHz. The radiator may have a thickness of approximately 2.4697 mmmils. The radiator dilation layer may have a thickness of approximately 0.5823 mm mils. The beamformer may have a thickness of approximately 1.3252 mmmils. The substrate support layer may embody chips and DC logic and may have a thickness of approximately 0.15 mm6 mils. The wave phase array may have a total thickness of approximately 1774.5 mm mils.

Another aspect of the present disclosure is directed to an AMT process for fabricating a wave phased array including a radiator, a radiator dilation layer supporting the radiator, a beamformer supporting the radiator dilation layer, a beamformer dilation layer supporting the beamformer, and a substrate support layer supporting the beamformer dilation layer. Embodiments of the process further may include at least one of the following: milling; conductive ink deposition; and lamination under CAD control.

BRIEF DESCRIPTION OF THE DRAWINGS

Various aspects of at least one embodiment are discussed below with reference to the accompanying figures, which are not intended to be drawn to scale. The figures are included to provide illustration and a further understanding of the various aspects and embodiments, and are incorporated in and constitute a part of this specification, but are not intended as a definition of the limits of the disclosure. In the figures, each identical or nearly identical component that is illustrated in various figures may be

using standard PCB process, which requires multiple process steps which increases cost and cycle time and restricts feature size and precision. The multi-step process is a significant cost driver for both terrestrial- and space-based phased arrays. Conductive vias are used for mode suppression and tuning, which require higher density ground via fields. Ground via fields and fences are generally not effective, and cause leakage or coupling between radio frequency (RF) circuits. This leads to complex rules to maintain adequate RF isolation and produces long and risky development cycles.

Referring to FIG. 6, a radiator that is fabricated using AMT techniques is generally indicated at 60. As shown, the radiator 60 includes miniaturized features having 0.05two to 0.08three mmmil trace widths and vertical transition vias having a maximum depth of 2.0380 mmmils. The radiator includes a spiral antenna 62 to provide circular polarization, having 3 GHz radar bandwidth and good scan performance. In the shown example, all radiator boundary conditions use AMT process, having high conductivity copper in high current areas and small geometric features. The radiator 60 includes printed vertical-launch feature 64 and Faraday walls 66.

In one embodiment, the spiral antenna 62 of the radiator 60 includes a spiral antenna portion coupled to a feed circuit portion. The spiral antenna portion includes an antenna substrate having two or more spiral conductors disposed or otherwise formed on a surface of the antenna substrate. Each of the spiral conductors has an inner end which defines an inner radius of the spiral and an outer end which defines an outer radius of the spiral. It should be appreciated that, depending upon the particular type of spiral antenna, the spacing and width may change at different points along the spiral.

The vertical launch feature 64 of the radiator 60 is disposed between a first ground plane of a stripline feed circuit substrate and the surface of the antenna substrate and surrounds (i.e., encompasses) vertical launch feed lines. In preferred embodiments, the vertical launch feature 64 is provided having a solid shape. In embodiments, it may be possible to provide a wall having gaps, slots or other forms of openings provided therein. In embodiments, one end of the vertical launch feature is in electrical contact with a feed circuit ground plane and a second opposite end of the vertical launch feature extends through the antenna substrate, but does not extend to the antenna substrate surface.

In embodiments, the Faraday wall 66 may or may not be in physical contact with a second ground plane. Such a conductive Faraday wall 66 confines electric fields to thus provide isolation and mode suppression. The vertical launch feature 64 and the Faraday wall 66 thus serves as a vertical launch isolation and mode suppression structure and thereby aids in providing the spiral antenna 62 with desired antenna operating characteristics.

In certain embodiments, antenna elements may be grouped together into a subarray and fed together in a phase-controlled manner to generate a beam characteristics of an antenna larger than that of any single antenna element. A beamformer can include a beam port and a plurality of element ports. In a transmit mode, the signal to be transmitted is applied to the beam port and is distributed by the beamformer to the various element ports. In the receive mode, the unguided electromagnetic signals received by the antenna elements and coupled in guided form to the element ports are combined to produce a beam signal at the beam port of the beamformer.

Referring to FIG. 7, a wave phased array block diagram concept is generally indicated at 70. As shown, the array block diagram concept 70 sets out a logical organization of the array components. A hierarchical structure of the array block diagram concept includes a panel, which functions as an array building block, a subarray, which functions as a panel building block, and a unit cell, which functions as the smallest functional unit. In one conceptual model, the wave phased array block diagram concept 70 is configured to include: single circular polarization, switched Tx/Rx path, half-duplex array operation, unit cell phase and amplitude control, and 8 x 8 subarray building block.

Referring to FIG. 8, an exemplary wave phased array structure profile is generally indicated at 80. As shown, the structure 80 includes a radiator 81, a radiator dilation layer 82, a beamformer 83, a beamformer dilation layer 84 and a chip and DC logic layer 85. The constituent parts of the structure 80 are shown in FIG. 9. In one embodiment, the radiator 81 has a thickness of 2.4797.1 mmmils, the radiator dilation 82 has a thickness of 0.5822.7 mmmils, the beamformer 83 has a thickness of 1.3151.7

mmmils and the chip and DC logic layer 85, sometimes referred to as the substrate support layer, has a thickness of 0.145.7 mmmils.

In the shown embodiment, the radiator 81 includes (a) a conductive spiral antenna (radiator) fabricated from copper that is 0.020.7 mmmils thick, (b) a radiator feed substrate purchased from Rogers under model RT/Duroid 5880 (PTFE/Glass) that is 1.8573 mmmils thick, (c) a radiator feed ground fabricated from copper that is 0.020.7 mmmils thick, (d) a radiator bond film purchased from Rogers under model 3001 Bonding Film that is 0.03 1 mmmil thick, (e) a radiator substrate upper layer purchased from Rogers under model RO3003 (ceramic/PTFE) that is 0.2510 mmmils thick, (f) a radiator bond film purchased from Rogers under model 3001 Bonding Film that is 0.031 mmmil thick, (g) a radiator substrate lower layer purchased from Rogers under model RO3003 (ceramic/PTFE), and (h) a radiator ground fabricated from copper that is 0.020.7 mmmils thick. The overall thickness of the radiator is 2.4797.1 mmmils thick.

In the shown embodiment, the radiator dilation layer 82 includes (a) a dilation bond film purchased from Rogers under model 3001 Bonding Film that is 0.031 mmmil thick, (b) a dilation substrate upper layer purchased from Rogers under model RT/Duroid 6006 (ceramic/PTFE) that is 0.2510 mmmils thick, (c) a dilation bond film purchased from Rogers under model 3001 Bonding Film that is 0.031 mmmil thick, (d) a dilation substrate lower layer purchased from Rogers under model RT/Duroid 6006 (ceramic/PTFE) that is 0.2510 mmmils thick, and (e) a dilation ground fabricated from copper that is 0.020.7 mmmils thick. The overall thickness of the dilation later is 0.5822.7 mmmils thick.

In the shown embodiment, the beamformer 83 includes (a) a beamformer bonding film purchased from Rogers under model 3001 Bonding Film that is 0.031 mmmil thick, (b) a beamformer substrate purchased from Taconic under model CER10 (ceramic/PTFE), and (c) a beamformer ground fabricated from copper that is 0.020.7 mmmils thick. The overall thickness of the beamformer 83, including the beamformer dilation layer 84, is 1.3151.7mm mils thick.

In the shown embodiment, the chip and DC logic layer 85 includes DC and logic bond film purchased from Rogers under model 3001 Bonding Film that is 0.031 mmmil thick, (b) DC and logic substrate fabricated from glass-reinforced epoxy laminate

material (FR-4) that is 0.14 mmmils thick, and (c) a DC and logic trace layer fabricated from copper that is 0.020.7 mmmils thick. The overall thickness of the DC and logic layer is 0.145.7 mmmils thick.

Accordingly, the overall thickness of the wave phased array structure 80 is 4.5177.2 mmmils thick. In addition, by employing the various techniques and methods disclosed herein, the thickness, complexity and costs of fabricating the wave phased array structure is reduced.

Referring to FIG. 10, the conductive spiral antenna of the radiator is generally indicated at 100. In one embodiment, the radiator 100 includes a spiral conductor, a central feed transmission line, and a circuit distribution provided in a cavity geometry. Other radiator designs can readily be implemented.

Referring to FIG. 11, the spiral antenna ground is generally indicated at 110. Archimedes or equiangular spiral geometry with open circuit terminations may be employed.

Referring to FIG. 12, the feed network is generally indicated at 120. The feed circuit introduces impedance matching and transfers the circuit to the active components.

Referring to FIG. 13, the feed network ground is generally indicated at 130.

Referring to FIG. 14, the radiator dilation layer is generally indicated at 140.

Referring to FIG. 15-17, the radiator dilation trace layer is indicated at 150.

Referring to FIG. 18, the radiator dilation ground is generally indicated at 180.

Referring to FIG. 19, the beamformer dilation layer is generally indicated at 190.

Referring to FIG. 20, the beamformer dilation ground is generally indicated at 200. The dilation circuit translates from the radiator to the active circuit geometry, using general transmission line theory.

Referring to FIG. 21, the chip layout is generally indicated at 210.

Referring to FIG. 22, the wave phased array antenna has a plurality of spiral radiators, each indicated at 220. In one embodiment, the spiral radiators 220 are spaced apart 5.18 mm from one another (center-to-center distance). The antenna is configured to operate in a 24-28 GHz operating ban, with 60-degree conical scan volume and single circular polarization. The array is composed of lattice of the radiating

CLAIMS

1. A wave phased array manufactured using additive manufacturing technology (AMT), the wave phased array comprising:

a radiator including a spiral antenna;

a radiator dilation layer supporting the radiator;

a beamformer supporting the radiator dilation layer;

a beamformer dilation layer supporting the beamformer; and

a substrate support layer supporting the beamformer dilation layer,

wherein at least one of the radiator, the radiator dilation layer, the beamformer, the beamformer dilation layer and the substrate support layer is fabricated at least in part by an AMT process, and

wherein the radiator further includes a vertical launch surrounding feed lines for the spiral antenna and Faraday walls disposed around the feed lines and the vertical launch.

~~2. The wave phased array of claim 1, wherein the radiator includes a spiral antenna.~~

~~3. The wave phased array of claim 2, wherein the radiator further includes a vertical launch surrounding feed lines for the spiral antenna.~~

~~4. The wave phased array of claim 3, wherein the radiator further includes Faraday walls disposed around the feed lines and the vertical launch.~~

2~~5~~. The wave phased array of claim 1~~4~~, wherein the wave phased array is configured to produce an electromagnetic signal having a frequency in the range of 24 GHz to 75 GHz.

36. The wave phased array of claim 14, wherein the wave phased array is configured to produce an electromagnetic signal having a frequency of approximately 30 GHz.

47. The wave phased array of claim 1, wherein the radiator has a thickness of approximately 2.4697 mmmils.

58. The wave phased array of claim 47, wherein the radiator dilation layer has a thickness of approximately 0.5823 mmmils.

69. The wave phased array of claim 58, wherein the beamformer has a thickness of approximately 1.3252 mmmils.

710. The wave phased array of claim 69, wherein the substrate support layer embodies chips and DC logic and has a thickness of approximately 0.156 mmmils.

811. The wave phased array of claim 1, wherein the wave phase array has a total thickness of approximately 4.5177 mmmils.

9. The wave phased array of claim 1, wherein the at least one of the radiator, radiator dilation layer, the beamformer, the beamformer dilation layer and the substrate is created by removing material by milling to create a void and depositing conductive ink to fill the void.

1012. An AMT process for fabricating thea wave phased array of claim 1 including a radiator, a radiator dilation layer supporting the radiator, a beamformer supporting the radiator dilation layer, a beamformer dilation layer supporting the beamformer, and a substrate support layer supporting the beamformer dilation layer.

1113. The process of claim 1012, wherein process steps include at least one of the following: milling; conductive ink deposition; and lamination under CAD control.

1214. The process of claim 1012, wherein the wave phased array is configured to produce an electromagnetic signal having a frequency in the range of 24 GHz to 75 GHz.

1315. The process of claim 1012, wherein the wave phased array is configured to produce an electromagnetic signal having a frequency of approximately 30 GHz.

1416. The process of claim 1012, wherein the radiator has a thickness of approximately 2.4697 mmmils.

1517. The process of claim 1416, wherein the radiator dilation layer has a thickness of approximately 0.5823 mmmils.

1618. The process of claim 1517, wherein the beamformer has a thickness of approximately 1.3252 mmmils.

1719. The process of claim 1618, wherein the substrate support layer embodies chips and DC logic and has a thickness of approximately 0.156 mmmils.