CLAIMS

What is claimed is:

1. A configuration information indication method, comprising:

receiving an uplink-downlink time division duplex TDD configuration from a network device, the uplink-downlink TDD configuration comprises a quantity of TDD patterns and a TDD pattern periodicity; and

sending indication information to a second terminal device based on the uplink-downlink TDD configuration, the indication information comprises a first bit sequence, a first part of bits in the first bit sequence indicate the quantity of TDD patterns, and a second part of bits in the first bit sequence indicate the TDD pattern periodicity.

2. The method according to claim 1, wherein

the indication information indicates that the quantity of the TDD patterns is 1 or 2, and the TDD pattern periodicity comprises a periodicity of each of the one or two TDD patterns.

3. The method according to claim 1 or 2, wherein

the indication information indicates that the quantity of TDD patterns is 1, the TDD pattern is a pattern 1, and the second part of bits in the first bit sequence indicate the periodicity of the pattern 1 by using the following table:

Number	Periodicity (ms)
0	0.5
1	0.625
2	1
3	1.25
4	2
5	2.5

wherein the number is an index corresponding to the periodicity of the pattern 1, and the second part of bits in the first bit sequence indicate the number.

4. The method according to claim 1 or 2, wherein

the indication information indicates that the quantity of TDD patterns is 2, the TDD patterns are a pattern 1 and a pattern 2, and the second part of bits in the first bit sequence indicate an index corresponding to a periodicity combination of a first periodicity *P* of the pattern 1 and a second periodicity P_2 of the pattern 2, wherein

the second part of bits in the first bit sequence indicate a number of the index is 0, the first periodicity *P* is 0.5ms and the second periodicity P_2 is 0.5ms,

the second part of bits in the first bit sequence indicate a number of the index is 1, the first periodicity *P* is 0.625ms and the second periodicity P_2 is 0.625ms,

the second part of bits in the first bit sequence indicate a number of the index is 2, the first periodicity *P* is 1ms and the second periodicity P_2 is 1ms,

the second part of bits in the first bit sequence indicate a number of the index is 3, the first periodicity *P* is 0.5ms and the second periodicity P_2 is 2ms,

the second part of bits in the first bit sequence indicate a number of the index is 4, the first periodicity *P* is 1.25ms and the second periodicity P_2 is 1.25ms,

the second part of bits in the first bit sequence indicate a number of the index is 5, the first periodicity *P* is 2ms and the second periodicity P_2 is 0.5ms,

the second part of bits in the first bit sequence indicate a number of the index is 6, the first periodicity *P* is 1ms and the second periodicity P_2 is 3ms,

the second part of bits in the first bit sequence indicate a number of the index is 7, the first periodicity *P* is 2ms and the second periodicity P_2 is 2ms,

the second part of bits in the first bit sequence indicate a number of the index is 8, the first periodicity *P* is 3ms and the second periodicity P_2 is 1ms,

the second part of bits in the first bit sequence indicate a number of the index is 9, the first periodicity *P* is 1ms and the second periodicity P_2 is 4ms,

the second part of bits in the first bit sequence indicate a number of the index is 10, the first periodicity *P* is 2ms and the second periodicity P_2 is 3ms,

the second part of bits in the first bit sequence indicate a number of the index is 11, the first periodicity *P* is 2.5ms and the second periodicity P_2 is 2.5ms,

the second part of bits in the first bit sequence indicate a number of the index is 12, the first periodicity *P* is 3ms and the second periodicity P_2 is 2ms,

the second part of bits in the first bit sequence indicate a number of the index is 13, the first

periodicity P is 4ms and the second periodicity P_2 is 1ms,

the second part of bits in the first bit sequence indicate a number of the index is 14, the first periodicity P is 5ms and the second periodicity P_2 is 5ms, or

the second part of bits in the first bit sequence indicate a number of the index is 15, the first periodicity P is 10ms and the second periodicity P_2 is 10ms.

5. The method according to any one of claims 1 to 4, wherein

the first part of bits in the first bit sequence are 1 bit, a value 0 of the first part of bits indicates that the quantity of TDD patterns is 1, and a value 1 of the first part of bits indicates that the quantity of TDD patterns is 2.

6. The method according to any one of claims 1 to 5, wherein

the second part of bits in the first bit sequence are 4 bits.

7. The method according to any one of claims 1 to 6, wherein the indication information comprises a second bit sequence, the second bit sequence indicates uplink UL transmission duration in the TDD pattern periodicity.

8. The method according to claim 7, wherein

the second bit sequence is 7 bits.

9. The method according to claim 7 or 8, wherein the quantity of TDD patterns comprised in the uplink-downlink TDD configuration is 1, the second bit sequence indicates UL transmission duration in the periodicity of the TDD pattern; or

the quantity of TDD patterns comprised in the uplink-downlink TDD configuration is 2, the second bit sequence indicates UL transmission duration in the periodicity of each of the two TDD patterns.

10. The method according to any one of claims 7 to 9, wherein

the quantity of TDD patterns comprised in the uplink-downlink TDD configuration is 1, the second bit sequence is a binary representation of a quantity of slots that corresponds to the UL transmission duration; or

the quantity of TDD patterns comprised in the uplink-downlink TDD configuration is 2, the second bit sequence indicates a quantity of slots that corresponds to the UL transmission duration in the periodicity of each TDD pattern.

11. The method according to any one of claims 7 to 10, wherein

the indication information is carried on a physical sidelink broadcast channel PSBCH of a

sidelink synchronization signal block S-SSB,

the UL transmission duration in the TDD pattern periodicity is related to a ratio of a subcarrier spacing SCS of the S-SSB to a reference SCS comprised in the uplink-downlink TDD configuration.

12. The method according to claim 11, wherein

the subcarrier spacing SCS of the S-SSB is an SCS configured on a sidelink bandwidth part BWP.

13. The method according to any one of claims 1 to 10, wherein

the indication information is carried on a physical sidelink broadcast channel PSBCH of a sidelink synchronization signal block, S-SSB.

14. A configuration information indication method, comprising:

receiving indication information from a first terminal device, wherein the indication information comprises a first bit sequence, a first part of bits in the first bit sequence indicates a quantity of TDD patterns, and a second part of bits in the first bit sequence indicates a TDD pattern periodicity; and

determining the quantity of TDD patterns and the TDD pattern periodicity based on the indication information.

15. The method according to claim 14, wherein

the indication information indicates that the quantity of the TDD patterns is 1 or 2, and the TDD pattern periodicity comprises a periodicity of each of the one or two TDD patterns.

16. The method according to claim 14 or 15, wherein

the indication information indicates that the quantity of TDD patterns is 1, the TDD pattern is a pattern 1, and the second part of bits in the first bit sequence indicate the periodicity of the pattern 1 by using the following table:

Number	Periodicity (ms)
0	0.5
1	0.625
2	1

3	1.25
4	2
5	2.5

wherein the number is an index corresponding to the periodicity of the pattern 1, and the second part of bits in the first bit sequence are used to indicate the number.

17. The method according to claim 14 or 15, wherein

the indication information indicates that the quantity of TDD patterns is 2, the TDD patterns are a pattern 1 and a pattern 2, and the second part of bits in the first bit sequence indicate an index corresponding to a periodicity combination of a first periodicity P of the pattern 1 and a second periodicity P_2 of the pattern 2, wherein

the second part of bits in the first bit sequence indicate a number of the index is 0, the first periodicity P is 0.5ms and the second periodicity P_2 is 0.5ms,

the second part of bits in the first bit sequence indicate a number of the index is 1, the first periodicity P is 0.625ms and the second periodicity P_2 is 0.625ms,

the second part of bits in the first bit sequence indicate a number of the index is 2, the first periodicity P is 1ms and the second periodicity P_2 is 1ms,

the second part of bits in the first bit sequence indicate a number of the index is 3, the first periodicity P is 0.5ms and the second periodicity P_2 is 2ms,

the second part of bits in the first bit sequence indicate a number of the index is 4, the first periodicity P is 1.25ms and the second periodicity P_2 is 1.25ms,

the second part of bits in the first bit sequence indicate a number of the index is 5, the first periodicity P is 2ms and the second periodicity P_2 is 0.5ms,

the second part of bits in the first bit sequence indicate a number of the index is 6, the first periodicity P is 1ms and the second periodicity P_2 is 3ms,

the second part of bits in the first bit sequence indicate a number of the index is 7, the first periodicity P is 2ms and the second periodicity P_2 is 2ms,

the second part of bits in the first bit sequence indicate a number of the index is 8, the first periodicity P is 3ms and the second periodicity P_2 is 1ms,

the second part of bits in the first bit sequence indicate a number of the index is 9, the first

periodicity P is 1ms and the second periodicity P_2 is 4ms,

the second part of bits in the first bit sequence indicate a number of the index is 10, the first periodicity P is 2ms and the second periodicity P_2 is 3ms,

the second part of bits in the first bit sequence indicate a number of the index is 11, the first periodicity P is 2.5ms and the second periodicity P_2 is 2.5ms,

the second part of bits in the first bit sequence indicate a number of the index is 12, the first periodicity P is 3ms and the second periodicity P_2 is 2ms,

the second part of bits in the first bit sequence indicate a number of the index is 13, the first periodicity P is 4ms and the second periodicity P_2 is 1ms,

the second part of bits in the first bit sequence indicate a number of the index is 14, the first periodicity P is 5ms and the second periodicity P_2 is 5ms, or

the second part of bits in the first bit sequence indicate a number of the index is 15, the first periodicity P is 10ms and the second periodicity P_2 is 10ms.

18. The method according to any one of claims 14 to 17, wherein

the first part of bits in the first bit sequence are 1 bit, a value 0 of the first part of bits indicates that the quantity of TDD patterns is 1, and a value 1 of the first part of bits indicates that the quantity of TDD patterns is 2.

19. The method according to any one of claims 14 to 18, wherein

the second part of bits in the first bit sequence are 4 bits.

20. The method according to any one of claims 14 to 19, wherein the indication information comprises a second bit sequence, the second bit sequence indicates uplink UL transmission duration in the TDD pattern periodicity.

21. The method according to claim 20, wherein

the second bit sequence is 7 bits.

22. The method according to claim 20 or 21, wherein the quantity of TDD patterns is 1, the second bit sequence is used to indicate UL transmission duration in the periodicity of the TDD pattern; or

the quantity of TDD patterns is 2, the second bit sequence is used to indicate UL transmission duration in the periodicity of each of the two TDD patterns.

23. The method according to any one of claims 20 to 22, wherein

the quantity of TDD patterns is 1, the second bit sequence is a binary representation of a

quantity of slots that corresponds to the UL transmission duration; or

the quantity of TDD patterns is 2, the second bit sequence is used to indicate a quantity of slots that corresponds to the UL transmission duration in the periodicity of each TDD pattern.

24. The method according to any one of claims 20 to 23, wherein

the indication information is carried on a physical sidelink broadcast channel PSBCH of a sidelink synchronization signal block S-SSB, and the UL transmission duration in the TDD pattern periodicity is related to a ratio of a subcarrier spacing SCS of the S-SSB to a reference SCS.

25. The method according to claim 24, wherein

the subcarrier spacing SCS of the S-SSB is an SCS configured on a sidelink bandwidth part BWP.

26. The method according to any one of claims 14 to 23, wherein

the indication information is carried on a physical sidelink broadcast channel (PSBCH) of a sidelink synchronization signal block (S-SSB).

27. A configuration information indication apparatus, comprising:

a receiving module, configured to receive an uplink-downlink time division duplex TDD configuration from a network device, the uplink-downlink TDD configuration comprises a quantity of TDD patterns and a TDD pattern periodicity; and

a sending module, configured to send indication information to a second terminal device based on the uplink-downlink TDD configuration, the indication information comprises a first bit sequence, a first part of bits in the first bit sequence indicate the quantity of TDD patterns, and a second part of bits in the first bit sequence indicate the TDD pattern periodicity.

28. The apparatus according to claim 27, wherein

the indication information indicates that the quantity of the TDD patterns is 1 or 2, and the TDD pattern periodicity comprises a periodicity of each of the one or two TDD patterns.

29. The apparatus according to claim 27 or 28, wherein

the indication information indicates that the quantity of TDD patterns is 1, the TDD pattern is a pattern 1, and the second part of bits in the first bit sequence indicate the periodicity of the pattern 1 by using the following table:

Number	Periodicity (ms)
0	0.5
1	0.625
2	1
3	1.25
4	2
5	2.5

wherein the number is an index corresponding to the periodicity of the pattern 1, and the second part of bits in the first bit sequence indicate the number.

30. The apparatus according to claim 27 or 28, wherein

the indication information indicates that the quantity of TDD patterns is 2, the TDD patterns are a pattern 1 and a pattern 2, and the second part of bits in the first bit sequence indicate an index corresponding to a periodicity combination of a first periodicity P of the pattern 1 and a second periodicity P_2 of the pattern 2, wherein

the second part of bits in the first bit sequence indicate a number of the index is 0, the first periodicity P is 0.5ms and the second periodicity P_2 is 0.5ms,

the second part of bits in the first bit sequence indicate a number of the index is 1, the first periodicity P is 0.625ms and the second periodicity P_2 is 0.625ms,

the second part of bits in the first bit sequence indicate a number of the index is 2, the first periodicity P is 1ms and the second periodicity P_2 is 1ms,

the second part of bits in the first bit sequence indicate a number of the index is 3, the first periodicity P is 0.5ms and the second periodicity P_2 is 2ms,

the second part of bits in the first bit sequence indicate a number of the index is 4, the first periodicity P is 1.25ms and the second periodicity P_2 is 1.25ms,

the second part of bits in the first bit sequence indicate a number of the index is 5, the first periodicity P is 2ms and the second periodicity P_2 is 0.5ms,

the second part of bits in the first bit sequence indicate a number of the index is 6, the first periodicity P is 1ms and the second periodicity P_2 is 3ms,

the second part of bits in the first bit sequence indicate a number of the index is 7, the first

periodicity P is 2ms and the second periodicity P_2 is 2ms,

the second part of bits in the first bit sequence indicate a number of the index is 8, the first periodicity P is 3ms and the second periodicity P_2 is 1ms,

the second part of bits in the first bit sequence indicate a number of the index is 9, the first periodicity P is 1ms and the second periodicity P_2 is 4ms,

the second part of bits in the first bit sequence indicate a number of the index is 10, the first periodicity P is 2ms and the second periodicity P_2 is 3ms,

the second part of bits in the first bit sequence indicate a number of the index is 11, the first periodicity P is 2.5ms and the second periodicity P_2 is 2.5ms,

the second part of bits in the first bit sequence indicate a number of the index is 12, the first periodicity P is 3ms and the second periodicity P_2 is 2ms,

the second part of bits in the first bit sequence indicate a number of the index is 13, the first periodicity P is 4ms and the second periodicity P_2 is 1ms,

the second part of bits in the first bit sequence indicate a number of the index is 14, the first periodicity P is 5ms and the second periodicity P_2 is 5ms, or

the second part of bits in the first bit sequence indicate a number of the index is 15, the first periodicity P is 10ms and the second periodicity P_2 is 10ms.

31. The apparatus according to any one of claims 27 to 30, wherein

the first part of bits in the first bit sequence are 1 bit, a value 0 of the first part of bits indicates that the quantity of TDD patterns is 1, and a value 1 of the first part of bits indicates that the quantity of TDD patterns is 2.

32. The apparatus according to any one of claims 27 to 31, wherein

the second part of bits in the first bit sequence are 4 bits.

33. The apparatus according to any one of claims 27 to 32, wherein the indication information comprises a second bit sequence, the second bit sequence indicates uplink UL transmission duration in the TDD pattern periodicity.

34. The apparatus according to claim 33, wherein

the second bit sequence is 7 bits.

35. The apparatus according to claim 33 or 34, wherein the quantity of TDD patterns comprised in the uplink-downlink TDD configuration is 1, the second bit sequence is used to indicate UL transmission duration in the periodicity of the TDD pattern; or

the quantity of TDD patterns comprised in the uplink-downlink TDD configuration is 2, the second bit sequence is used to indicate UL transmission duration in the periodicity of each of the two TDD patterns.

36. The apparatus according to any one of claims 33 to 35, wherein

the quantity of TDD patterns comprised in the uplink-downlink TDD configuration is 1, the second bit sequence is a binary representation of a quantity of slots that corresponds to the UL transmission duration; or

the quantity of TDD patterns comprised in the uplink-downlink TDD configuration is 2, the second bit sequence is used to indicate a quantity of slots that corresponds to the UL transmission duration in the periodicity of each TDD pattern.

37. The apparatus according to any one of claims 33 to 36, wherein

the indication information is carried on a physical sidelink broadcast channel PSBCH of a sidelink synchronization signal block S-SSB, and the UL transmission duration in the TDD pattern periodicity is related to a ratio of a subcarrier spacing SCS of the S-SSB to a reference SCS comprised in the uplink-downlink TDD configuration.

38. The apparatus according to claim 37, wherein

the subcarrier spacing SCS of the S-SSB is an SCS configured on a sidelink bandwidth part BWP.

39. The apparatus according to any one of claims 27 to 36, wherein

the indication information is carried on a physical sidelink broadcast channel (PSBCH) of a sidelink synchronization signal block (S-SSB).

40. A configuration information indication apparatus, comprising:

a receiving module, configured to receive indication information from a first terminal device, the indication information comprises a first bit sequence, a first part of bits in the first bit sequence are used to indicate the quantity of TDD patterns, and a second part of bits in the first bit sequence are used to indicate the TDD pattern periodicity; and

a processing module, configured to determine the quantity of TDD patterns and the TDD pattern periodicity based on the indication information.

41. The apparatus according to claim 40, wherein

the indication information indicates that the quantity of the TDD patterns is 1 or 2, and the TDD pattern periodicity comprises a periodicity of each of the one or two TDD patterns.

42. The apparatus according to claim 40 or 41, wherein

the indication information indicates that the quantity of TDD patterns is 1, the TDD pattern is a pattern 1, and the second part of bits in the first bit sequence indicate the periodicity of the pattern 1 by using the following table:

Number	Periodicity (ms)
0	0.5
1	0.625
2	1
3	1.25
4	2
5	2.5

wherein the number is an index corresponding to the periodicity of the pattern 1, and the second part of bits in the first bit sequence indicate the number.

43. The apparatus according to claim 40 or 41, wherein

the indication information indicates that the quantity of TDD patterns is 2, the TDD patterns are a pattern 1 and a pattern 2, and the second part of bits in the first bit sequence indicate an index corresponding to a periodicity combination of a first periodicity P of the pattern 1 and a second periodicity P_2 of the pattern 2, wherein

the second part of bits in the first bit sequence indicate a number of the index is 0, the first periodicity P is 0.5ms and the second periodicity P_2 is 0.5ms,

the second part of bits in the first bit sequence indicate a number of the index is 1, the first periodicity P is 0.625ms and the second periodicity P_2 is 0.625ms,

the second part of bits in the first bit sequence indicate a number of the index is 2, the first periodicity P is 1ms and the second periodicity P_2 is 1ms,

the second part of bits in the first bit sequence indicate a number of the index is 3, the first periodicity P is 0.5ms and the second periodicity P_2 is 2ms,

the second part of bits in the first bit sequence indicate a number of the index is 4, the first periodicity P is 1.25ms and the second periodicity P_2 is 1.25ms,

the second part of bits in the first bit sequence indicate a number of the index is 5, the first

periodicity P is 2ms and the second periodicity P_2 is 0.5ms,

the second part of bits in the first bit sequence indicate a number of the index is 6, the first periodicity P is 1ms and the second periodicity P_2 is 3ms,

the second part of bits in the first bit sequence indicate a number of the index is 7, the first periodicity P is 2ms and the second periodicity P_2 is 2ms,

the second part of bits in the first bit sequence indicate a number of the index is 8, the first periodicity P is 3ms and the second periodicity P_2 is 1ms,

the second part of bits in the first bit sequence indicate a number of the index is 9, the first periodicity P is 1ms and the second periodicity P_2 is 4ms,

the second part of bits in the first bit sequence indicate a number of the index is 10, the first periodicity P is 2ms and the second periodicity P_2 is 3ms,

the second part of bits in the first bit sequence indicate a number of the index is 11, the first periodicity P is 2.5ms and the second periodicity P_2 is 2.5ms,

the second part of bits in the first bit sequence indicate a number of the index is 12, the first periodicity P is 3ms and the second periodicity P_2 is 2ms,

the second part of bits in the first bit sequence indicate a number of the index is 13, the first periodicity P is 4ms and the second periodicity P_2 is 1ms,

the second part of bits in the first bit sequence indicate a number of the index is 14, the first periodicity P is 5ms and the second periodicity P_2 is 5ms, or

the second part of bits in the first bit sequence indicate a number of the index is 15, the first periodicity P is 10ms and the second periodicity P_2 is 10ms.

44. The apparatus according to any one of claims 40 to 43, wherein

the first part of bits in the first bit sequence are 1 bit, a value 0 of the first part of bits indicates that the quantity of TDD patterns is 1, and a value 1 of the first part of bits indicates that the quantity of TDD patterns is 2.

45. The apparatus according to any one of claims 40 to 44, wherein

the second part of bits in the first bit sequence are 4 bits.

46. The apparatus according to any one of claims 40 to 45, wherein the indication information comprises a second bit sequence, the second bit sequence indicate uplink UL transmission duration in the TDD pattern periodicity.

47. The apparatus according to claim 46, wherein

the second bit sequence is 7 bits.

48. The apparatus according to claim 46 or 47, wherein

the quantity of TDD patterns is 1, the second bit sequence indicates UL transmission duration in the periodicity of the TDD pattern; or

the quantity of TDD patterns is 2, the second bit sequence indicates UL transmission duration in the periodicity of each of the two TDD patterns.

49. The apparatus according to any one of claims 46 to 48, wherein

the quantity of TDD patterns is 1, the second bit sequence is a binary representation of a quantity of slots that corresponds to the UL transmission duration; or

the quantity of TDD patterns is 2, the second bit sequence is used to indicate a quantity of slots that corresponds to the UL transmission duration in the periodicity of each TDD pattern.

50. The apparatus according to any one of claims 46 to 49, wherein

the indication information is carried on a physical sidelink broadcast channel PSBCH of a sidelink synchronization signal block S-SSB, and the UL transmission duration in the TDD pattern periodicity is related to a ratio of a subcarrier spacing SCS of the S-SSB to a reference SCS.

51. The apparatus according to claim 50, wherein

the subcarrier spacing SCS of the S-SSB is an SCS configured on a sidelink bandwidth part BWP.

52. The apparatus according to any one of claims 40 to 49, wherein

the indication information is carried on a physical sidelink broadcast channel (PSBCH) of a sidelink synchronization signal block (S-SSB).

53. A communication apparatus, comprising a processor and a memory, wherein the memory stores a program run on the processor, and the processor implements the method according to any one of claims 1 to 13 when executing the program.

54. A communication apparatus, comprising a processor and a memory, wherein the memory stores a program run on the processor, and the processor implements the method according to any one of claims 14 to 26 when executing the program.

55. A communication apparatus, comprising a processor and an interface circuit, wherein

the interface circuit is configured to receive code instructions and transmit the code instructions to the processor; and

the processor is configured to run the code instructions to perform the method according to

any one of claims 1 to 13.

56. A communication apparatus, comprising a processor and an interface circuit, wherein

the interface circuit is configured to receive code instructions and transmit the code instructions to the processor; and

the processor is configured to run the code instructions to perform the method according to any one of claims 14 to 26.

57. A computer readable storage medium, configured to store instructions, wherein when the instructions are executed, the method according to any one of claims 1 to 13 is implemented.

58. A computer readable storage medium, configured to store instructions, wherein when the instructions are executed, the method according to any one of claims 14 to 26 is implemented.

59. A computer program, comprising instructions, wherein when the instructions are run on a computer, the method according to any one of claims 1 to 13 is implemented.

60. A computer program, comprising instructions, wherein when the instructions are run on a computer, the method according to any one of claims 14 to 26 is implemented.