

Description

The invention relates to a controlled oscillator that is used in, for example, a stereo decoder of a television apparatus.

BACKGROUND OF THE INVENTION

Typical baseband composite audio stereo signals include a main signal formed from the sum of the left and right channel signals (L+R), a pilot signal having a frequency ω_p which is greater than the maximum frequency of the (L+R) signal, and a difference signal (L-R) which is the difference between the left and right channel signals. The difference signal is in the form of a double sideband, amplitude modulated suppressed carrier centered at a frequency of twice ω_p . The pilot signal is essential for demodulating the suppressed carrier to extract the (L-R) audio information.

The demodulated (L-R) signal will nominally include a component corresponding to the pilot signal, and the maximum signal frequency of the (L+R) signal is nominally relatively close to the pilot signal frequency.

In such stereo decoder, a phase-lock-loop circuit (PLL) may be used for generating, for example, a signal at the frequency $2\omega_p$ that is synchronized to the pilot signal and that is used for demodulating the (L-R) signal.

A controllable oscillator suitable for use in such a stereo decoder is known, for example, from U.S. Patent 4,020,500 (Harwood) issued 26 April 1977. In apparatus according to U.S. 4,020,500, the phase of the output signal of the controllable oscillator is responsive to the combination of a reference signal and two complementary phase-shifted signals of differing magnitudes. These complementary phase-shifted signals are produced in respective halves of two transistor pairs. No use is made of the signal currents generated in the other halves of the transistor pairs of Harwood.

SUMMARY OF THE INVENTION

It is herein recognized that by utilizing and combining the signals from both halves of each transistor pair that, advantageously, two antiphase resultant signals can be formed, and combined in an output stage such that undesirable common mode signals which may be present can be cancelled.

In carrying out another aspect of the invention, two variable gain differential amplifiers that are constructed each using a pair of MOS transistors have corresponding gains that are controlled in accordance with a control signal. The gain of each differential amplifier is varied by a third MOS transistor that is coupled at a junction between the pair of MOS transistors that form such differential amplifier. The conductivity of the third MOS transistor varies in accordance with the control signal. By selecting a predetermined channel geometry of the third MOS transistor, for example, establishing the gain parameter of the variable gain amplifier is, advantageously, simplified.

In accordance with a further aspect of the invention, a crystal having a narrow band width that is coupled in the regenerative feedback network makes the oscillator a voltage controlled crystal oscillator (VCXO). The crystal causes noise and jitter in the VCXO output signal to be, advantageously, reduced that, in turn, reduces distortions in, for example, the extracted (L-R) audio information.

In accordance with a yet further aspect of the invention, the VCXO utilizes a Pierce type arrangement in the regenerative feedback loop that, advantageously, provides signal stability.

FIGURE 1 illustrates a block diagram of a portion of a stereo decoder that includes a voltage controlled crystal oscillator, embodying an aspect of the invention;

FIGURE 2 illustrates a detailed embodiment of the oscillator of FIGURE 1;

FIGURE 3 illustrates a graph useful in explaining the operation of the circuit of FIGURE 2; and

FIGURE 4 illustrates a second detailed embodiment of the oscillator of FIGURE 1.

In FIGURE 1, a composite audio stereo signal IN_s that is obtained from, for example, an FM decoder of a television receiver, not shown in the figures, is coupled to an input terminal 109a of an analog-to-digital converter 109 that generates a composite signal IN_D . Signal IN_D is a digital representation of a signal having a frequency composition similar to the spectral waveform 5 that contains a pilot signal component PILOT. Signal component PILOT is, in the BTSC standard, at a frequency ω_p that is equal to the horizontal scan frequency, f_H .

Signal IN_D is applied via a conductor 110 to the minuend input terminal of a signal subtraction circuit 112 of a phase-lock-loop circuit (PLL) 100. A synthesized pilot signal P_s is coupled via connection 111 to the subtrahend input terminal of subtraction circuit 112. Subtraction circuit 112 provides a composite signal 112a, with the pilot signal component substantially eliminated, at its output connection 113. Subtraction

circuit 112 is included in a circuit 99 shown within the dashed-line. Circuit 99 performs the analogous function of a phase detector in a conventional PLL.

Signal 112a is also coupled to a low-pass filter 115 which passes, or separates the (L + R) signal to the substantial exclusion of higher frequency components of the composite signal. Since the pilot signal component is not present in the signal applied to filter 115, the frequency cut off characteristics of filter 115 are, advantageously, significantly less critical than if the pilot signal component were present.

Output signal 112a from subtraction circuit 112 is, additionally, coupled to one input of a multiplier circuit 120 that is included in circuit 99. The output developed by the multiplier 120 is coupled to serially coupled circuit elements including an arrangement 122, a digital-to-analog converter 123, a voltage controlled crystal oscillator (VCXO) 124, embodying an aspect of the invention, a sinewave generator circuit 126 and a 90° phase shifter 128. Arrangement 122 includes a low-pass filter 122 and an error accumulator that is not shown in the Figures.

Low-pass filter 122 of arrangement 122, having a cutoff frequency that is substantially lower than that of pilot signal component PILOT, low-pass filters the digital output words at a port 120a of multiplier 120 to produce an error word, not shown in FIGURE 1, that is representative of a phase or of a frequency error between signal component PILOT and an output signal CK of VCXO 124, as described later on. Such digital error word is then periodically accumulated in the error accumulator of arrangement 122, that is not shown in the FIGURES, every, for example, 2/3 of the period of pilot signal component PILOT, to produce a frequency control word 122a that contains the periodically accumulated error. Word 122a is converted in a digital-to-analog converter 123 that produces an equivalent, analog signal 123a that remains substantially constant between the above-mentioned periodic accumulation intervals. Signal 123a is coupled to an input terminal of VCXO 124 to establish the output frequency produced thereby.

For a zero average value of the signal at port 120a of multiplier 120, VCXO 124 develops output signal CK having a frequency that is substantially equal to a predetermined integer multiple N of the frequency, ω_p , of pilot signal component PILOT.

Output signal CK from VCXO 124 is applied to sinewave generator 126 which develops a signal 126a that provides a digital representation of a sinusoidal signal, $\sin(\omega_p t)$, that is in the same frequency and in the same phase as pilot signal component PILOT. Sinewave generator 126 may include, for example, a counter that counts pulses of signal CK and a read-only-memory (ROM), having an address port that is coupled to an output word of the counter, such that signal 126a is produced at an output port of such ROM. Generator 126 establishes the value of integer N that was mentioned before, to be equal, for example, to 700, in accordance with the ratio between the frequency of signal CK and that of signal 126a generated by generator 126. Output signal 126a of sinewave generator 126 is coupled to phase shifter 128 which develops, in a well known manner, a cosine signal of at the same frequency of, but in a phase that is shifted by 90°, which signal corresponds to the expression $\cos(\omega_p t)$.

Standard FM and BTSC baseband composite audio signals, C(t), can be described by the equation

$$C(t) = S(t) + P\sin(\omega_p t) + D(t)\sin(2\omega_p t) \quad (1)$$

where C(t) corresponds to signal IN_D , and S(t) and D(t) correspond to the time varying (L + R) and (L - R) signals respectively, P is the amplitude, and ω_p the radian frequency of pilot signal component PILOT.

Synthesized pilot signal P_s , applied to subtraction circuit 112, is developed by measuring the amplitude of the residual pilot signal at the output of subtraction circuit 112, effectively amplifying the residual amplitude, and multiplying this value by the output of sinewave generator 126.

Assume that the amplitude, P_c , of synthesized pilot signal P_s exactly equals the amplitude P of pilot signal component PILOT. Also, the synthesized pilot signal P_s can be represented as $P_c \sin(\omega_p' t)$. The value C(t) obtained from subtraction circuit 112 that is representative of signal 112a may be expressed as

$$C'(t) = S(t) + P\sin(\omega_p t) - P_c \sin(\omega_p' t) + D(t)\sin(2\omega_p t). \quad (2)$$

The value C'(t) is multiplied in multiplier 120 by $\cos(\omega_p' t)$ to yield

$$C'(t)\cos(\omega_p' t) = S(t)\cos(\omega_p' t) + P\sin(\omega_p t)\cos(\omega_p' t) - P_c \sin(\omega_p' t)\cos(\omega_p' t) + D(t)\sin(2\omega_p t)\cos(\omega_p' t). \quad (3)$$

The first and last terms in equation (3) are sinusoids which will average to zero in the low-pass filter 122. The center two terms, $P\sin(\omega_p t)\cos(\omega_p' t) - P_c \sin(\omega_p' t)\cos(\omega_p' t)$, may be shown, by manipulating trigonometric identities, to be equivalent to

$$P/2(\sin(\omega_p t - \omega_p' t) + \sin(\omega_p t + \omega_p' t) - \sin(2\omega_p t)). \quad (4)$$

The two rightmost terms are relatively high frequency sinusoids and will average to zero in the low-pass filter 122. Since the nominal output frequency of signal 126a of sinewave generator 126 is established close to ω_p , the argument $(\omega_p t - \omega_p' t)$ of the first term of expression (4) will be close to zero. The term $\sin(\omega_p t - \omega_p' t)$ will be a very low frequency sinusoid and will not average to zero unless ω_p' equals ω_p . Therefore, as long as the frequency ω_p' is different from the pilot frequency ω_p , multiplier 120 and low-pass filter 122 will periodically vary signal 122a that is applied to VCXO 124 in a negative feedback manner that will tend to synchronize signal 126a of sinewave generator 126 to pilot signal component PILOT.

Next, consider, for example, that ω_p' and ω_p are identical frequencies but that synthesized pilot signal P_s and pilot signal component PILOT are out of phase by Δ degrees. In this instance, the output of multiplier 120 takes the form

$$C'(t)\cos(\omega_p t + \Delta) = S(t)\cos(\omega_p' t + \Delta) + P_s \sin(\omega_p t)\cos(\omega_p t + \Delta) - P_c \sin(\omega_p t + \Delta)\cos(\omega_p t + \Delta) + D(t)\sin(2\omega_p t)\cos(\omega_p t + \Delta). \quad (5)$$

The first and fourth terms on the right hand side of equation will average to zero in low-pass filter 122 since they represent sinusoidal signals having frequencies relatively high compared to the reciprocal time constant of the filter. The two middle terms can be shown to be equivalent to

$$P/2(\sin(2\omega_p t + \Delta) + \sin\Delta - \sin(2\omega_p t + 2\Delta)). \quad (6)$$

The first and third terms are relatively high frequency sinusoidal signals and will average to zero in low-pass filter 122 of PLL 100. The remaining term, $P/2\sin\Delta$, is substantially a DC term and, thus, will be passed by the low-pass filter 122 and provide a phase correction term to VCXO 124. Thus, as long as a frequency or phase error exists, multiplier 120 and low-pass filter 122 vary signal 123a. If no error exists, signal 123a remains constant.

Signal CK is coupled to an input terminal of a sinewave generator 150 that generates a signal 150a that is a digital representation of a sinewave at the radian frequency $2\omega_p$. Sinewave signal 150a is coupled to a multiplicand input port of a multiplier 116. Composite signal IN_D , less the synthesized pilot signal P_s obtained from subtraction circuit 112, is coupled to respective multiplicand input terminals of multipliers 116 and 138. Signal 150a from sinewave generator 150, that varies in accordance with the expression $\sin(2\omega_p t)$, is applied to a multiplier input terminal of multiplier 116 to produce the signal $(L-R)'$, described by the equation

$$(L-R)' = S(t)\sin(2\omega_p t) + D(t)\sin(2\omega_p t)\sin(2\omega_p t) \quad (7)$$

$$= S(t)\sin(2\omega_p t) + D(t)(1 - \cos^2(2\omega_p t)) \quad (8)$$

which is applied to a low-pass filter 118. Low-pass filter 118 is designed to pass only the baseband term $D(t)$, thus the $(L-R)$ signal is separated.

The output from subtraction circuit 112 is multiplied by the term $\sin(\omega_p t)$ in multiplier 138. Therefore, output signal P_o of multiplier 130 may be expressed as

$$P_o = S(t)\sin(\omega_p t) + P_s \sin(\omega_p t)\sin(\omega_p t) - P_c \sin(\omega_p t)\sin(\omega_p t) + D(t)\sin(2\omega_p t)\sin(\omega_p t). \quad (9)$$

The term $P_c \sin(\omega_p t)\sin(\omega_p t)$ corresponds to the pilot cancelling signal, as described in detail in U.S. Patent Application No. 882,384 entitled APPARATUS FOR CANCELLING A PILOT SIGNAL FROM A COMPOSITE SIGNAL, in the name of Todd Christopher. Signal P_o is applied to a low-pass filter 132 which integrates the signal over a relatively long period compared to $2\pi/\omega_p$. An output signal of filter 132, applied to multiplier 134 is multiplied by signal 126a of generator 126 to generate synthesized pilot signal P_s .

FIGURE 2 illustrates a detailed embodiment of VCXO 124 of FIGURE 1, embodying an aspect of the invention. Similar numerals and symbols in FIGURES 1 and 2 illustrate similar items or functions. In FIGURE 2, sinewave signal 50a at a frequency, for example, $700f_p$, where f_p is equal to the horizontal scan frequency f_H in the BTSC standard, is developed at a terminal 124b of a crystal 124a, shown in FIGURE 2 in electrical equivalent form. Signal 50a is coupled to an input terminal of a differential amplifier 50, embodying a feature of the invention, that includes PMOS transistors MQ1 and MQ2. A common current

source IS1 that is formed by utilizing CMOS technology, not shown in detail in FIGURE 2, is coupled to a junction terminal between the source electrodes of transistors MQ1 and MQ2. Consequently, complementary currents i501 and i502, having, each, a sinewave waveform, are produced at the drain electrodes of transistors MQ1 and MQ2, respectively. Thus, current i501 is in anti-phase with signal 50a; whereas, current i502 is in phase with signal 50a.

A phase control stage 51, embodying another feature of the invention, includes differential amplifiers 51a and 51b having corresponding variable gains that vary in an opposite manner. Amplifier 51b includes a pair of PMOS transistors MQ8 and MQ9. Amplifier 51a includes a pair of PMOS transistors MQ5 and MQ6. A phase shifting arrangement that includes a transistor MQ20, coupled as a source follower, a capacitor C1 and a resistor R1 produces a sinewave signal 51c, having a phase lead of, approximately, 90° relative to signal 50a. Signal 51c is coupled to the gate electrodes of transistors MQ5 and MQ8 of amplifiers 51a and 51b, respectively. The gate electrodes of transistors MQ6, MQ9 and MQ2 are coupled to a reference voltage VREF that establishes the average DC voltage at the gate electrodes of each of transistors MQ1, MQ5, MQ6, MQ8 and MQ9.

A PMOS transistor MQ7 having a drain electrode that is coupled at a junction between the source electrodes of transistors MQ5 and MQ6 forms a variable or controllable current source that varies in accordance with a controllable signal 512. Signal 512 is produced in a differential control amplifier 53. Amplifier 53 includes a pair of NMOS transistors MQ11 and MQ12. A constant current source IS2 is coupled at a junction terminal between the source electrodes of transistors MQ11 and MQ12. The gate electrode of transistor MQ11 is coupled to reference voltage VREF, and that of transistor MQ12 is coupled to frequency control signal 123a of FIGURE 1, that was mentioned before, that controls the frequency of VCO 124.

A PMOS transistor MQ14 having a drain electrode that is coupled to the drain electrode of transistor MQ12 develops signal 512, that was mentioned before, at the junction between transistors MQ14 and MQ12. The gate electrode of transistor MQ14 is coupled to its drain electrode, thus establishing a resistive load at the drain of transistor MQ12. Consequently, signal 512 varies when signal 123a varies to cause the current in transistor MQ7, operating as a common current source of differential amplifier 51a, to vary.

In accordance with a feature of the invention, the ratio between the current that flows in transistor MQ14 that is controlled by signal 123a and between the current that flows in transistor MQ7 is established by specifying the corresponding channel geometries of transistors MQ7 and MQ14, as indicated by dimensions L and W in FIGURE 2. Dimensions L and W represent the channel length and width, respectively. In this way, obtaining the required gain parameter is, advantageously, facilitated. A variation in the level of frequency control signal 123a causes the gain of amplifier 51a to vary. The gain of amplifier 51a may be defined by the ratio between current i515 or i516 that flows in transistor MQ5 or MQ6, respectively, and between signal 51c.

In accordance with another feature of the invention, the magnitude of each of current i516, that is in phase with signal 51c, and that of current i515 that is in anti-phase, changes in the same sense or direction when signal 123a changes.

Differential amplifier 51b that operates similarly to amplifier 51a generates sinewave currents i528 and i529 that are in phase with currents i515 and i516, respectively. Thus, currents i529 and i528 are in anti-phase and are complementary. Transistors MQ8, MQ9 and MQ10 of amplifier 51b perform the analogous functions to transistors MQ5, MQ6 and MQ7, respectively, of amplifier 51a. However, a gain control signal 511 that is coupled to the gate electrode of transistor MQ10 changes in the opposite sense or direction to gain control signal 512 at the gate electrode of transistor MQ7 when a change in frequency control signal 123a occurs.

Signal 511 is developed at a junction between a PMOS transistor MQ13 that is coupled to the drain electrode of transistor MQ11. Load forming transistor MQ13 performs the analogous function as transistor MQ14, that was described before, except that it causes signal 511 to vary in the opposite sense to that of signal 512 when a change in frequency control signal 123a occurs. Consequently, the current in transistor MQ10 decreases, for example, when the current in transistor MQ7 increases as a result of a corresponding change in frequency control signal 123a that causes the gain of amplifier 51a to increase. The decrease in the current in transistor MQ10 causes the corresponding gain in amplifier 51b to decrease.

Currents i501, i516 and i528 of amplifiers 50, 51a and 51b, respectively, are summed at a terminal 56 and a resulting sum current i_{SUMA} that flows in an NMOS transistor MQ3 develops a signal 56a. Signal 56a is proportional to sum current i_{SUMA} because transistor MQ3, having its gate electrode coupled to its drain electrode, operates as a resistive load. Similarly, currents i502, i515 and i529 are summed at a terminal 57 and a resulting sum current i_{SUMB} that flows in an NMOS transistor MQ4 develops a proportional signal 57a that is substantially equal in magnitude and opposite in phase to signal 56a. Thus signals 57a and 56a are

complementary.

Signal 57a is coupled to the gate electrode of an NMOS transistor MQ18; whereas, signal 56a is coupled through an inverter stage that is formed by transistors MQ15 and MQ16 to form a signal 57b that is coupled to a gate electrode of a PMOS transistor MQ17. In the inverter stage, transistor MQ16 operates as a resistive load. Consequently, current that flows in transistor MQ17 has a magnitude that is determined by the respective channel geometries of transistors MQ15, MQ16 and MQ17. Thus, by specifying the channel geometries, the design of the required gain parameters is, advantageously, simplified.

In accordance with a further aspect of the invention, PMOS transistor MQ17 and NMOS transistor MQ18, operating in a push-pull configuration, produce a signal 52a at a junction terminal between transistors MQ17 and MQ18 that is representative of the sum of the magnitudes of signals 57a and 56a. Therefore, by using complementary signals 56a and 57a to obtain single ended sum signal 52a, the magnitude of signal 52a is advantageously larger than if only one of signals 56a and 57a were used.

Sum signal 52a is coupled through an NMOS transistor MQ19, operating as a source follower, to form oscillatory signal CK. Signal CK is coupled through an RC network that includes a resistor RX5 and a capacitor C3 to a terminal 124c of crystal 124a to complete a regenerative positive feedback loop signal path of oscillator 124 when oscillatory signal CK is coupled via crystal 124a back to the reference starting terminal 124b of the feedback loop. Signal 50a, that was mentioned before, is developed across a capacitor C2 that is coupled to terminal 124b.

VCXO 124 will produce oscillatory signal CK at a frequency that will cause a total of 0° phase shift of signal 50a at, for example, terminal 124b after signal 50a traverses the entire feedback loop signal path. The phase shift between the phase of signal 50a and that of the signal at terminal 14c associated with crystal 124a is significantly frequency dependent. Crystal 124a functions in such a way that the phase of signal 50a lags that of the signal at terminal 124c by less than 180°. By having amplifiers 50, 51a, 51b vary the phase between signals CK and signal 50a, in accordance with frequency control signal 123a, the oscillation frequency of signal CK can be controllably changed.

FIGURE 3 depicts a vector diagram illustrating the range of phase variation of signal CK relative to signal 50a. Similar numbers and symbols in FIGURES 1, 2 and 3 indicate similar items or functions. Since signal CK of FIGURE 2 is in phase and is proportional in magnitude to signal 56a, for example, it is sufficient to show in FIGURE 3 the contribution signal 56a to the phase of signal CK and, for the sake of explanation, to disregard the contribution of signal 57a. In FIGURE 3, signals 50a, 51c and i501 are shown with the corresponding correct phase relationship but with arbitrary predetermined magnitudes.

In a first example, the vectors representing currents i528 and i516 have respective equal magnitudes as established in accordance with a particular value of signal 123a of FIGURE 2, representing one extreme end of a range of values that signal 123a may assume. In the first example, each of signal 56a and current i_{SUM}A of FIGURE 3, that is equal to the vector sum of currents i501, i528 and i516, is at an angle that is equal to 180° relative to signal 50a.

In a second example, that corresponds with signal 123a being less positive than in the first example, the magnitude of current i528' is larger than that of current i516'. Consequently, each of current i_{SUM}A' and signal 56a' is leading signal 50a by a phase ϕ' that is less than 180°. Thus, by varying signal 123a of FIGURE 2, the phase of signal 56a or CK varies that causes frequency of signal CK to change accordingly.

In a third example, that corresponds with signal 123a being more positive than in the first example, the magnitude of current i516" is larger than that of current i528". Consequently, each of current i_{SUM}A" and signal 56a" is lagging after signal 50a by a phase ϕ'' that is less than 180°. Because crystal 124a can cause a phase lag of no more than 180°, as mentioned before, the total phase shift after signal 50a traverses the entire feedback loop signal path, in the third example, cannot be zero. Therefore, the third example may represent an undesirable or abnormal condition that prevents VCXO 124 from operating.

FIGURE 4 illustrates a VCXO 124, embodying another aspect of the invention, that represents a second embodiment of VCXO 124 of FIGURE 1. Similar numerals and symbols in FIGURES 1, 2, 3 and 4 illustrate similar items or functions. VCXO 124' of FIGURE 4 is identical and operates similarly to, VCXO 124 of FIGURE 2 except that differential amplifier 51b and transistor MQ13 of FIGURE 1 have been eliminated from VCXO 124' of FIGURE 4. Thus, advantageously, only two differential amplifiers, 50 and 51a, of FIGURE 4 perform the function of three differential amplifiers 50, 51a and 51b, of FIGURE 2. Furthermore, because amplifier 51b of FIGURE 1 has no corresponding amplifier in VCXO 124' of FIGURE 4, a situation such as the third example that was discussed before, advantageously, cannot occur in VCXO 124' of FIGURE 4. Consequently, signal 123a of FIGURE 4 may assume values that are more positive than in the first example that was discussed before.

VCXO 124 operates as a Pierce type oscillator that is, advantageously, a stable oscillator. By varying the phase ϕ between signals 56a or CK and signal 50a, PLL 100 of FIGURE 1 generates signal CK that is

synchronized to pilot signal component PILOT.

Claims

- 5 1. A controllable phase-shifting circuit for controlling the phase of a reference signal, comprising:
means (124b,C1) for providing first and second signals, said first and second signals having a phase difference therebetween;
a first differential amplifier (50) responsive to said first signal for producing first (i501) and second (i502) antiphase output signals;
10 a second differential amplifier (51) responsive to said second signal for providing controllable amounts of third (i516) and fourth (i515) antiphase signals in response to a gain control signal (123a);
a third differential amplifier (52) also coupled to receive said second signal for providing controllable amounts of fifth (i528) and sixth (i529) antiphase signals in response to said gain control signal;
15 first combining means (MQ3) for combining said first (i501), third (i516) and fifth (i528) signals for producing a first resultant signal (56a), said third and fifth signals being of opposite phase; and characterized by
second combining means (MQ4) for combining said second (i502), fourth (i515) and sixth (i529) signals for producing a resultant second signal (57a), said fourth and sixth signals being of opposite phase; and
20 a fourth amplifier (MQ15,MQ16,MQ17,MQ18,MQ19) responsive to said first (56a) and second (57a) resultant signals for producing an output signal (CK) having a controllable phase.
2. Apparatus according to Claim 1 characterized in that said second (51) and third (52) differential amplifiers which provide said fourth (i515) and sixth (i529) signals are gain-controlled differential
25 amplifiers.
3. Apparatus according to Claim 2 characterized in that said first and second combining means are diode-connected transistor devices.
- 30 4. Apparatus according to Claim 3 characterized in that said fourth amplifier is a differential amplifier having a single-ended output.

Patentansprüche

- 35 1. Regelbare Phasenschieberschaltung zur Regelung der Phase eines Bezugssignals mit
 - einer ein erstes und ein zweites Signal mit gegenseitigem Phasenunterschied liefernden Einrichtung (124b,C1),
 - einem ersten Differenzverstärker (50), der unter Steuerung durch das erste Signal ein erstes (i501) und ein dazu gegenphasiges zweites Ausgangssignal (i502) liefert,
 - 40 - einem zweiten Differenzverstärker (51), der unter Steuerung durch das zweite Signal ein drittes (i516) und ein dazu gegenphasiges viertes Signal (i515) liefert, deren Größe durch ein Verstärkungsregelsignal (123a) bestimmbar ist,
 - einem dritten Differenzverstärker (52), der ebenfalls unter Steuerung durch das zweite Signal ein fünftes (i528) und ein dazu gegenphasiges sechstes Signal (i529) liefert, deren Größe durch das Verstärkungsregelsignal bestimmbar ist,
 - 45 - einer ersten Kombinationsschaltung (MQ3) zur Kombinierung des ersten (i501), dritten (i516) und fünften (i528) Signals zu einem ersten resultierenden Signal (56a), wobei das dritte und das fünfte Signal gegenphasig zueinander sind,
gekennzeichnet durch
 - 50 - eine zweite Kombinationsschaltung (MQ4) zur Kombinierung des zweiten (i502), vierten (i515) und sechsten (i529) Signals zu einem zweiten resultierenden Signal (57a), wobei das vierte und das sechste Signal gegenphasig zueinander sind, und
 - einen vierten Verstärker (MQ15, MQ16, MQ17, MQ18, MQ19), der unter Steuerung durch das erste (56a) und das zweite (57a) resultierende Signal ein Ausgangssignal (CK) geregelter Phasenlage erzeugt.
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2. Schaltung nach Anspruch 1, dadurch gekennzeichnet, daß der zweite und der dritte Differenzverstärker (51, 52), welche das vierte und sechste Signal (i515, i529) liefern, verstärkungsgeregelte Differenz-



synchronized to pilot signal component PILOT.

Claims

- 5 1. A controllable phase-shifting circuit for controlling the phase of a reference signal, comprising:
 - means (124b,C1) for providing first and second signals, said first and second signals having a phase difference therebetween;
 - a first differential amplifier (50) responsive to said first signal for producing first (i501) and second (i502) antiphase output signals;
 - 10 a second differential amplifier (51) responsive to said second signal for providing controllable amounts of third (i516) and fourth (i515) antiphase signals in response to a gain control signal (123a);
 - a third differential amplifier (52) also coupled to receive said second signal for providing controllable amounts of fifth (i528) and sixth (i529) antiphase signals in response to said gain control signal;
 - first combining means (MQ3) for combining said first (i501), third (i516) and fifth (i528) signals for producing a first resultant signal (56a), said third and fifth signals being of opposite phase; and characterized by
 - 15 second combining means (MQ4) for combining said second (i502), fourth (i515) and sixth (i529) signals for producing a resultant second signal (57a), said fourth and sixth signals being of opposite phase; and
 - 20 a fourth amplifier (MQ15,MQ16,MQ17,MQ18,MQ19) responsive to said first (56a) and second (57a) resultant signals for producing an output signal (CK) having a controllable phase.
2. Apparatus according to Claim 1 characterized in that said second (51) and third (52) differential amplifiers which provide said fourth (i515) and sixth (i529) signals are gain-controlled differential amplifiers.
- 25 3. Apparatus according to Claim 2 characterized in that said first and second combining means are diode-connected transistor devices.
- 30 4. Apparatus according to Claim 3 characterized in that said fourth amplifier is a differential amplifier having a single-ended output.

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 - einer ein erstes und ein zweites Signal mit gegenseitigem Phasenunterschied liefernden Einrichtung (124b,C1),
 - einem ersten Differenzverstärker (50), der unter Steuerung durch das erste Signal ein erstes (i501) und ein dazu gegenphasiges zweites Ausgangssignal (i502) liefert,
 - 40 - einem zweiten Differenzverstärker (51), der unter Steuerung durch das zweite Signal ein drittes (i516) und ein dazu gegenphasiges viertes Signal (i515) liefert, deren Größe durch ein Verstärkungsregelsignal (123a) bestimmbar ist,
 - einem dritten Differenzverstärker (52), der ebenfalls unter Steuerung durch das zweite Signal ein fünftes (i528) und ein dazu gegenphasiges sechstes Signal (i529) liefert, deren Größe durch das Verstärkungsregelsignal bestimmbar ist,
 - 45 - einer ersten Kombinationsschaltung (MQ3) zur Kombinierung des ersten (i501), dritten (i516) und fünften (i528) Signals zu einem ersten resultierenden Signal (56a), wobei das dritte und das fünfte Signal gegenphasig zueinander sind,
 - gekennzeichnet durch**
 - 50 - eine zweite Kombinationsschaltung (MQ4) zur Kombinierung des zweiten (i502), vierten (i515) und sechsten (i529) Signals zu einem zweiten resultierenden Signal (57a), wobei das vierte und das sechste Signal gegenphasig zueinander sind, und
 - einen vierten Verstärker (MQ15, MQ16, MQ17, MQ18, MQ19), der unter Steuerung durch das erste (56a) und das zweite (57a) resultierende Signal ein Ausgangssignal (CK) geregelter Phasenlage erzeugt.
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2. Schaltung nach Anspruch 1, **dadurch gekennzeichnet**, daß der zweite und der dritte Differenzverstärker (51, 52), welche das vierte und sechste Signal (i515, i529) liefern, verstärkungsgeregelte Differenz-



verstärker sind.

3. Schaltung nach Anspruch 2, dadurch gekennzeichnet, daß die erste und zweite Kombinationsschaltung als Dioden geschaltete Transistoren sind.
- 5 4. Schaltung nach Anspruch 3, dadurch gekennzeichnet, daß der vierte Verstärker ein Differenzverstärker mit Eintaktausgang ist.

Revendications

- 10 1. Circuit à décalage de phase pilotable pour commander la phase d'un circuit de référence comprenant :
- des moyens (124 b, C1) pour délivrer des premier et second signaux, lesdits premier et second signaux présentant entre eux une différence de phase ;
 - un premier amplificateur différentiel (50) agissant en réponse audit premier signal pour produire des premier (1501) et second (1502) signaux de sortie anti-phase.
 - 15 - un second amplificateur différentiel (51) agissant en réponse audit second signal pour produire des valeurs pilotables de troisième (1516) et quatrième (1515) signaux anti-phase en réponse à un signal de commande de gain (123a).
 - un troisième amplificateur différentiel (52) également couplé de manière à recevoir ledit second signal pour fournir des valeurs pilotables de cinquième (1528) et de sixième (1529) signaux anti-phase en réponse audit signal de commande de phase ;
 - des premiers moyens de combinaison (MQ3) pour combiner lesdits premier (1501), troisième (1516) et cinquième (1528) signaux afin de produire un premier signal résultant (56a), lesdits troisième et cinquième signaux étant de phase opposée et caractérisé par :
 - 20 - des seconds moyens de combinaison (MQ4) pour combiner lesdits second (1502), quatrième (1515) et sixième (1529) afin de produire un second signal résultant (57a), lesdits quatrième et sixième signaux étant de phase opposée et,
 - un quatrième amplificateur (MQ15, MQ16, MQ17, MQ18, MQ19) agissant en réponse aux premier (56a) et second (57a) signaux résultants pour produire un signal de sortie (CK) ayant une phase pilotable.
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 - 30
2. Dispositif selon la revendication 1, caractérisé en ce que, lesdits second (51) et troisième (52) amplificateurs différentiels qui fournissent lesdits quatrième (1515) et sixième (1529) signaux sont des amplificateurs différentiels à commande de gain.
- 35 3. Dispositif selon la revendication 2, caractérisé en ce que lesdits premiers et seconds moyens de combinaison sont des dispositif transistors connectés par diode.
- 40 4. Dispositif selon la revendication 3, caractérisé en ce que ledit quatrième amplificateur est un amplificateur différentiel ayant une sortie asymétrique.
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