

DESCRIPTION

RESONATOR MANUFACTURING METHOD

TECHNICAL FIELD

[0001]

The present invention relates to a method for manufacturing a resonator.

BACKGROUND ART

[0002]

Prior to the formation of resonators such as piezo-resonators, ingots of Si (silicon) are manufactured which are doped with large amounts of, for example, n-type dopants such as P (phosphorus), that is, impurities. A plurality of wafers are cut out from these ingots, and resonators are formed in a plurality of zones defined on the wafers. Thereafter, the respective zones are cut along the outlines of the respective zones of the wafers, thereby forming resonance devices.

[0003]

The ingots of Si are manufactured substantially in cylindrical shapes by the growth of single-crystalline Si according to, for example, a manufacturing method referred to as a CZ method (Czochralski method). Specifically, the ingots are manufactured by, for example, melting, on heating,

polycrystalline Si doped with large amounts of n-type dopant, for example, such as P, and immersing Si rods in the molten Si, and lifting the Si rods while rotating the rods.

PRIOR ART DOCUMENT

PATENT DOCUMENT

[0004]

Patent Document 1: Japanese Patent Application Laid-Open No. 2010-028536

SUMMARY OF THE INVENTION

Problem to be solved by the invention

[0005]

It is determined that these ingots each have a higher impurity concentration at the outer peripheral side in a radial direction of the ingot than at the inner peripheral side therein, and at the same time, have a higher impurity concentration at the bottom side in a lifting direction of the ingot than the top side therein. In accordance with these distributions in impurity concentration, the ingots each have a resistivity distribution formed to decrease in resistivity from the inner peripheral side toward the outer peripheral side, and a resistivity distribution formed to decrease in resistivity from the top side toward the bottom side.

[0006]

In the case of a plurality of wafers cut out from the ingots which have such distributions in resistivity, the resistivity varies among the wafers, depending on the distributions in impurity concentration. In the case of resonators manufactured from these wafers, frequency temperature characteristics vary depending on the variation in resistivity among the wafers. However, conventionally, this variation in resistivity among wafers have not been addressed at all.

[0007]

The present invention has been made in view of these circumstances, and an object of the invention is to provide a method for manufacturing a resonator, which is capable of effectively addressing the variation in resistivity for each wafer.

Means for solving the problem

[0008]

A method for manufacturing a resonator according to an aspect of the present invention includes the step of forming a Si oxide film at the surface of a degenerated Si wafer, and the Si oxide film has a thickness set in accordance with the doping amount of impurity in the Si wafer.

[0009]

A method for manufacturing a resonator according to another aspect of the present invention includes the step of forming a piezoelectric thin film on the surface of a degenerated Si wafer, and the piezoelectric thin film has a thickness set in accordance with the distribution of the doping amount of impurity in the Si wafer in an in-plane direction of thereof.

[0010]

A wafer body according to an aspect of the present invention includes: a degenerated Si wafer; and a piezoelectric thin film formed on the surface of the Si wafer, and the piezoelectric thin film has a thickness set in accordance with the distribution of the doping amount of impurity in the Si wafer in an in-plane direction of thereof.

Advantageous effect of the invention

[0011]

According to the present invention, a method for manufacturing a resonator can be provided, which is capable of effectively addressing the variation in resistivity for each wafer.

BRIEF EXPLANATION OF DRAWINGS

[0012]

FIG. 1 is a perspective view schematically illustrating

the appearance of a piezoelectric resonance device according to a specific example.

FIG. 2 is an exploded perspective view schematically illustrating the structure of a piezoelectric resonance device according to a specific example.

FIG. 3 is a pattern diagram of a cross section of the piezo-resonator along the line 3-3 of FIG. 2.

FIG. 4 is a graph showing the relationship between the thickness of a Si oxide film and the frequency-temperature characteristic range of a piezo-resonator.

FIG. 5 is a graph showing the relationship between the thickness of a piezoelectric thin film and the frequency-temperature characteristic range of a piezo-resonator.

FIG. 6 is a graph showing the relationship between the doping amount of impurity and the primary temperature coefficient of elastic constant of a piezo-resonator.

FIGS. 7(a) to 7(c) are each a pattern diagram of a cross section for explaining a method for manufacturing a piezoelectric resonance device according to a specific example.

FIGS. 8(a) to 8(c) are each a pattern diagram of a cross section for explaining a method for manufacturing a piezoelectric resonance device according to a specific example.

FIGS. 9(a) and 9(b) are each a pattern diagram of a

cross section for explaining a method for manufacturing a piezoelectric resonance device according to a specific example.

FIG. 10 is a graph showing the relationship between the resistivity of a wafer and the frequency-temperature characteristic range of a piezo-resonator.

FIGS. 11(a) to 11(c) are each a pattern diagram of a cross section for explaining a method for manufacturing a piezoelectric resonance device according to a specific example.

FIG. 12 is an exploded perspective view schematically illustrating the structure of a piezoelectric resonance device according to another specific example.

FIG. 13 is a pattern diagram of a cross section of the piezo-resonator along the line 12-12 of FIG. 12.

MODE FOR CARRYING OUT THE INVENTION

[0013]

An embodiment of the present invention will be described below with reference to the accompanying drawings. FIG. 1 is a perspective view schematically illustrating the appearance of a piezoelectric resonance device 10 according to a specific example. This piezoelectric resonance device 10 includes a lower substrate 11, an upper substrate 12 that forms an oscillation space with the lower substrate 11, and

a piezo-resonator 13 sandwiched between the lower substrate 11 and the upper substrate 12. The piezo-resonator 13 is a MEMS resonator manufactured by a MEMS technology. This piezoelectric resonance device 10 functions as, for example, a timing device incorporated in an electronic device such as a smartphone.

[0014]

FIG. 2 is an exploded perspective view schematically illustrating the structure of a piezoelectric resonance device 10 according to a specific example. As shown in FIG. 2, the piezo-resonator 13 includes: a support frame 14 that spreads in the form of a rectangular frame along the XY plane in the orthogonal coordinate system in FIG. 2; a base 15 that spreads in the form of a flat plate along the XY plane in the support frame 14 from one end of the support frame 14; and a plurality of oscillation arms 16 that each extend along the XY plane from a fixed end connected to one end of the base 15 toward a free end. According to the present embodiment, the four oscillation arms 16 extend parallel to the Y axis. It is to be noted that the number of oscillation arms 16 is not limited to 4, but may be set to, for example, any number of 3 or more.

[0015]

For the piezoelectric resonance device 10 according to a specific example, the lower substrate 11 spreads in the

form of a plate along the XY plane, and the upper surface of the substrate has a depression 17 formed therein. The depression 17 formed in, for example, a flat cuboid shape forms a part of the oscillation space for the oscillation arms 16. On the other hand, the upper substrate 12 spreads in the form of a plate along the XY plane, and the lower surface of the substrate has a depression 18 formed therein. The depression 18 formed in, for example, a flat cuboid shape forms a part of the oscillation space for the oscillation arms 16. The lower substrate 11 and the upper substrate 12 are both formed from Si (silicon).

[0016]

In this piezoelectric resonance device 10, the support frame 14 of the piezo-resonator 13 is received on a peripheral edge of the upper surface of the lower substrate 11, which is defined outside the depression 17, and a periphery of the lower surface of the upper substrate 12, which is defined outside the depression 18, is received on the support frame 14 of the piezo-resonator 13. In this way, the piezo-resonator 13 is held between the lower substrate 11 and the upper substrate 12, and the lower substrate 11, the upper substrate 12, and the support frame 14 of the piezo-resonator 13 form the oscillation space for the oscillation arms 16. This oscillation space is kept airtight, and the vacuum state is maintained.

[0017]

FIG. 3 is a pattern diagram of a cross section of the piezo-resonator 13 along the line 3-3 of FIG. 2.

Referring to FIG. 3 together, in the case of the piezo-resonator 13, the oscillation arms 16 each includes: a Si oxide film (thermal oxidation film), for example, a SiO_2 layer (silicon dioxide) 21; an active layer, that is, a Si layer 22 laminated on the SiO_2 layer 21; a piezoelectric thin film, that is, an AlN (aluminum nitride) layer 23 laminated on the Si layer 22; a lower electrode, that is, a Mo (molybdenum) layer 24 and an upper electrode, that is, a Mo layer 25 formed on the upper surface and lower surface of the AlN layer 23 to sandwich the AlN layer 23; and further, an AlN layer 23' laminated on the Mo layer 25. It is to be noted that the SiO_2 layer 21 may be formed between the Si layer 22 and the Mo layer 24, or on the upper surface of the Mo layer 25.

[0018]

A silicon oxide material including any composition of Si_aO_b layer (a and b are integers) is used for the Si oxide film. The active layer formed from a degenerated n-type Si semiconductor contains, as an impurity, that is, an n-type dopant, a Group 15 element such as P (phosphorus), As (arsenic), and Sb (antimony). It is to be noted that two or more of P, As, and Sb may be mixed in the active layer.

Furthermore, Ge (germanium) that has a larger ionic radius than the ionic radius of Si may be added to the active layer to control lattice distortion due to impurity doping in large amounts. According to the present embodiment, the Si layer 22 is doped with a predetermined doping amount of P (phosphorus) as an n-type dopant.

[0019]

The AlN layer 23 is a piezoelectric thin film that converts an applied voltage to oscillations. In place of the AlN layer 23, for example, a ScAlN (scandium-containing aluminum nitride) layer may be used for the piezoelectric thin film. In addition, in place of the AlN layer 23, a MgNbAlN (magnesium-niobium-containing aluminum nitride) layer, a MgZrAlN (magnesium-zirconium-containing aluminum nitride) layer, BAlN (boron-containing aluminum nitride), and GeAlN (germanium-containing aluminum nitride) may be used for the piezoelectric thin film. Furthermore, a GaN (gallium nitride) layer, an InN (indium nitride) layer, a ZnO (zinc oxide) layer, a PZT (lead zirconate titanate) layer, a KNN (potassium sodium niobate) layer, a LiTaO₃ (lithium tantalate) layer, and a LiNbO₃ (lithium niobate) layer may be used for the piezoelectric thin film.

[0020]

In place of the Mo layers 24, 25, for example, a metal material such as Ru (ruthenium), Pt (platinum), Ti

(titanium), Cr (chromium), Al (aluminum), Cu (copper), Ag (silver) or an alloy thereof is used for the lower electrode and the upper electrode. The Mo layer 24 and the Mo layer 25 are each connected to an alternating-current power supply (not shown) provided outside the piezoelectric resonance device 10. For the connection, for example, an electrode (not shown) formed on the upper surface of the upper substrate 12, a through silicon via (TSV) (not shown) formed in the lower substrate 11 or the upper substrate 12, or the like is used.

[0021]

The AlN layer 23' is, for example, a film for protecting the Mo layer 25. It is to be noted that the layer formed on the Mo layer 25 is not limited to the AlN layer, but may be, for example, a film formed from an insulator.

[0022]

The AlN layer 23 has a wurtzite structure, which is C-axis oriented substantially perpendicular to the Si layer 22. When a voltage is applied in the C-axis direction through the Mo layer 24 and the Mo layer 25, the AlN layer 23 is stretched in a direction substantially perpendicular to the C axis. With this stretching, the oscillation arms 16 undergo flexural displacement in the Z-axis direction to cause free ends thereof to undergo displacement toward the

inner surfaces of the lower substrate 11 and the upper substrate 12, thereby oscillating in an out-of-plane flexural oscillation mode.

[0023]

According to the present embodiment, the thicknesses of the Si oxide film and piezoelectric thin film are controlled in accordance with the doping amount of a dopant, that is, an impurity formed in an ingot in the manufacture of the ingot used for the manufacture of the piezo-resonator 13, and the distribution of the doping amount. The control of the thicknesses of the Si oxide film and piezoelectric thin film can reduce variations in frequency-temperature characteristics of the piezo-resonator 13. Accordingly, as will be described later, according to the present invention, the piezo-resonator 13, that is, the piezoelectric resonance device 10 can be provided which has favorable temperature characteristics.

[0024]

Next, a method for setting the thicknesses of the Si oxide film and piezoelectric thin film will be described. Prior to the manufacture of the piezoelectric resonance device 10, ingots in a substantially cylindrical shape are manufactured by, for example, a CZ method (Czochralski method). For each ingot, the doping amount of an impurity, for example, such as P is set to a predetermined setting.

However, the ingots manufactured each have a tendency to have a higher impurity concentration at the outer peripheral side in a radial direction of the ingot than at the inner peripheral side therein, and have a higher impurity concentration at the bottom side in a lifting direction of the ingot than the top side therein. In this way, the distribution of the impurity concentration is produced in the ingots.

[0025]

This distribution of the impurity concentration roughly agrees with the distribution of resistivity. Specifically, in accordance with the distribution of the impurity concentration in the lifting direction, the ingots each have such a resistivity distribution as a decrease in resistivity from the top side toward the bottom side. This resistivity distribution in the lifting direction can be specified by measuring the impurity concentration at a plurality of points in the ingot manufactured. For example, the resistivity distribution can be specified by measuring the impurity concentration through SIMS (secondary ion mass spectrometry) at a plurality of points at the bottom surface of a cylindrical block of ingot with ends removed from the ingot manufactured, and measuring the impurity concentration in the same way at a plurality of points at the upper surface of the cylindrical block. Alternatively, the

resistivity may be actually measured at these points. The resistivity can be measured by, for example, a four probe method.

[0026]

In addition, in accordance with the distribution of the impurity concentration in the radial direction of the ingot, the ingots each have such a resistivity distribution as a decrease in resistivity from the inner peripheral side toward the outer peripheral side. This resistivity distribution in the radial direction can be specified by measuring the impurity concentration at a plurality of points in the radial direction at the bottom surface and upper surface of the cylindrical block of ingot, and in consideration of the distribution of the impurity concentration in the lifting direction, calculating the distribution of the impurity concentration in the radial direction in each position in the lifting direction of the ingot.

[0027]

Prior to the manufacture of the piezo-resonator 13, a plurality of Si wafers are cut out from the cylindrical block of the ingot. Each Si wafer has an impurity concentration, that is, a resistivity in accordance with the location in the lifting direction in the ingot, and the wafers are sorted into respective lots grouped for each

predetermined resistivity range. This operation of sorting into the lots is repeated for each ingot, thereby collecting, for each lot, a plurality of Si wafers with resistivity in a predetermined range, which are cut from a plurality of ingots. In this regard, the resistivity of the Si wafer as a criterion for sorting into the lots is specified on the basis of the average value for the doping amount of impurity (average value for resistivity) in the in-plane direction of the Si wafer.

[0028]

The thickness of the Si oxide film, that is, the SiO₂ layer 21 formed at the Si wafer is controlled, for example, in each lot unit. Thus, the frequency-temperature characteristic range of the piezo-resonator 13 can be controlled appropriately in accordance with the distribution of the doping amount of impurity (resistivity) in the ingot in the lifting direction. FIG. 4 is a graph showing the relationship between the thickness of the Si oxide film and the frequency-temperature characteristic range of the piezo-resonator 13. The frequency-temperature characteristic range [ppm] refers to a value indicating a difference, that is, a magnitude of change between the maximum value and minimum value of the frequency in the operation temperature range (for example, -40°C to 85°C) of the piezoelectric resonator 13. As this frequency-temperature characteristic

range is smaller, the variation in frequency-temperature characteristics is reduced.

[0029]

As is clear from FIG. 4, for example, when the doping amount of impurity in the Si wafer has an average value of 12.6×10^{19} atm/cm³, setting the thickness of the Si oxide film to 0.33 μ m causes the frequency-temperature characteristic range to reach a minimum value. In addition, for example, when the doping amount of impurity in the Si wafer has an average value of 13.0×10^{19} atm/cm³, setting the thickness of the Si oxide film to 0.35 μ m causes the frequency-temperature characteristic range to reach a minimum value. In this way, the variation in frequency-temperature characteristics is reduced by setting the thickness of the Si oxide film to a thickness that causes the frequency-temperature characteristic range to reach a minimum value.

[0030]

In addition, in place of the thickness of the Si oxide film, that is, the SiO₂ layer 21, or in addition to the thickness of the SiO₂ layer 21, the thickness of the piezoelectric thin film that is, the AlN film 23 may be controlled. For example, as in the case of the SiO₂ layer 21, the thickness of the AlN film 23 is controlled in each lot unit. Thus, the frequency-temperature characteristic range

of the piezo-resonator 13 can be controlled appropriately in accordance with the distribution of the doping amount of impurity (resistivity) in the ingot in a radial direction. FIG. 5 is a graph showing the relationship between the thickness of the piezoelectric thin film and the frequency-temperature characteristic range of the piezo-resonator 13. As in the case described previously, the frequency-temperature characteristic range [ppm] refers to a value indicating a difference, that is, a magnitude of change between the maximum value and minimum value of the frequency in the operation temperature range (for example, -40°C to 85°C) of the piezoelectric resonator 13.

[0031]

For example, a case is assumed where the doping amount of impurity is 1.26×10^{20} atm/cm³ near the center of the Si wafer, whereas the doping amount of impurity is 1.30×10^{20} atm/cm³ near the outer periphery of the Si wafer. In this case, as is clear from FIG. 5, near the center of the Si wafer, the thickness of the piezoelectric thin film is set to 0.850 μm with which the frequency-temperature characteristic range reaches a minimum value. In addition, near the outer periphery of the Si wafer, the thickness of the piezoelectric thin film is set to 0.790 μm with which the frequency-temperature characteristic range reaches a minimum value.

[0032]

As described above, the distribution of the doping amount of impurity is formed in the in-plane direction of the Si wafer, and the thickness distribution is thus set in the radial direction in the case of the AlN film 23 in accordance with the distribution of the doping amount, formed in the radial direction from the inner peripheral side of the Si wafer toward the outer peripheral side thereof, for example. This thickness distribution of the piezoelectric thin film in the radial direction is set so as to achieve a thickness distribution in which the frequency-temperature characteristic range reaches a minimum value, thereby reducing the variation in frequency-temperature characteristics.

[0033]

FIG. 6 is a graph showing the relationship between the doping amount of impurity and the primary temperature coefficient of elastic constant of the piezo-resonator 13. As is clear from FIG. 6, the frequency-temperature characteristics increase in a relatively rapid manner up to approximately 9×10^{19} atm/cm³ as the doping amount of impurity in the Si wafer is increased from 0, while the frequency-temperature characteristics decrease in relatively gradual manner when the doping amount of impurity exceeds approximately 9×10^{19} atm/cm³.

[0034]

Therefore, in order to address the distribution of the doping amount (resistivity) in the in-plane direction of the Si wafer, for example, a material such as AlN or ScAlN that has a negative primary temperature coefficient of elastic constant is used as the piezoelectric thin film, and when the doping amount in the Si wafer is more than approximately 9×10^{19} atm/cm³, the thickness of the piezoelectric thin film is increased at the outer peripheral side of the Si wafer, rather than at the inner peripheral side thereof. On the other hand, in the case of the doping amount below approximately 9×10^{19} atm/cm³, the thickness of the piezoelectric thin film is decreased at the outer peripheral side of the Si wafer, rather than at the inner peripheral side thereof. More specifically, it is preferable to control the thickness distribution of the piezoelectric thin film, with the doping amount of approximately 9×10^{19} atm/cm³ as a threshold value.

[0035]

It is to be noted that the distribution of the doping amount (resistivity) in the in-plane direction of the Si wafer can be also addressed by control of the thickness distribution of the thin film (resonator-constituting thin film) constituting the piezo-resonator 13 formed above the Si layer 22, in place of the control of the thickness

distribution of the piezoelectric thin film. Examples of the resonator-constituting thin film include, for example, the lower electrode 24 and the upper electrode 25. Besides, the distribution of the doping amount (resistivity) in the in-plane direction of the Si wafer can be also addressed by control of the distribution of, for example, the thickness of a parasitic capacitance-reducing (for example, silicon oxide) layer formed between the lower electrode 24 and the Si layer 22, or the thickness of an additional thin film layer such as a protective film layer of, for example, a silicon oxide layer or an AlN layer formed on the upper electrode 25.

[0036]

For the foregoing resonator-constituting thin film, in the case of using, as the resonator-constituting thin film, a material such as, for example, AlN, Mo, Al, Pt, Ru, Ir (iridium), Ti, ScAlN, or SiN (silicon nitride) that has a negative primary temperature coefficient of elastic constant, it is preferable to control the thickness distribution of the resonator-constituting thin film, with the doping amount of approximately 9×10^{19} atm/cm³ as a threshold value in the same way as described previously. The distribution of the thickness in the in-plane direction of the Si wafer is controlled in the same way as described previously. It is to be noted that in the case of, for example, a material

that has a positive primary temperature coefficient of elastic constant, such as SiO₂ or SiOF (fluorine-containing silicon oxide film), it is preferable to set the thickness in an opposite manner to the foregoing in the in-plane direction of the Si wafer, with the above-mentioned threshold voltage as a boundary.

[0037]

Next, a method for manufacturing the piezoelectric resonance device 10 will be schematically described below. FIGS. 7(a) to 7(c) are each a cross-sectional view for explaining a method for manufacturing the piezoelectric resonance device 10 according to a specific example of the present invention. It is to be noted that while a plurality of zones corresponding to respective piezoelectric resonance devices 10 are defined on a Si wafer, only one zone on the Si wafer is illustrated in the figures for the following explanation of the manufacturing method. In addition, the thicknesses of the Si oxide film and piezoelectric thin film are controlled for each lot of a plurality of collected Si wafers with a predetermined range of resistivity.

[0038]

First, as shown in FIG. 7(a), for the manufacture of the lower substrate 11, a plate-like wafer 31 formed from Si is prepared, and the entire surface of the wafer 31 is subjected to a thermal oxidation treatment, thereby forming

a Si oxide film (for example, SiO_2) 32 with a predetermined thickness over the entire surface of the wafer 31. As shown in FIG. 7(b), in the surface of the wafer 31, a depression 33 is formed by, for example, etching. Thereafter, as shown in FIG. 7(c), the wafer 31 is cleaned after removing the Si oxide film 32. In this way, the lower substrate 11 with the depression 17 in the upper surface thereof is formed.

[0039]

On the other hand, as shown in FIG. 8(a), for the manufacture of the piezo-resonator 13, a degenerated Si wafer 34 is prepared. The Si wafer 34 is doped with an impurity in a predetermined doping amount, the actual doping amount (resistivity) of the Si wafer 34 is specified in advance. The entire surface of the Si wafer 34 is subjected to a thermal oxidation treatment, thereby forming a Si oxide film (for example, SiO_2) 35 with a predetermined thickness. It is to be noted that besides thermal oxidation films, TEOS oxidation films, PECVD oxidation films, and sputtered oxidation films can be used for the Si oxide film 35. The thickness of the Si oxide film is set in accordance with the average value for the actual doping amount (resistivity) in the in-plane direction of the Si wafer 34 as described above.

[0040]

Thereafter, as shown in FIG. 8(b), the lower surface of the Si wafer 34 is put on the upper surface of the wafer 31

described previously, thereby joining the Si wafer 34 to the upper surface of the wafer 31. For the joining, for example, fusion joining is carried out. Subsequently, as shown in FIG. 8(c), the upper surface of the Si wafer 34 is subjected to a grinding treatment and a polishing treatment (CMP: chemical mechanical polishing), thereby grinding and removing the Si oxide film 35 at the upper surface of the Si wafer 34 and a part of the Si wafer 34, and thus planarizing the surface of the Si wafer 34. In this way, a so-called Cavity SOI is manufactured.

[0041]

Thereafter, as shown in FIG. 9(a), on the Si wafer 34, a lower electrode film (for example, Mo) 36, a piezoelectric thin film (for example, AlN) 37, an upper electrode film (for example, Mo) 38, and a piezoelectric thin film 37' are sequentially deposited by, for example, sputtering. In this regard, the thickness of the piezoelectric thin film 37 is set in accordance with the distribution of the doping amount of impurity (resistivity) in the in-plane direction of the Si wafer 34 as described above. For example, the thickness of the piezoelectric thin film 37 has a distribution in the in-plane direction such that the thickness of the piezoelectric thin film 37 is decreased from near the center of the Si wafer 34 toward the outer periphery. In this way, a wafer body is manufactured which includes the

piezoelectric thin film 37 with a thickness set in accordance with the distribution of the doping amount (resistivity) in the in-plane direction of the Si wafer 34. [0042]

In this regard, for the formation of the piezoelectric thin film 37, for example, an Al target (not shown) is disposed to be opposed to the upper surface of the Si wafer 34. A magnet (not shown) is disposed behind the Al target to confine electrons in a magnetic field, thereby accelerating ionization of an inert gas such as Ar (argon), and thus generating a high concentration of plasma around the Al target. As a result, the piezoelectric thin film 37 can be deposited at high speed. Accordingly, the distribution of sputtered particles that reach the upper surface of the Si wafer 34 depends largely on the distribution of the magnetic field formed by the magnet. In other words, controlling the distribution of the magnetic field allows the thickness of the piezoelectric thin film 37 to have a distribution. [0043]

Accordingly, for example, the location of the magnet or the rotation speed of the Si wafer 34 is adjusted to control the magnetic field intensity of the magnet, thereby allowing the thickness of the piezoelectric thin film 37 to have a distribution in the in-plane direction. Alternatively, in

place of this method, it is also possible to measure the thickness of the piezoelectric thin film 37 actually after forming the piezoelectric thin film 37 with a uniform thickness on the upper surface of the Si wafer 34, and chip away the piezoelectric thin film 37 with Ar ion beams or the like so as to achieve a desired distribution in thickness, thereby causing the piezoelectric thin film 37 to have a distribution in thickness. According to this method, the thickness of the piezoelectric thin film 37 can be controlled in a more precise manner.

[0044]

Subsequently, as shown in FIG. 9(b), the Si wafer 34, the Si oxide film 35, the lower electrode film 36, the piezoelectric thin film 37, the upper electrode film 38, and the piezoelectric thin film 37' are subjected to, for example, dry etching or wet etching, thereby forming the shapes of the support frame 14, base 15, and oscillation arms 16 described above. In this way, the piezo-resonator 13 is formed which is supported by the support frame 14 on the upper surface of the lower substrate 11. Thereafter, a wafer (not shown) that has depressions formed in advance in zones corresponding to the respective zones of the Si wafer 34 is joined onto the piezo-resonator 13. Subsequently, respective piezoelectric resonance devices 10 are cut out along the outlines of the respective zones, for example,

with a diamond blade or by a laser dicing method.

[0045]

It is to be noted that while the both thicknesses of the Si oxide film 35 and piezoelectric thin film 37 are controlled in accordance with the doping amount of impurity (resistivity) in the degenerated Si wafer 34 and the distribution thereof according to the above-described method for manufacturing the piezoelectric resonance device 10, the present invention is not to be considered limited thereto, but for example, the thickness of only either the Si oxide film 35 or the piezoelectric thin film 37 may be controlled. The piezoelectric resonance device 10 which varies little in frequency-temperature coefficient can be provided even by controlling the thickness of only either the Si oxide film 35 or the piezoelectric thin film 37 in this way as just described.

[0046]

Moreover, a method where a Si wafer is sorted into a lot on the basis of the average value for the doping amount of impurity in the in-plane direction of the Si wafer, and the thickness of the SiO₂ layer 21 formed at the Si wafer is controlled in each lot unit has been described as an example in accordance with the above-described method for manufacturing the piezoelectric resonance device 10. However, the invention is not limited thereto, but it is

also possible to further control the thickness of the SiO₂ layer 21 in accordance with the distribution of the doping amount of impurity in the in-plane direction of the Si wafer. [0047]

Specifically, in the step shown in FIG. 8(a), the film thickness of the Si oxide film 35 is controlled after forming the Si oxide film 35 with a predetermined thickness over the entire surface of the Si wafer 34. Prior to the control of the film thickness of the Si oxide film 35, first, the in-plane resistivity distribution of the Si wafer 34 is specified.

[0048]

It is possible to specify the in-plane resistivity distribution of the Si wafer 34, for example, on the basis of the distribution of the resistivity in a radial direction of an ingot. Specifically, the distribution of the resistivity in the radial direction of the ingot can be specified by calculating the distribution of the impurity concentration in the radial direction in each location in the lifting direction of the ingot as described above.

[0049]

Next, the film thickness distribution of the Si oxide film 35 is measured in plane with the Si wafer 34. Then, the film thickness of the Si oxide film 35 is controlled by trimming on the basis of the specified resistivity

distribution and film thickness distribution, such that the piezo-resonator 13 has uniform frequency-temperature characteristics in plane with the Si wafer 34.

[0050]

FIG. 10 is a diagram showing the relationship between the resistivity of a wafer and the frequency-temperature characteristics of the piezo-resonator 13. In FIG. 10, the horizontal axis indicates the resistivity of a wafer, whereas the vertical axis indicates a primary coefficient term of frequency-temperature characteristics. From FIG. 10, it is determined that as the resistivity of the wafer is increased, the frequency-temperature characteristics have a larger value, and approach asymptotically to around 2.0 ppm/K. Accordingly, from the relationship between the frequency-temperature characteristics and the resistivity, and the relationship between the frequency-temperature characteristic and the thickness of the Si oxide film as shown in FIG. 4, it is determined that for example, in the case of a wafer of 0.5 mΩcm in average resistivity, the variation in frequency-temperature characteristics can be reduced by controlling the film thickness so as to make the Si oxide film 35 thinner, in a region where the resistivity is high in plane with the wafer.

[0051]

For example, local etching with the use of, for example,

a rare gas, for example, Ar (argon) ion beams, or a chemical reaction gas, for example, SF_6 (sulfur hexafluoride) gas plasma, or local etching of spraying a hydrofluoric acid solution from a thin nozzle to the Si wafer can be used for trimming the film thickness of the Si oxide film 35.

[0052]

This local etching makes it possible to reduce the variation in frequency-temperature characteristics on the basis of the resistivity in plane with the Si wafer.

[0053]

In addition, the manufacturing method described below may be implemented in place of the method for manufacturing a Cavity SOI as described above. For example, as shown in FIG. 11(a), the entire surface of the degenerated Si wafer 34 described previously is subjected to a thermal oxidation treatment, thereby forming the Si oxide film 35 with a predetermined thickness. A handle wafer 41 of Si is joined to the lower surface of the Si wafer 34. On the other hand, a wafer 31 with a depression 33 is formed in the same way as described previously. Thereafter, as shown in FIG. 11(b), the upper surface of the Si wafer 34 is bonded to the upper surface of the wafer 31 with the depression 33 by, for example, fusion joining.

[0054]

After joining the wafer 31 and the Si wafer 34, the

handle wafer 41 is removed from the upper surface of the Si wafer 34. Thereafter, as shown in FIG. 11(c), the Si oxide film 35 at the upper surface of the Si wafer 34 is removed by wet etching.

Thereafter, in the same way as described previously, a lower electrode film (for example, Mo) 36, a piezoelectric thin film (for example, AlN) 37, and an upper electrode film (for example, Mo) 38 are sequentially deposited on the upper surface of the Si wafer 34, for example, by sputtering, thereby manufacturing a piezoelectric resonance device 10.

[0055]

FIG. 12 is an exploded perspective view schematically illustrating a structure that represents the appearance of a piezoelectric resonance device 50 according to another specific example. This piezoelectric resonance device 50 includes a piezo-resonator 53 which oscillates in an in-plane spread oscillation mode, in place of the piezo-resonator 13 which oscillates in a flexural oscillation mode as described previously. The piezo-resonator 53 is sandwiched between a lower substrate 11 and an upper substrate 12, as in the case of the piezo-resonator 13 described previously. The lower substrate 11 and the upper substrate 12 have the same configurations as the structures described previously, and the repeated explanations will be thus left out.

[0056]

The piezo-resonator 53 includes: a support frame 54 that spreads in the form of a rectangular frame along the XY plane in the orthogonal coordinate system in FIG. 12; an oscillation part 55 disposed inside the support frame 54 to spread in a rectangular form along the XY plane as in the case of the support frame 54; and a pair of connection parts 56, 56 connecting the support frame 54 and the oscillation part 55 to each other. The oscillation part 55 oscillates by repeated stretching in the Y-axis direction along the XY plane, as will be described later.

[0057]

The support frame 54 includes: a pair of longer frame parts 54a, 54a extending parallel to the X axis; and a pair of shorter frame parts 54b, 54b extending parallel to the Y axis, with both ends thereof connected respectively to both ends of the frame parts 54a, 54a. According to the present embodiment, the connection parts 56, 56 extend in a straight line parallel to the X axis to connect the frame parts 54b, 54b and the oscillation part 55 to each other. The connection parts 56, 56 are located at ends (node points) in intermediate positions of the oscillation part 55 in the Y-axis direction, that is, in center positions in the oscillation direction of the oscillation part 55.

[0058]

FIG. 13 is a pattern diagram of a cross section along the line 12-12 of FIG. 12. As is clear from FIG. 13, in the case of piezo-resonator 53, the support frame 54, the oscillation part 55, and the connection parts 56 are formed from: a Si oxide film, that is, a SiO₂ layer 61; an active film, that is, a Si layer 62 laminated on the SiO₂ layer 61; a piezoelectric thin film, that is, an AlN layer 63 laminated on the Si layer 62; a lower electrode, that is, a Mo layer 64 and an upper electrode, that is, a Mo layer 65 formed on the upper surface and lower surface of the AlN layer 63 to sandwich the AlN layer 63 therebetween; and further an AlN layer 63' laminated on the Mo layer 65. These layers have the same structures as the layers described previously, and the repeated explanations will be thus left out.

[0059]

In this piezoelectric resonance device 50, the AlN layer 63 is C-axis oriented substantially perpendicular to the Si layer 62. The oscillation part 55 is excited through the application of alternating electric field substantially in the C-axis direction between the Mo layer 64 and the Mo layer 65. As a result, the oscillation part 55 undergoes stretching oscillation in the shorter side direction, that is, the Y-axis direction. In other words, there is stretching oscillation of repeating the stretched

oscillation part 55 and the shortened oscillation part 55 in the Y-axis direction. The manufacturing method according to the present invention can be also applied to the piezoelectric resonance device 50.

[0060]

While the piezoelectric resonance devices 10, 50 according to the embodiments described above have been described to function as timing devices, the devices may be configured to function as, for example, a gyro sensor, an acceleration sensor, a pressure sensor, a microphone, an ultrasonic transducer, an energy harvester, or a RF (high-frequency) filter.

[0061]

It is to be noted that the foregoing respective embodiments are intended to facilitate understanding of the present invention, but not intended to construe the present invention in any limited way. Modifications and/or improvements can be made to the present invention without departing from the spirit of the invention, and the invention encompasses equivalents thereof. More specifically, the scope of the present invention also encompasses therein the respective embodiments with design changes appropriately made thereto by one skilled in the art, as long as the embodiments have the features of the present invention. For example, the respective elements included in

the respective embodiments, and the layout, materials, conditions, shapes, sizes, and the like of the elements are not to be considered limited to those exemplified, but may be changed appropriately. In addition, the respective elements included in the respective elements may be combined as long as the combinations are technically possible, and the scope of the present invention also encompasses therein the combinations as long as the combinations have the features of the present invention.

DESCRIPTION OF REFERENCE SYMBOLS

[0062]

- 13: resonator (piezo-resonator)
- 21: Si oxide film
- 23: piezoelectric thin film
- 34: Si wafer
- 35: Si oxide film
- 37: piezoelectric thin film
- 53: resonator (piezo-resonator)
- 61: Si oxide film
- 63: piezoelectric thin film

CLAIMS:

1. A method for manufacturing a resonator, the method comprising the step of forming a Si oxide film at a surface of a degenerated Si wafer,

wherein the Si oxide film has a thickness set in accordance with a doping amount of impurity in the Si wafer.

2. The method for manufacturing a resonator according to claim 1, wherein the doping amount of impurity is specified by an average for the doping amount of impurity in an in-plane direction of the Si wafer.

3. The method for manufacturing a resonator according to one of claims 1 and 2, the method further comprising the step of forming a piezoelectric thin film on a surface of the Si wafer,

wherein the piezoelectric thin film has a thickness set in accordance with a distribution of the doping amount of impurity in the Si wafer in an in-plane direction thereof.

4. The method for manufacturing a resonator according to claim 3, wherein the piezoelectric thin film has a thickness distribution set on the basis of the doping amount of impurity and a temperature coefficient of elastic constant

of the resonator.

5. The method for manufacturing a resonator according to one of claims 1 and 2, the method further comprising the step of forming a resonator-constituting thin film on a surface of the Si wafer,

wherein the resonator-constituting thin film has a thickness set in accordance with a distribution of the doping amount of impurity in the Si wafer in an in-plane direction thereof.

6. The method for manufacturing a resonator according to claim 5, wherein the resonator-constituting thin film has a thickness distribution set on the basis of the doping amount of impurity and a temperature coefficient of elastic constant of the resonator.

7. The method for manufacturing a resonator according to one of claims 5 and 6, wherein the resonator-constituting thin film comprises any one of: a piezoelectric thin film formed on the Si wafer; an upper electrode and a lower electrode formed to sandwich the piezoelectric thin film therebetween; an additional thin film layer formed between the Si wafer and the lower electrode; and an additional thin film layer formed over the upper electrode.

8. A method for manufacturing a resonator, the method comprising the step of forming a piezoelectric thin film on a surface of a degenerated Si wafer,

wherein the piezoelectric thin film has a thickness set in accordance with a distribution of a doping amount of impurity in the Si wafer in an in-plane direction of thereof.

9. A wafer body comprising:

a degenerated Si wafer; and

a piezoelectric thin film formed on a surface of the Si wafer,

wherein the piezoelectric thin film has a thickness set in accordance with a distribution of a doping amount of impurity in the Si wafer in an in-plane direction of thereof.