CLAIMS

What is claimed is:

1. A receiver system comprising:

a data interface circuit configured to receive a plurality of data frames corresponding to redundant data, the plurality of data frames having an error checking portion, the error checking portion having a frame error checking code, the plurality of data frames including a first data frame and a second data frame;

a comparison circuit coupled to the data interface circuit, the comparison circuit configured to perform a bit comparison of first bit values at bit positions of the first data frame of the plurality of data frames against second bit values at the bit positions of a second data frame of the plurality of data frames, and to identify based on the bit comparison inconsistent bit values between the first bit values and the second bit values;

a frame permutation assembly circuit coupled to the comparison circuit, the frame permutation assembly circuit configured to assemble permutations of data frames, each of the permutations of data frames including a unique set of bit values across the bit positions having the inconsistent bit values; and

a frame error checking circuit coupled to the frame permutation assembly circuit, the frame error checking circuit implemented in hardware and configured to perform an analysis of each of the permutations of data frames for validation of a calculated error checking code, the validation including a parallel calculation of the calculated error checking code of each of the permutations of data frames, and a comparison of each calculated error checking code with the frame error checking code in the error checking portion of one of the first data frame and the second data frame.

2. The receiver system of claim 1, wherein:

the comparison circuit is configured to perform a byte comparison of first byte values at byte positions of the first data frame of the plurality of data frames against second byte values at the byte positions of the second data frame of the plurality of data frames, and to identify, based on the byte comparison, inconsistent byte values between the first byte values and the second byte values; and

the permutations of data frames include a unique set of permutations of bytes at each of the inconsistent byte values.

3. The receiver system of claim 1, wherein the system is incorporated into an indoor unit (IDU) of a split-mount radio system.

4. The receiver system of claim 1, wherein the comparison circuit is configured to perform a bitwise Exclusive Or (XOR) operation on each of the plurality of data frames to identify the inconsistent bit positions in the plurality of data frames.

5. The receiver system of claim 1, wherein the comparison circuit is configured to perform a summation and voting operation on each of the plurality of data frames to identify the inconsistent bit positions in the plurality of data frames.

6. The receiver system of claim 5, wherein the plurality of data frames comprises more than two data frames.

7. The receiver system of claim 1, wherein the system supports a radio link, and a number of the permutations of data frames is limited by a specified error rate of the radio link.

8. The receiver system of claim 1, wherein the plurality of data frames comprises Ethernet data frames.

9. The receiver system of claim 1, wherein the data interface circuit is configured to provide a passed data frame from the permutations of data frames, the calculated error checking code of the passed data frame being consistent with the frame error checking code of the error checking portion of the passed data frame.

10. The receiver system of claim 1, wherein the hardware comprises a Field Programmable Gate Array (FPGA) incorporated into a radio access card (RAC) of an indoor unit of a split-mount radio system.

11. A method implemented by one or more physical processors of a receiver, the method comprising:

receiving a plurality of data frames corresponding to redundant data, the plurality of data frames having an error checking portion, the error checking portion having a frame error checking code, the plurality of data frames including a first data frame and a second data frame;

performing a bit comparison of first bit values at bit positions of the first data frame of the plurality of data frames against second bit values at the bit positions of a second data frame of the plurality of data frames;

identifying, based on the bit comparison, inconsistent bit values between the first bit values and the second bit values;

assembling permutations of data frames, each of the permutations of data frames including a unique set of bit values across the bit positions having the inconsistent bit values; and

performing an analysis of each of the permutations of data frames for validation of a calculated error checking code, the validation including a parallel calculation of the calculated error checking code of each of the permutations of data frames, and a comparison of each calculated error checking code with the frame error checking code in the error checking portion of one of the first data frame and the second data frame.

12. The method of claim 11, wherein:

performing the bit comparison comprises performing a byte comparison of first byte values at byte positions of the first data frame of the plurality of data frames against second byte values at the byte positions of the second data frame of the plurality of data frames, and identifying, based on the byte comparison, inconsistent byte values between the first byte values and the second byte values; and

the permutations of data frames include a unique set of permutations of bytes at each of the inconsistent byte values.

13. The method of claim 11, wherein the method is executed by a controller module of an indoor unit (IDU) of a split-mount radio system.

14. The method of claim 11, wherein performing the bit comparison comprises performing a bitwise Exclusive Or (XOR) operation on each of the plurality of data frames to identify the inconsistent bit values.

15. The method of claim 11, wherein performing the bit comparison comprises performing a summation and voting operation on each of the plurality of data frames to identify the inconsistent bit values.

16. The method of claim 15, wherein the plurality of data frames comprises more than two data frames.

17. The method of claim 11, wherein the permutations of data frames are limited by a specified error rate of a radio link supporting communication of the plurality of data frames.

18. The method of claim 11, wherein the plurality of data frames comprises Ethernet data frames.

19. The method of claim 11, further comprising providing a passed data frame from the permutations of data frames, the calculated error checking code of the passed data frame being consistent with the frame error checking code of the error checking portion of the passed data frame.

20. The method of claim 11, wherein the receiver comprises a Field Programmable Gate Array (FPGA) incorporated into a radio access card (RAC) of an indoor unit of a split-mount radio system.

21. A receiver system comprising:

means for receiving a plurality of data frames corresponding to redundant data, the plurality of data frames having an error checking portion, the error checking portion having a frame error checking code, the plurality of data frames including a first data frame and a second data frame;

means for performing a bit comparison of first bit values at bit positions of the first data frame of the plurality of data frames against second bit values at the bit positions of a second data frame of the plurality of data frames, and to identify, based on the bit comparison, inconsistent bit values between the first bit values and the second bit values;

means for assembling permutations of data frames, each of the permutations of data frames including a unique set of bit values across the bit positions having the inconsistent bit values; and

means for performing an analysis of each of the permutations of data frames for validation of a calculated error checking code, the validation including a parallel calculation of the calculated error checking code of each of the permutations of data frames, and a comparison of each calculated error checking code with the frame error checking code in the error checking portion of one of the first data frame and the second data frame.