What is claimed is:

1. A memory array, comprising:

a plurality of first dielectric materials and a plurality of stacks, wherein each respective first dielectric material and each respective stack alternate, and wherein each respective stack comprises a first conductive material and a storage material on only one side of the first conductive material;

a second conductive material passing through the plurality of first dielectric materials and the plurality of stacks such that a major axis of the second conductive material is perpendicular to a major axis of the storage material; and

a second dielectric material in direct physical contact with the second conductive material and passing through the plurality of first dielectric materials and the plurality of stacks between the second conductive material and the plurality of stacks;

wherein each respective stack further comprises a third dielectric material between the first conductive material and the second dielectric material such that the storage material of the respective stack is on only one side of the third dielectric material, the second dielectric material is between the second conductive material and the third dielectric material, and the third dielectric material is in direct physical contact with the first conductive material and the second dielectric material.

2. The memory array of claim 1,wherein the storage material is in direct physical contact with the second dielectric material.

3. The memory array of claim 1, wherein the second dielectric material is in direct physical contact with the plurality of first dielectric materials.

4. The memory array of claim 1, wherein each respective stack further comprises a fourth dielectric material between the first conductive material and the storage material.

5. The memory array of claim 1, wherein the first conductive material and the storage material are at different levels within each respective stack.

6. The memory array of claim 1, wherein the major axis of the second conductive material is perpendicular to major axes of the plurality of first dielectric materials.

7. The memory array of claim 1, wherein the storage material is a self-selecting storage material.

8. The memory array of claim 1, wherein the storage material is formed around the second conductive material.

9. The memory array of claim 1, wherein the storage material comprises a chalcogenide material.

10. A memory array, comprising:
a stack of memory cells;
a first dielectric material; and
a first conductive material in direct physical contact with the first dielectric material;
wherein each respective memory cell comprises:
a respective portion of the first conductive material;
a respective portion of the first dielectric material;
a second conductive material;
a storage material on only one side of the second conductive material such that a major axis of the first conductive material is perpendicular to a major axis of the storage material; and
a second dielectric material between the second conductive material and the first dielectric material such that the storage material is on only one side of the second dielectric material, the first dielectric material is between the first conductive material and the second dielectric material and the second dielectric material is in direct physical contact with the first dielectric material and the second conductive material.

11. The memory array of claim 10, wherein the memory cells are separated from each other by an additional dielectric material.

12. The memory array of claim 10, wherein the first dielectric material is between the first conductive material and the storage material.

13. The memory array of claim 10, wherein each respective memory cell comprises an additional dielectric material between the second dielectric material and the storage material.

14. The memory array of claim 13, wherein the additional dielectric material is between the second conductive material and the storage material.

15. The memory array of claim 10, wherein the storage material of each respective memory cell is to form a conductive path between the first conductive material and the second conductive material.

16. The memory array of claim 10, wherein the major axis of the first conductive material is perpendicular to a major axis of the second conductive material.

17. The memory array of claim 10, wherein the second conductive material and the storage material of each respective memory cell are formed around the first conductive material.

18. The memory array of claim 1, wherein a surface of the charge storage material, in each respective stack, that is in direct physical contact with the second dielectric material is coplanar with a surface of the third dielectric material, in each respective stack, that is in direct physical contact with the second dielectric material.