

DESCRIPTION

INFORMATION PROCESSING DEVICE, METHOD, AND PROGRAM

FIELD

[0001] Embodiments of the present invention relate to an information processing device, a method, and a program.

BACKGROUND

[0002] For example, an intelligent input/output device is known which includes multiple master MPUs that access for control via a shared memory in a system applied to process control.

Such an intelligent input/output device includes one or more master MPUs that process input/output data from and to corresponding controlled devices, a shared memory for input/output data transfer to and from a master MPU of a host controller, and a circuit that connects the master MPUs processing input/output data and the master MPU of the host controller to the shared memory.

CITATION LIST

Patent Literature

[0003] Patent Literature 1: Japanese Laid-open Patent Publication No. 2000-20491

SUMMARY OF THE INVENTION

Problem to be Solved by the Invention

[0004] In the conventional intelligent input/output device, when two or more master MPUs access the shared memory concurrently, the other or rest of the master MPUs need to wait for access until one of the master MPUs completes the processing.

[0005] This may lead to decreasing an effective processing speed of the master MPU waiting for the processing. Particularly, as the number of master MPUs increases, the number of master MPUs waiting for the processing also increases, which may cause a significant decrease in the effective processing speed of each master MPU.

[0006] In view of the above, the present invention aims to provide an information processing device, a method, and a program that enable master MPUs of an intelligent input/output device to transfer input/output data via a shared memory without a decrease in the effective processing speed of each master MPU even with an increase in the number of master MPUs.

Means for Solving Problem

[0007] An information processing device according to the embodiments is the information processing device that controls access from n (n being an integer equal to or greater than 2) MPUs to a shared memory.

A control unit analyzes an access pattern to the shared memory based on access requests to the shared memory received in parallel from the n MPUs in a same access phase, and sequentially processes, in the access phase, the received m (m being a natural number equal to or less than n) access requests in order based on the analyzed access pattern.

BRIEF DESCRIPTION OF DRAWINGS

[0008] FIG. 1 is a schematic block diagram of a configuration of a process control system 10 including an information processing device according to an embodiment.

FIG. 2 is a schematic block diagram of a configuration of a host controller 11 and an intelligent input/output

device 12.

FIG. 3 is a process timing chart illustrating an example in which a master MPU 11A and a master MPU 23-1 perform a data read process when the intelligent input/output device is in a T2 phase.

FIG. 4 is a process timing chart illustrating an example in which the master MPU 11A and the master MPU 23-1 perform a data write process when the intelligent input/output device is in the T2 phase.

FIG. 5 is a diagram illustrating an access pattern analysis table.

FIG. 6 is a process flowchart of the intelligent input/output device 12.

DETAILED DESCRIPTION

[0009] Hereinafter, an embodiment will be described in detail with reference to the accompanying drawings.

FIG. 1 is a schematic block diagram of a configuration of a process control system 10 including an information processing device according to the embodiment.

The process control system 10 includes a host controller 11 that integrally controls the overall process control system 10, an intelligent input/output device 12 that controls inputs and outputs under the control of the host controller 11, an interface unit 13 that includes input/output interfaces I11 to I1n, and controlled devices DEV1 to DEVn that are connected to the interface unit 13 via corresponding interfaces I21 to I2n and a communication network 14.

[0010] Herein, it is assumed that the controlled devices DEV1 to DEVn include controlled devices such as motors and valves and sensor units that sense various conditions (such as a current, a voltage, a temperature, a flow rate, and a

pressure).

[0011] In the following, for the purpose of better understanding, one master MPU 23-1 of the intelligent input/output device 12 will be mainly described. In the following description, it is assumed that read addresses and write addresses in a shared memory 21 are pre-assigned to the controlled devices DEV1 to DEVn, an access order is also designated in advance in a cyclic manner, and the same read address or write address is not redundantly assigned to the controlled devices DEV1 to DEVn.

[0012] FIG. 2 is a schematic block diagram of a configuration of the host controller 11 and the intelligent input/output device 12.

The host controller 11 includes a master MPU 11A that controls the host controller 11 as a whole and includes a clock terminal CLK, a ready terminal RDY to which a first ready signal RDY1 is input, a chip select terminal CS, an address terminal ADR, a read terminal RD, a write terminal WT, and a data terminal DATA.

[0013] The intelligent input/output device 12 includes a shared memory 21 that stores input/output data, a control unit (hereinafter referred to as an arbitration control circuit 22) that arbitrates master MPUs when competing access to the shared memory 21, and master MPUs 23-1 to 23-n that control data input and output to and from the controlled device DEV1.

[0014] The arbitration control circuit 22 includes a first access temporary latching processing unit 31 that temporarily latches access data to the shared memory 21 from the master MPU 11A of the host controller 11, a second access temporary latching processing unit 32 that temporarily latches access data from the master MPUs 23-1 to 23-n to the shared memory 21, and an access pattern

analyzer 33 that analyzes an access pattern to the shared memory 21 on the basis of the access data latched by the first access temporary latching processing unit 31 and the access data latched by the second access temporary latching processing unit 32.

[0015] The arbitration control circuit 22 further includes an address switching processing unit 34 that switches a read address or a write address of the shared memory 21 to address data stored in the first access temporary latching processing unit 31 or address data stored in the second access temporary latching processing unit 32 on the basis of a result of the analysis by the access pattern analyzer 33, a command output processing unit 35 that outputs a write command, a read command, or a chip select command for the shared memory 21 on the basis of the analysis result of the access pattern analyzer 33, and a data switching processing unit 36 that switches the master MPU as a data input destination or the master MPU as a data output destination on the basis of the analysis result of the access pattern analyzer 33.

[0016] The master MPU 23-1 includes a clock terminal CLK, a ready terminal RDY to which a second ready signal RDY2 is input, a chip select terminal CS, an address terminal ADR, a read terminal RD, a write terminal WT, and a data terminal DATA.

[0017] Operations of the embodiment will be described below.

The access pattern of the intelligent input/output device 12 includes three temporally continuous access phases, T1 to T3.

[0018] FIG. 3 is a process timing chart of a data read process of the master MPU 11A and the master MPU 23-1 when the intelligent input/output device is in the T2 phase, by

way of example.

FIG. 4 is a process timing chart of a data write process of the master MPU 11A and the master MPU 23-1 when the intelligent input/output device is in the T2 phase, by way of example.

[0019] It is assumed that each of the T1 to T3 phases includes three sub phases, first to third sub phases A0 to A2 plotted in a time series. The access pattern is analyzed in the first sub phase A0, one of the master MPUs accessing the shared memory is processed in the second sub phase A1, and the other master MPU accessing the shared memory is processed in the third sub phase A2. It is assumed that the sub phases include at least one sub phase (one in this embodiment) for access pattern analysis and the number (two in this embodiment) of sub phases corresponding to the number of the master MPUs which can simultaneously access the shared memory 21.

[0020] First, the operation of the access pattern analyzer will be described below.

FIG. 5 is a diagram illustrating an access pattern analysis table.

FIG. 5 illustrates the analysis of an access pattern in the T2 phase.

In the case of the device configured as illustrated in FIG. 2, there are the following nine access patterns to the shared memory 21.

The access pattern analyzer 33 analyzes the access pattern from a combination of statuses (in positive logic [high active] "H" level indicated by "1" in FIG. 3 and "L" level indicated by "0" in FIG. 3) of the chip select terminals CS, the read terminals RD, and the write terminals WT of the master MPU 11A and the master MPU 23-1.

[0021] (1) Access pattern No. 1

Both the master MPU 11A and the master MPU 23-1 read data from the shared memory 21.

[0022] Specifically, the access pattern analyzer 33 determines access pattern No. 1 when in the master MPU 11A the chip select terminal CS = "L", the read terminal RD = "L", and the write terminal WT = "H", and in the master MPU 23-1 the chip select terminal CS = "L", the read terminal RD = "L", and the write terminal WT = "H" in an intended phase (T2 phase in this embodiment).

[0023] (2) Access pattern No. 2

Both the master MPU 11A and the master MPU 23-1 write data to the shared memory 21.

[0024] Specifically, the access pattern analyzer 33 determines access pattern No. 2 when in the master MPU 11A the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "L", and in the master MPU 23-1 the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "L" in an intended phase.

[0025] (3) Access pattern No. 3

The master MPU 11A reads data from the shared memory 21 and the master MPU 23-1 writes data to the shared memory 21.

[0026] Specifically, the access pattern analyzer 33 determines access pattern No. 3 when in the master MPU 11A the chip select terminal CS = "L", the read terminal RD = "L", and the write terminal WT = "H", and in the master MPU 23-1 the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "L" in an intended phase.

[0027] (4) Access pattern No. 4

The master MPU 11A writes data to the shared memory 21 and the master MPU 23-1 reads data from the shared memory

21.

[0028] Specifically, the access pattern analyzer 33 determines access pattern No. 4 when in the master MPU 11A the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "L", and in the master MPU 23-1 the chip select terminal CS = "L", the read terminal RD = "L", and the write terminal WT = "H" in an intended phase.

[0029] (5) Access pattern No. 5

The master MPU 11A reads data from the shared memory 21 and the master MPU 23-1 performs no operation to the shared memory 21.

[0030] Specifically, the access pattern analyzer 33 determines access pattern No. 5 when in the master MPU 11A the chip select terminal CS = "L", the read terminal RD = "L", and the write terminal WT = "H", and in the master MPU 23-1 the chip select terminal CS = "H", the read terminal RD = "H", and the write terminal WT = "H" in an intended phase.

[0031] The access pattern analyzer 33 also determines access pattern No. 5 when in the master MPU 11A the chip select terminal CS = "L", the read terminal RD = "L", and the write terminal WT = "H", and in the master MPU 23-1 the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "H" in an intended phase.

[0032] (6) Access pattern No. 6

The master MPU 23-1 reads data from the shared memory 21 and the master MPU 11A performs no operation to the shared memory 21.

[0033] Specifically, the access pattern analyzer 33 determines access pattern No. 6 when in the master MPU 11A the chip select terminal CS = "H", the read terminal RD = "H", and the write terminal WT = "H", and in the master MPU

23-1 the chip select terminal CS = "L", the read terminal RD = "L", and the write terminal WT = "H" in an intended phase.

[0034] The access pattern analyzer 33 also determines access pattern No. 6 when in the master MPU 11A the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "H", and in the master MPU 23-1 the chip select terminal CS = "L", the read terminal RD = "L", and the write terminal WT = "H" in an intended phase.

[0035] (7) Access pattern No. 7

The master MPU 11A writes data to the shared memory 21 and the master MPU 23-1 performs no operation to the shared memory 21.

[0036] Specifically, the access pattern analyzer 33 determines access pattern No. 7 when in the master MPU 11A the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "L", and in the master MPU 23-1 the chip select terminal CS = "H", the read terminal RD = "H", and the write terminal WT = "H" in an intended phase.

[0037] The access pattern analyzer 33 also determines access pattern No. 7 when in the master MPU 11A the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "L", and in the master MPU 23-1 the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "H" in an intended phase.

[0038] (8) Access pattern No. 8

The master MPU 23-1 writes data to the shared memory 21 and the master MPU 11A performs no operation to the shared memory 21.

[0039] Specifically, the access pattern analyzer 33 determines access pattern No. 8 when in the master MPU 11A the chip select terminal CS = "H", the read terminal RD =

"H", and the write terminal WT = "H", and in the master MPU 23-1 the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "L" in an intended phase.

[0040] The access pattern analyzer 33 also determines access pattern No. 8 when in the master MPU 11A the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "H", and in the master MPU 23-1 the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "L" in an intended phase.

[0041] (9) Access pattern No. 9

Neither the master MPU 23-1 nor the master MPU 11A performs any operation to the shared memory 21.

[0042] Specifically, the access pattern analyzer 33 determines access pattern No. 9 when in the master MPU 11A the chip select terminal CS = "H", the read terminal RD = "H", and the write terminal WT = "H", and in the master MPU 23-1 the chip select terminal CS = "H", the read terminal RD = "H", and the write terminal WT = "H" in an intended phase.

[0043] The access pattern analyzer 33 also determines access pattern No. 9 when in the master MPU 11A the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "H", and in the master MPU 23-1 the chip select terminal CS = "L", the read terminal RD = "H", and the write terminal WT = "H" in an intended phase.

[0044] FIG. 6 is a process flowchart of the intelligent input/output device 12.

In FIG. 6, for the purpose of simplification, the master MPU 11A is denoted by MPU1 and the master MPU 23-1 is denoted by MPU2.

First, the first access temporary latching processing unit 31 of the arbitration control circuit 22 latches

address data output from the address terminal ADR and write data output from the data terminal DATA of the master MPU 11A in the first sub phase A0 of the T2 phase (indicated by T2_A0 in FIG. 4). On the other hand, the second access temporary latching processing unit 32 of the arbitration control circuit 22 latches address data output from the address terminal ADR and write data output from the data terminal DATA of the master MPU 23-1 (Step S11).

[0045] Then, the access pattern analyzer 33 analyzes an access pattern from a combination of the statuses of the chip select terminals CS, the read terminals RD, and the write terminals WT of both the master MPU 11A and the master MPU 23-1 (Step S12).

Subsequently, the access pattern analyzer 33 determines whether the analyzed access pattern is access pattern No. 1 that both the master MPU 11A and the master MPU 23-1 read data from the shared memory 21 (Step S13).

[0046] When determining in Step S13 that the analyzed access pattern is access pattern No. 1 (Yes in Step S13), the access pattern analyzer 33 controls the address switching processing unit 34 to switch an address bus to the master MPU 11A in the second sub phase A1 of the T2 phase (indicated by T2_A1 in FIG. 4) (Step S14).

[0047] Thus, the access pattern analyzer 33 issues (outputs) a shared memory read command for the master MPU 11A as a shared memory command output (Step S15). As a result, the first access temporary latching processing unit 31 reads and latches data corresponding to the read address from the shared memory 21 (Step S16).

[0048] Subsequently, the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus to the master MPU 23-1 in the third sub phase A2 of the T2 phase (indicated by T2_A2 in FIG. 4)

(Step S17).

[0049] Thus, the access pattern analyzer 33 issues (outputs) a shared memory read command for the master MPU 23-1 as a shared memory command output (Step S18).

As a result, the second access temporary latching processing unit 32 reads and latches data corresponding to the read address from the shared memory 21 (Step S19).

[0050] The master MPU 11A reads intended data from the first access temporary latching processing unit 31, and the master MPU 23-1 reads intended data from the second access temporary latching processing unit 32, ending the processing in the T2 phase (Step S20).

[0051] The data read process in the case of access pattern No. 1 will be described in detail below with reference to FIG. 3, for example.

To allow the master MPU 11A to access the shared memory 21, the arbitration control circuit 22 sets the first ready signal RDY1 to "H" level over the T1 to T3 phases as illustrated in FIG. 3. Similarly, to allow the master MPU 23-1 to access the shared memory 21, the arbitration control circuit 22 sets the second ready signal RDY2 to "H" level over the T1 to T3 phases as illustrated in FIG. 3.

[0052] Thereby, the master MPU 11A recognizes from the first ready signal RDY1 that access to the shared memory 21 is allowed, and outputs a read address 110 of the shared memory from the address terminal ADR over the T1 to T3 phases as illustrated in FIG. 3.

[0053] Subsequently, the master MPU 11A places a read signal R in the "L" level during the T2 phase in order to notify the arbitration control circuit 22 of its readiness to read.

[0054] Meanwhile, the master MPU 23-1 recognizes from

the second ready signal RDY2 that access to the shared memory 21 is allowed, and outputs a read address 210 of the shared memory from the address terminal ADR over the T1 to T3 phases as illustrated in FIG. 3.

[0055] Subsequently, the master MPU 23-1 places a read signal R in the "L" level during the T2 phase in order to notify the arbitration control circuit 22 of its readiness to read.

Meanwhile, the first access temporary latching processing unit 31 of the arbitration control circuit 22 latches address data 110 output from the address terminal ADR of the master MPU 11A in the first sub phase A0 of the T2 phase (indicated by T2_A0 in FIG. 6). The second access temporary latching processing unit 32 of the arbitration control circuit 22 latches address data 210 output from the address terminal ADR of the master MPU 23-1.

[0056] Then, the access pattern analyzer 33 analyzes the access pattern from a combination of the statuses of the chip select terminals CS, the read terminals RD, and the write terminals WT of both the master MPU 11A and the master MPU 23-1.

[0057] Subsequently, the access pattern analyzer 33 determines, from the "L" level of the chip select terminals CS and the "L" level of the read signals R of the read terminals RD of the master MPU 11A and the master MPU 23-1 in the first sub phase A0 of the T2 phase, the access pattern as No. 1 that both the master MPU 11A and the master MPU 23-1 read data from the shared memory 21.

[0058] The access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 11A in the second sub phase A1 of the T2 phase (indicated by T2_A1 in FIG. 6).

[0059] Thus, the access pattern analyzer 33 issues

(outputs) a shared memory read command for the master MPU 11A as a shared memory command output (Step S15). As a result, the first access temporary latching processing unit 31 reads and latches read data 112 corresponding to a read address 111 from the shared memory 21 and outputs the read data 112 to the data bus.

[0060] Thus, latched read data 113 is output to the data bus of the master MPU 11A in the second to third sub phases A1 to A2 of the T2 phase (indicated by T2_A1 to T2_A2 in FIG. 6).

[0061] In this case, the latched read data 113 is continuously output to the data bus of the master MPU 11A till the end time of the T2 phase being a data read timing 114 of the master MPU 11A for a longer period than a predetermined data read setup time DRS. Thereby, the master MPU 11A can surely receive the latched read data 113.

[0062] The access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 23-1 in the third sub phase A2 of the T2 phase (indicated by T2_A2 in FIG. 6).

[0063] Thus, the access pattern analyzer 33 issues (outputs) a shared memory read command for the master MPU 23-1 as a shared memory command output. As a result, the second access temporary latching processing unit 32 reads and latches read data 212 corresponding to a read address 211 from the shared memory 21 and outputs the read data 212 to the data bus.

[0064] Thus, latched read data 213 is output to the data bus of the master MPU 23-1 in the third sub phases A2 of the T2 phase (indicated by T2_A1 to T2_A2 in FIG. 6).

[0065] In this case, the latched read data 213 is continuously output to the data bus of the master MPU 23-1 till the end time of the T2 phase being a data read timing

214 of the master MPU 23-1 for a longer period than the predetermined data read setup time DRS. Thereby, the master MPU 23-1 can surely receive the latched read data 213.

[0066] The processing is now described referring back to FIG. 6.

When determining in Step S13 that the analyzed access pattern is not access pattern No. 1 (No in Step S13), the access pattern analyzer 33 determines whether the analyzed access pattern is access pattern No. 2 that both the master MPU 11A and the master MPU 23-1 write data to the shared memory 21 (Step S21).

[0067] When determining in Step S21 that the analyzed access pattern is access pattern No. 2 (Yes in Step S21), the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 11A in the second sub phase A1 of the T2 phase (Step S22).

[0068] Thus, the access pattern analyzer 33 issues (outputs) a shared memory write command for the master MPU 11A to the shared memory 21 as a shared memory command output (Step S23).

As a result, the first access temporary latching processing unit 31 writes data of the master MPU 11A to an area of the shared memory 21 corresponding to the write address (Step S24).

Subsequently, the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 23-12 in the third sub phase A2 of the T2 phase (Step S25).

[0069] Thus, the access pattern analyzer 33 issues (outputs) a shared memory write command for the master MPU 23-1 to the shared memory 21 as a shared memory command

output (Step S26).

As a result, the second access temporary latching processing unit 32 writes data of the master MPU 23-1 to an area of the shared memory 21 corresponding to the read address(Step S27).

[0070] The data write process in the case of access pattern No. 2 will be described in detail below with reference to FIG. 4, for example.

The arbitration control circuit 22 places the first ready signal RDY1 in the "H" level over the T1 to T3 phases as illustrated in FIG. 4 in order to permit the master MPU 11A to access the shared memory 21. Similarly, the arbitration control circuit 22 places the second ready signal RDY2 in the "H" level over the T1 to T3 phases as illustrated in FIG. 4 in order to permit the master MPU 23-1 to access the shared memory 21.

[0071] Thus, the master MPU 11A recognizes from the first ready signal RDY1 that the access to the shared memory 21 is allowed, and outputs a write address 120 of the shared memory from the address terminal ADR over the T1 to T3 phases as illustrated in FIG. 4.

[0072] Subsequently, the master MPU 11A places a write signal W in the "L" level during the T2 phase in order to notify the arbitration control circuit 22 of its readiness to write.

[0073] Meanwhile, the master MPU 23-1 recognizes from the second ready signal RDY2 that the access to the shared memory 21 is allowed, and outputs a write address 220 of the shared memory from the address terminal ADR over the T1 to T3 phases as illustrated in FIG. 4.

[0074] Subsequently, the master MPU 23-1 places a write signal W in the "L" level during the T2 phase in order to notify the arbitration control circuit 22 of its readiness

to write.

Meanwhile, the first access temporary latching processing unit 31 of the arbitration control circuit 22 latches address data 120 output from the address terminal ADR of the master MPU 11A in the first sub phase A0 of the T2 phase (indicated by T2_A0 in FIG. 6). The second access temporary latching processing unit 32 of the arbitration control circuit 22 latches address data 220 output from the address terminal ADR of the master MPU 23-1.

[0075] Then, the access pattern analyzer 33 analyzes the access pattern from a combination of the statuses of the chip select terminals CS, the read terminals RD, and the write terminals WT of both the master MPU 11A and the master MPU 23-1.

[0076] Subsequently, the access pattern analyzer 33 determines the access pattern as No. 2 that both the master MPU 11A and the master MPU 23-1 write data to the shared memory 21, from the "L" level of the chip select terminals CS and the "L" level of the write signals W of the write terminals WT of the master MPU 11A and the master MPU 23-1 in the first sub phase A0 of the T2 phase.

[0077] The access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 11A in the second sub phase A1 of the T2 phase (indicated by T2_A1 in FIG. 6).

[0078] Thus, the access pattern analyzer 33 issues (outputs) a shared memory write command for the master MPU 11A as a shared memory command output. The first access temporary latching processing unit 31 outputs the write address 120 and corresponding write data 122 to the shared memory 21 as a write address 121 and write data 123.

[0079] Because of this, the write signal W to the shared memory 21 turns to the "L" level and the write data 123 is

written to an area corresponding to the write address 121 in the second sub phase A1 of the T2 phase (indicated by T2_A1 in FIG. 6).

[0080] The access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 23-1 in the third sub phase A2 of the T2 phase (indicated by T2_A2 in FIG. 6).

[0081] Thus, the access pattern analyzer 33 issues (outputs) a shared memory write command for the master MPU 23-1 as a shared memory command output. The second access temporary latching processing unit 32 outputs the write address 220 and corresponding write data 222 to the shared memory 21 as a write address 221 and write data 223.

[0082] Thus, the write signal W to the shared memory 21 turns to the "L" level and the write data 223 is written to an area corresponding to the write address 221 in the third sub phase A2 of the T2 phase (indicated by T2_A2 in FIG. 6).

[0083] The processing is now described referring back to FIG. 6 again.

When determining in Step S21 that the analyzed access pattern is not access pattern No. 2 (No in Step S21), the access pattern analyzer 33 determines whether the analyzed access pattern is access pattern No. 3 that the master MPU 11A reads data from the shared memory 21 and the master MPU 23-1 writes data to the shared memory 21 (Step S31).

[0084] When determining in Step S31 that the analyzed access pattern is access pattern No. 3 (Yes in Step S31), the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 11A in the second sub phase A1 of the T2 phase (Step S32).

[0085] Thus, the access pattern analyzer 33 issues (outputs) a shared memory read command for the master MPU

11A as a shared memory command output (Step S33).

As a result, the first access temporary latching processing unit 31 reads and latches data corresponding to the read address from the shared memory 21 (Step S34).

[0086] Subsequently, the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the second access temporary latching processing unit 32 of the master MPU 23-1 in the third sub phase A2 of the T2 phase (Step S35).

[0087] Thus, the access pattern analyzer 33 issues (outputs) a shared memory write command for the master MPU 23-1 to the shared memory 21 as a shared memory command output (Step S36).

As a result, the second access temporary latching processing unit 32 writes data of the master MPU 23-1 to an area of the shared memory 21 corresponding to the write address (Step S37).

[0088] The master MPU 11A reads intended data from the first access temporary latching processing unit 31, ending the process in the T2 phase (Step S38).

[0089] When determining in Step S31 that the analyzed access pattern is not access pattern No. 3 (No in Step S31), the access pattern analyzer 33 determines whether the analyzed access pattern is access pattern No. 4 that the master MPU 11A writes data to the shared memory 21 and the master MPU 23-1 reads data from the shared memory 21 (Step S41).

[0090] When determining in Step S41 that the analyzed access pattern is access pattern No. 4 (Yes in Step S41), the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 23-1 in the second sub phase A1 of the T2 phase (Step S42).

[0091] Thus, the access pattern analyzer 33 issues (outputs) a shared memory read command for the master MPU 23-1 as a shared memory command output (Step S43).

As a result, the second access temporary latching processing unit 32 reads and latches data corresponding to the read address from the shared memory 21 (Step S44).

[0092] Subsequently, the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the first access temporary latching processing unit 31 of the master MPU 11A in the third sub phase A2 of the T2 phase (Step S45).

[0093] Thus, the access pattern analyzer 33 issues (outputs) a shared memory write command for the master MPU 11A to the shared memory 21 as a shared memory command output (Step S46).

As a result, the first access temporary latching processing unit 31 writes data of the master MPU 11A to an area of the shared memory 21 corresponding to the write address (Step S47).

[0094] The master MPU 11A reads intended data from the second access temporary latching processing unit 32, ending the process in the T2 phase (Step S48).

[0095] When determining in Step S41 that the analyzed access pattern is not access pattern No. 4 (No in Step S41), the access pattern analyzer 33 determines whether the analyzed access pattern is access pattern No. 5 that the master MPU 11A reads data from the shared memory 21 and the master MPU 23-1 performs no operation to the shared memory 21 (Step S51).

[0096] When determining in Step S51 that the analyzed access pattern is access pattern No. 5 (Yes in Step S51), the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and

the data bus to the master MPU 11A in the second sub phase A1 of the T2 phase (Step S52).

[0097] Thus, the access pattern analyzer 33 issues (outputs) a shared memory read command for the master MPU 11A as a shared memory command output (Step S53).

As a result, the first access temporary latching processing unit 31 reads and latches data corresponding to the read address from the shared memory 21 (Step S54).

[0098] Subsequently, the master MPU 11A reads intended data from the first access temporary latching processing unit 31, ending the process in the T2 phase (Step S55).

[0099] When determining in Step S51 that the analyzed access pattern is not access pattern No. 5 (No in Step S51), the access pattern analyzer 33 determines whether the analyzed access pattern is access pattern No. 6 that the master MPU 23-1 reads data from the shared memory 21 and the master MPU 11A performs no operation to the shared memory 21 (Step S61).

[0100] When determining in Step S61 that the analyzed access pattern is access pattern No. 6 (Yes in Step S61), the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 23-1 in the second sub phase A1 of the T2 phase (Step S62).

[0101] Thus, the access pattern analyzer 33 issues (outputs) a shared memory read command for the master MPU 23-1 as a shared memory command output (Step S63).

As a result, the second access temporary latching processing unit 32 reads and latches data corresponding to the read address from the shared memory 21 (Step S64).

[0102] Subsequently, the master MPU 23-1 reads intended data from the second access temporary latching processing unit 32, ending the process in the T2 phase (Step S65).

[0103] When determining in Step S61 that the analyzed access pattern is not access pattern No. 6 (No in Step S61), the access pattern analyzer 33 determines whether the analyzed access pattern is access pattern No. 7 that the master MPU 11A writes data to the shared memory 21 and the master MPU 23-1 performs no operation to the shared memory 21 (Step S71).

[0104] When determining in Step S71 that the analyzed access pattern is access pattern No. 7 (Yes in Step S71), the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 11A in the second sub phase A1 of the T2 phase (Step S72).

[0105] Thus, the access pattern analyzer 33 issues (outputs) a shared memory write command for the master MPU 11A to the shared memory 21 as a shared memory command output (Step S73).

As a result, the first access temporary latching processing unit 31 writes data of the master MPU 11A to an area of the shared memory 21 corresponding to the write address, ending the process in the T2 phase (Step S74).

[0106] When determining in Step S71 that the analyzed access pattern is not access pattern No. 7 (No in Step S71), the access pattern analyzer 33 determines whether the analyzed access pattern is access pattern No. 8 that the master MPU 23-1 writes data to the shared memory 21 and the master MPU 11A performs no operation to the shared memory 21 (Step S81).

[0107] When determining in Step S81 that the analyzed access pattern is access pattern No. 8 (Yes in Step S81), the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 23-1 in the second sub phase

A1 of the T2 phase (Step S82).

[0108] Thus, the access pattern analyzer 33 issues (outputs) a shared memory write command for the master MPU 23-1 to the shared memory 21 as a shared memory command output (Step S83).

As a result, the second access temporary latching processing unit 32 writes data of the master MPU 23-1 to an area of the shared memory 21 corresponding to the write address, ending the process in the T2 phase (Step S84).

[0109] When determining in Step S81 that the analyzed access pattern is not access pattern No. 8 (No in Step S81), the access pattern analyzer 33 determines the analyzed access pattern as access pattern No. 9 that neither the master MPU 23-1 nor the master MPU 11A performs any operation to the shared memory 21, therefore, performs no operation, ending the process in the T2 phase (Step S91).

[0110] As described above, according to this embodiment, the master MPUs' accessing the shared memory 21 can be considered simultaneous access in the same access phase (the T1 to T3 phases), and the master MPUs do not need to wait, thereby preventing a decrease in effective processing speed.

[0111] A program executed by the information processing device according to this embodiment is provided in an installable or executable file format on a computer-readable recording medium such as a CD-ROM, a flexible disk (FD), a CD-R, or a digital versatile disk (DVD).

[0112] The program executed by the information processing device according to this embodiment may be stored in a computer connected via a network such as the Internet and provided by downloading via the network. The program executed by the information processing device according to this embodiment may be provided or distributed

via a network such as the Internet.

The program of the information processing device according to this embodiment may be incorporated into a ROM in advance, for example.

[0113] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

[0114] The above embodiment has described an example of receiving access requests for the shared memory 21 in parallel from two master MPUs 11A and 23-1 in the same access phase. However, the same access pattern analysis can be applied to three or more master MPUs that can issue access requests in the same access phase, upon preparation of combinations of the access patterns of the three or more master MPUs.

CLAIMS

1. An information processing device that controls access from n (n being an integer equal to or greater than 2) MPUs to a shared memory, the information processing device comprising:

a control unit that analyzes an access pattern to the shared memory based on access requests to the shared memory received in parallel from the n MPUs in a same access phase, and sequentially processes, in the access phase, the received m (m being a natural number equal to or less than n) access requests in order based on the analyzed access pattern.

2. The information processing device according to claim 1, wherein the control unit includes:

a plurality of latching processing units that stores the access requests from the MPUs and data corresponding to the access requests;

an access pattern analyzer that analyzes the access pattern of the MPUs to the shared memory based on the access requests for the shared memory received in parallel from the n MPUs; and

a command output processing unit that outputs an access command to the shared memory based on a result of the analysis of the access pattern.

3. The information processing device according to claim 2, wherein the control unit includes:

an address switching processing unit that outputs, to the shared memory, address data corresponding to an access request from any of the n MPUs based on the result of the analysis of the access pattern; and

a data switching processing unit that outputs, to the

shared memory, write data corresponding to an access request from any of the n MPUs or that reads, from the shared memory, read data corresponding to an access request from any of the n MPUs, based on the result of the analysis of the access pattern.

4. The information processing device according to any one of claims 1 to 3, wherein

the access phase includes at least $(n+1)$ sub phases, and

the control unit analyzes the access pattern in the first sub phase of the access phase and sequentially processes the m access requests in the remaining n sub phases.

5. The information processing device according to any one of claims 1 to 4, wherein

at least one of the n MPUs constitutes a host controller, and

the MPUs other than the MPU constituting the host controller among the n MPUs constitute the information processing device, and control corresponding controlled devices under control of the host controller.

6. A method to be performed by an information processing device that controls access from n (n being an integer equal to or greater than 2) MPUs to a shared memory, the method comprising:

receiving access requests for the shared memory in parallel from the n MPUs in a same access phase;

analyzing an access pattern to the shared memory based on the access requests; and

sequentially processing, in the access phase, the

received m (m being a natural number equal to or less than n) access requests in order based on the analyzed access pattern.

7. A program causing a computer to control an information processing device that controls access from n (n being an integer equal to or greater than 2) MPUs to a shared memory, the program causing the computer to function as:

means for receiving access requests for the shared memory in parallel from the n MPUs in a same access phase;

means for analyzing an access pattern to the shared memory based on the access requests; and

means for sequentially processing, in the access phase, the received m (m being a natural number equal to or less than n) access requests in order based on the analyzed access pattern.