whether to replace the main repair unit with the redundant repair unit depending on the first correctable status, the second correctable status, and the first and second cumulative correctable fail bit counts and performing a repair operation depending on a result of the determining.

[0008] In some aspects, the disclosure is directed to a semiconductor memory device comprising: a main cell array including a plurality of main repair units; a redundant cell array including a plurality of redundant repair units; error correction code logic configured to correct an error of data output from each of the main and redundant repair units; and a testability block configured to detect a fail bit of each of the plurality of main repair units and the plurality of redundant repair units and to replace at least one main repair unit, in which a defect is present, with at least one redundant repair unit with reference to a number of the detected fail bits and a correction capacity of the error correction code logic.

[0009] In some aspects, the disclosure is directed to a semiconductor memory device comprising: a memory cell array including a plurality of main repair units and a plurality of redundant repair units; error correction code logic configured to perform an error detection and correction operation on data stored in the memory cell array; and a testability block configured to replace at least one main repair unit, in which a fail bit is present, with at least one redundant repair unit depending on a correction capability of the error correction code logic, wherein a fail bit count of the at least one main repair unit is greater than a fail bit count of the at least one redundant repair unit, and a fail bit of the at least one redundant repair unit is correctable by the error detection and correction operation.

WHAT IS CLAIMED IS:

1. A repair method of a semiconductor memory device which includes a memory cell array including a main cell array and a redundant cell array and error correction code (ECC) logic, the method comprising:

detecting a fail bit of each of a main repair unit of the main cell array and a redundant repair unit of the redundant cell array;

determining whether the fail bit detected from each of the main repair unit and the redundant repair unit is correctable to determine a first correctable status for the main repair unit or a second correctable status for the redundant repair unit, by using the ECC logic;

calculating a first cumulative correctable fail bit count of the main repair unit and a second cumulative correctable fail bit count of the redundant repair unit; and

determining whether to replace the main repair unit with the redundant repair unit depending on the first correctable status, the second correctable status, and the first and second cumulative correctable fail bit counts and performing a repair operation depending on a result of the determining.

2. The method of claim 1, further comprising:

when the first correctable status corresponds to an uncorrectable status and the second correctable status corresponds to a correctable status, replacing the main repair unit with the redundant repair unit.

3. The method of claim 1 or claim 2, further comprising:

when each of the first correctable status and the second correctable status corresponds to a correctable status and the first cumulative correctable fail bit count is greater than the second cumulative correctable fail bit count, replacing the main repair unit with the redundant repair unit.

4. The method of any one of claims 1 to 3, further comprising:

when each of the first correctable status and the second correctable status corresponds to a correctable status and the first cumulative correctable fail bit count is not greater than the second cumulative correctable fail bit count, blocking replacement of the main repair unit with the redundant repair unit.

5. The method of any one of claims 1 to 4, further comprising:

when the first correctable status corresponds to a non-fail bit status in which a fail bit does not exist or the second correctable status corresponds to an uncorrectable status, blocking replacement of the main repair unit with the redundant repair unit.

6. The method of any one of claims 1 to 5, wherein the determining the first correctable status and the second correctable status further comprises:

determining the first correctable status to be an uncorrectable status when at least one of a plurality of main codeword units included in the main repair unit is uncorrectable; and

determining the second correctable status to be an uncorrectable status when at least one of a plurality of redundant codeword units included in the redundant repair unit is uncorrectable.

7. The method of claim 6, wherein the first cumulative correctable fail bit count is a value of summing fail bits of the plurality of main codeword units, and the second cumulative correctable fail bit count is a value of summing fail bits of the plurality of redundant codeword units.

8. A semiconductor memory device comprising:

a main cell array including a plurality of main repair units;

a redundant cell array including a plurality of redundant repair units;

error correction code logic configured to correct an error of data output from each of the main and redundant repair units; and

a testability block configured to detect a fail bit of each of the plurality of main repair units and the plurality of redundant repair units and to replace at least one main repair unit, in which a defect is present, with at least one redundant repair unit with reference to a number of the detected fail bits and a correction capacity of the error correction code logic.

9. The semiconductor memory device of claim 8, wherein each of the plurality of main repair units or the plurality of redundant repair units includes at least one dynamic random access memory (DRAM) cell.

10. The semiconductor memory device of claim 8 or claim 9, wherein the testability block includes:

an error detection circuit configured to output first defect information by detecting the fail bit of the plurality of main repair units and to output second defect information by detecting the fail bit of the plurality of redundant repair units;

a main cell register configured to store a first address corresponding to the first defect information and the first defect information;

a redundant cell register configured to store a second address corresponding to the second defect information, and to store the second defect information; and

a repair controller configured to perform a repair operation based on a result of comparing the first defect information and the second defect information.

11. The semiconductor memory device of claim 10, wherein the first defect information includes a fail bit count or a fail bit status of each of the plurality of main repair units, and the second defect information includes a fail bit count or a fail bit status of each of the plurality of redundant repair units.

12. The semiconductor memory device of claim 11, wherein an information of a main repair unit having an uncorrectable fail bit error or a larger fail bit count is stored in the main cell register with a higher priority, and

wherein an information of a redundant unit, in which a fail bit does not exist or which has a smaller fail bit count, is stored in the redundant cell register with a higher priority.

13. The semiconductor memory device of claim 12, wherein the repair controller is further configured to replace an address of a main repair unit, which is selected according to a priority stored in each of the main cell register and the redundant cell register, with an address of a redundant repair unit.

14. The semiconductor memory device of claim 12 or claim 13, wherein each of the main cell register and the redundant cell register includes a contents addressable memory (CAM).

15. The semiconductor memory device of any one of claims 8 to 14, further comprising:

repair logic configured to repair the at least one main repair unit selected from the plurality of main repair units with the at least one redundant repair unit selected from the plurality of redundant repair units under control of the testability block.

16. A semiconductor memory device comprising:

a memory cell array including a plurality of main repair units and a plurality of redundant repair units;

error correction code logic configured to perform an error detection and correction operation on data stored in the memory cell array; and

a testability block configured to replace at least one main repair unit, in which a fail bit is present, with at least one redundant repair unit depending on a correction capability of the error correction code logic,

wherein a fail bit count of the at least one main repair unit is greater than a fail bit count of the at least one redundant repair unit, and a fail bit of the at least one redundant repair unit is correctable by the error detection and correction operation.

17. The semiconductor memory device of claim 16, wherein the at least one main repair unit is a main repair unit, which has an uncorrectable fail bit count, from among the plurality of main repair units.

18. The semiconductor memory device of claim 16 or claim 17, wherein at least one redundant repair unit of the plurality of redundant repair units does not include a fail bit.

19. The semiconductor memory device of any one of claims 16 to 18, wherein the testability block includes a contents addressable memory (CAM) that stores the fail bit count and an address of the at least one main repair unit and the fail bit count and an address of the at least one redundant repair unit.

20. The semiconductor memory device of any one of claims 16 to 19, wherein an information of a main repair unit having an uncorrectable fail bit error or a larger fail bit count is stored in a main cell register of the memory cell array with a higher priority, and

wherein information of a redundant unit, in which a fail bit does not exist or which has a smaller fail bit count, is stored in a redundant cell register of the memory cell array with a higher priority.