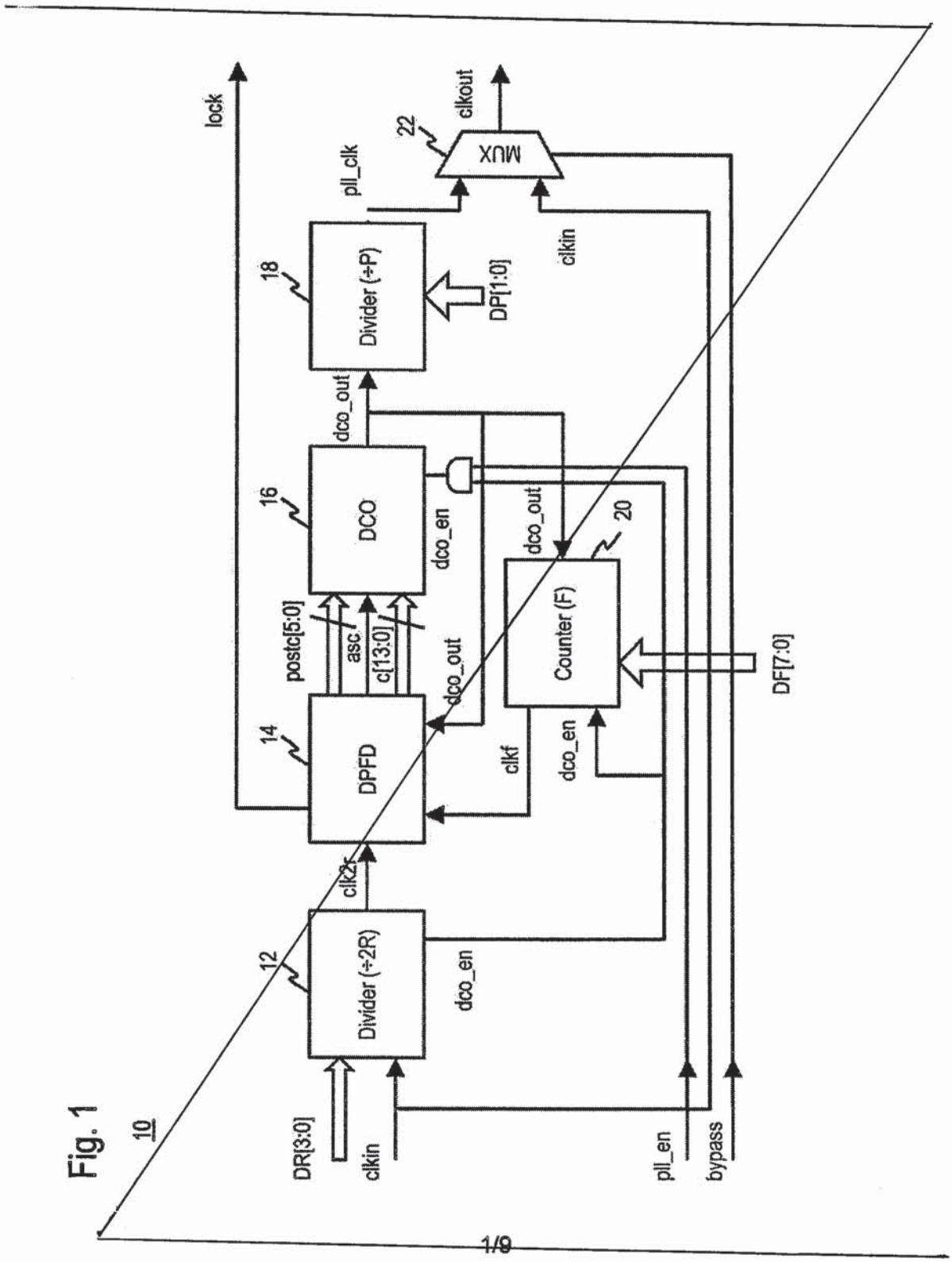
Fig. 1


10
lock
clkout
22
MUX
pll_clk
clkin
18
Divider (÷P)
DP[1:0]
dco_out
16
DCO
dco_en
dco_out
20
Counter (F)
DF[7:0]
postc[5:0]
asc
c[13:0]
dco_out
14
DPFD
clkf
dco_en
clk2x
12
Divider (÷2R)
dco_en
DR[3:0]
clkin
pll_en
bypass

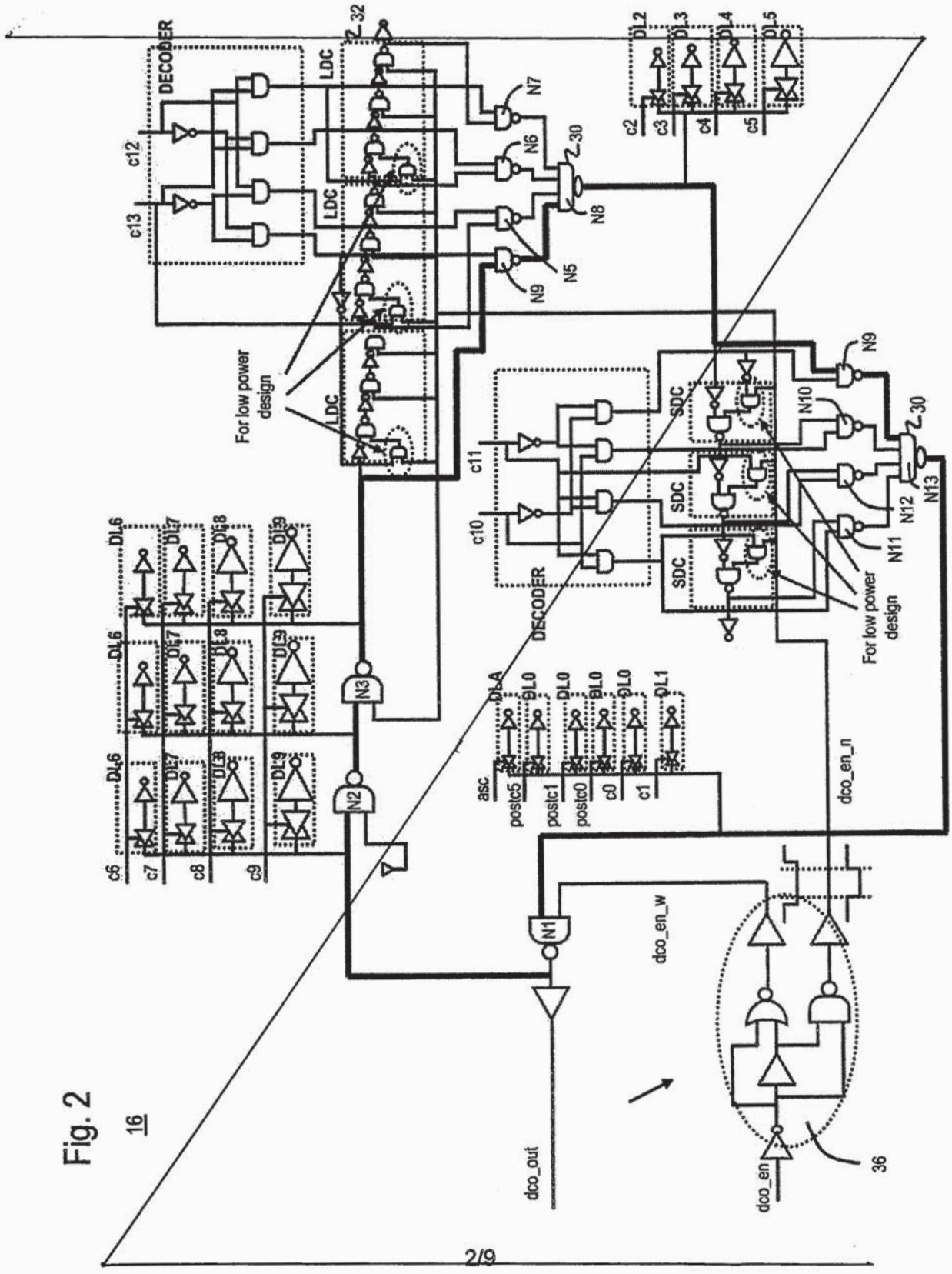

DECODER
LDC
LDC
LDC
LDC
For low power design
c12
c13
32
30
N5
N6
N7
N8
N9
DL2
DL3
DL4
DL5
c2
c3
c4
c5
DL6
DL7
DL8
DL9
c6
c7
c8
c9
N3
N2
c11
c10
SDC
SDC
SDC
DECODER
N10
N11
N12
N13
For low power design
DL-A
DL0
DL0
DL0
DL0
DL1
asc
postc5
postc1
postc0
c0
c1
dco_en_n
N1
dco_en_w
dco_out
dco_en
36
2/9

Fig. 2

16

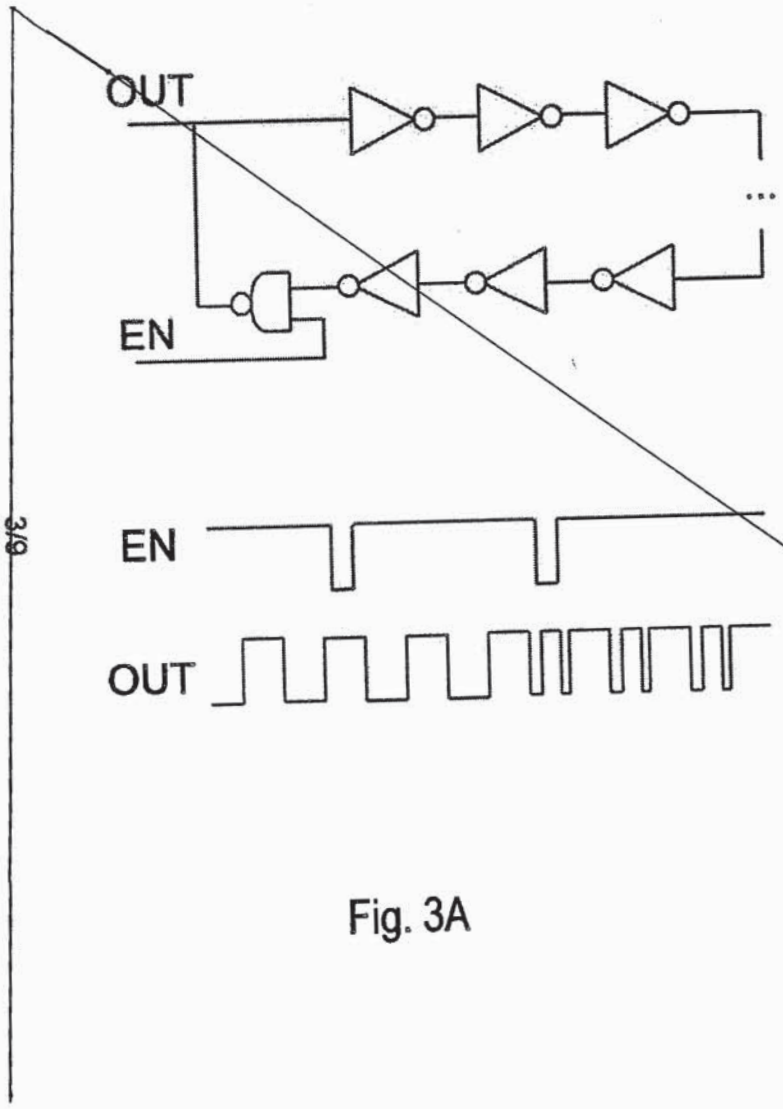

OUT
EN
EN
OUT

Fig. 3A

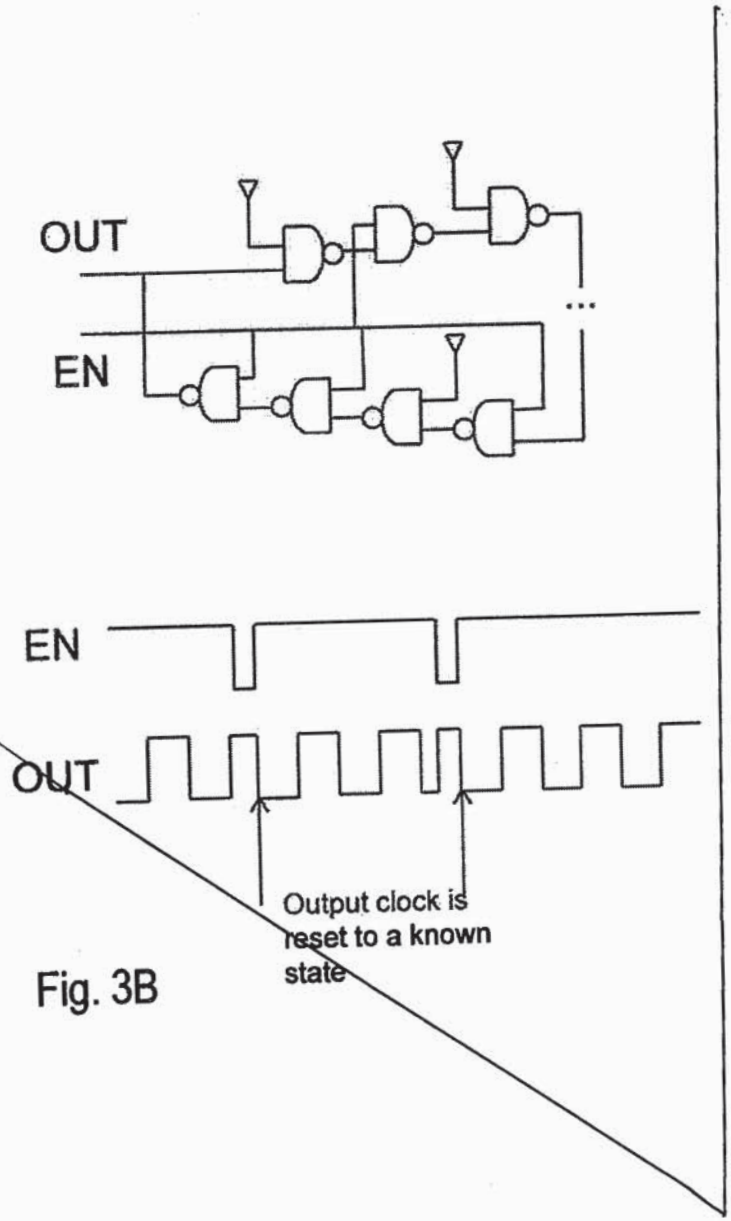
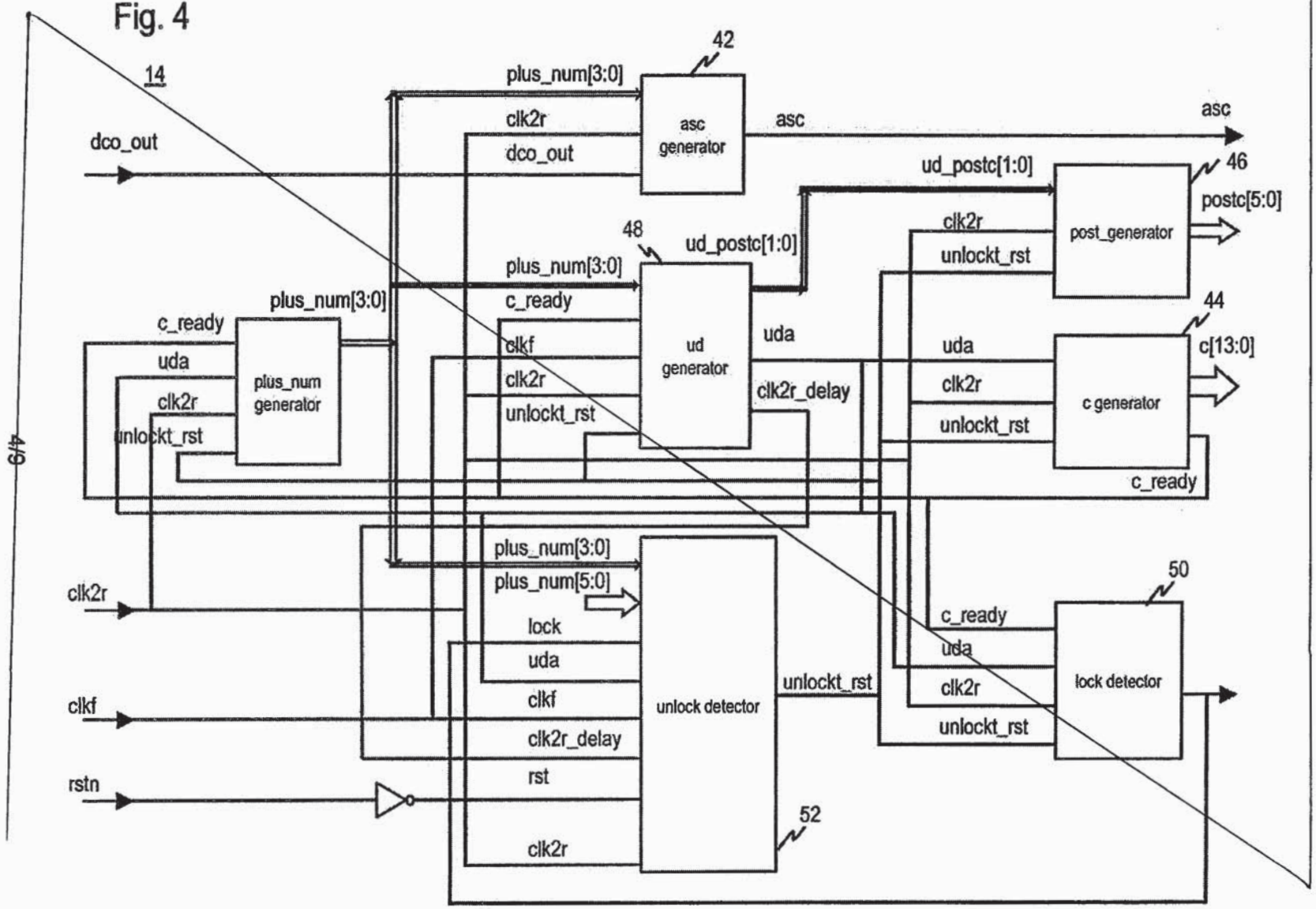

OUT
EN
EN
OUT
Output clock is reset to a known state

Fig. 3B

Fig. 4


14
42
plus_num[3:0]
clk2r
dco_out
asc generator
asc
asc
dco_out
ud_postc[1:0]
46
post_generator
postc[5:0]
clk2r
unlockt_rst
48
ud_postc[1:0]
plus_num[3:0]
c_ready
clkf
clk2r
unlockt_rst
ud generator
uda
clk2r_delay
plus_num[3:0]
c_ready
uda
clk2r
unlockt_rst
plus_num generator
44
c generator
c[13:0]
c_ready
plus_num[3:0]
plus_num[5:0]
lock
uda
clkf
clk2r_delay
rst
clk2r
unlock detector
unlockt_rst
52
50
c_ready
uda
clk2r
unlockt_rst
lock detector
clk2r
clkf
rstn
49

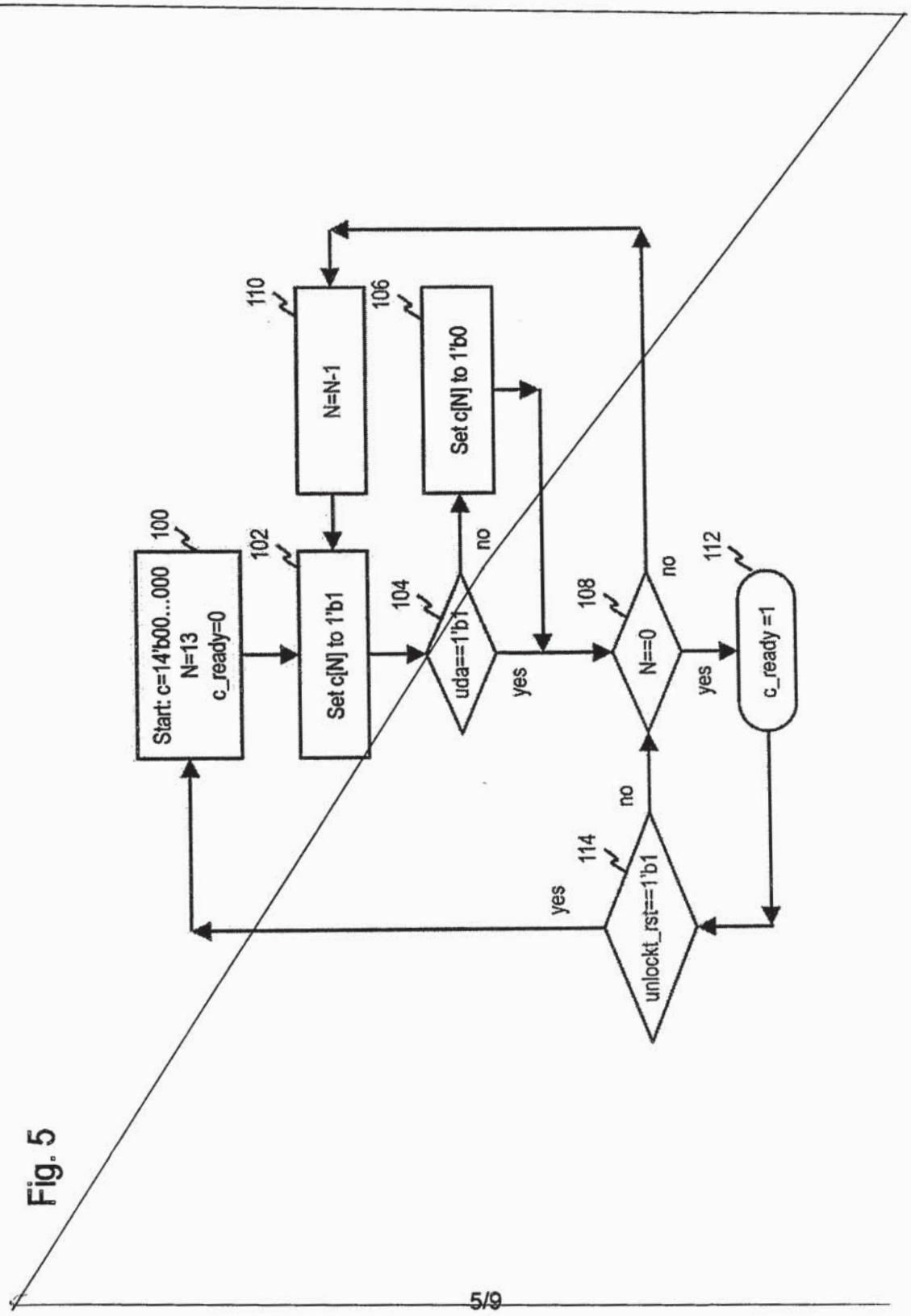
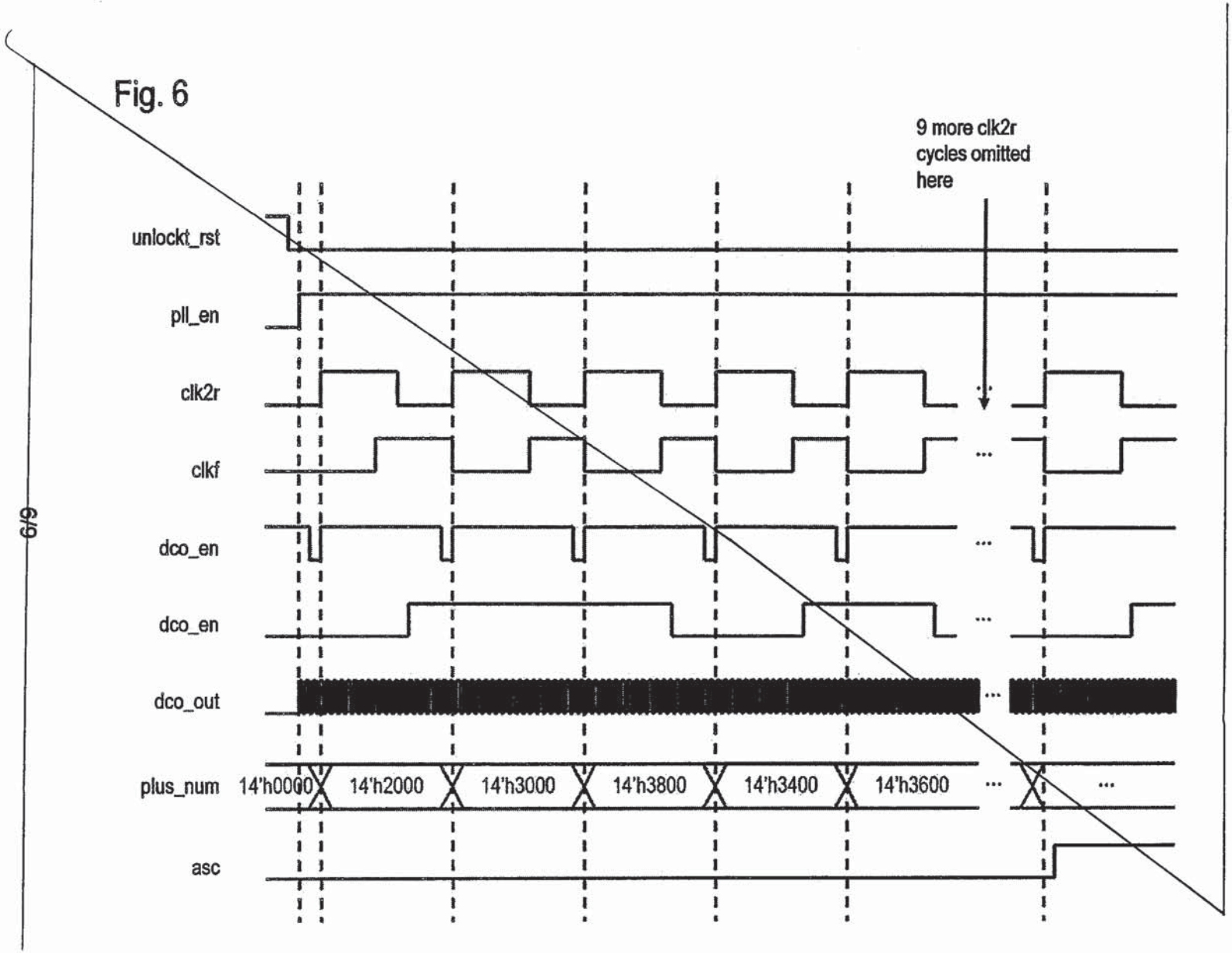

Start: c=14'b00...000
N=13
c_ready=0
100
Set c[N] to 1'b1
102
uda==1'b1
104
yes
no
Set c[N] to 1'b0
106
N=N-1
110
N==0
108
yes
no
c_ready =1
112
unlockt_rst==1'b1
114
yes
no

Fig. 5

Fig. 6


9 more clk2r cycles omitted here
unlockt_rst
pll_en
clk2r
clkf
dco_en
dco_en
dco_out
plus_num
14'h0000
14'h2000
14'h3000
14'h3800
14'h3400
14'h3600
asc

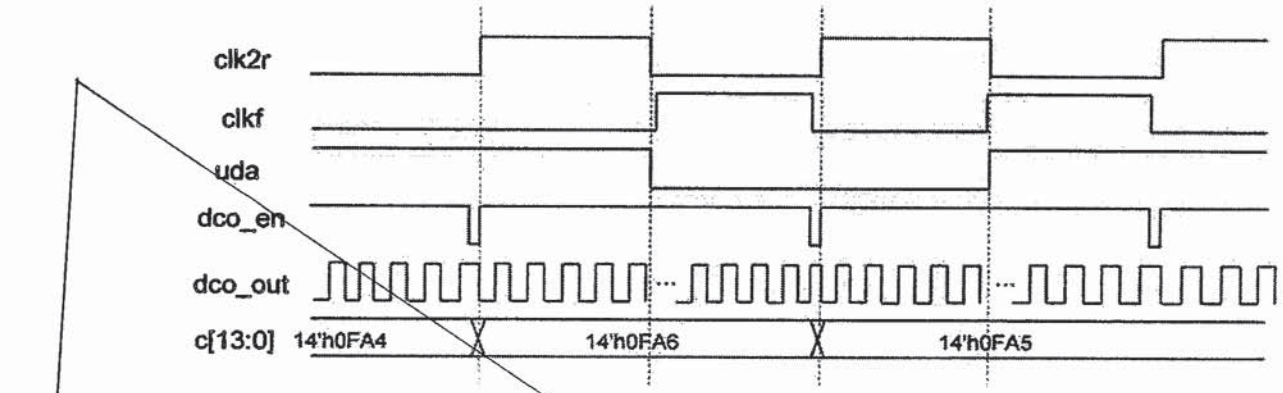

clk2r
clkf
uda
dco_en
dco_out
c[13:0]
14'h0FA4
14'h0FA6
14'h0FA5

Fig. 7A

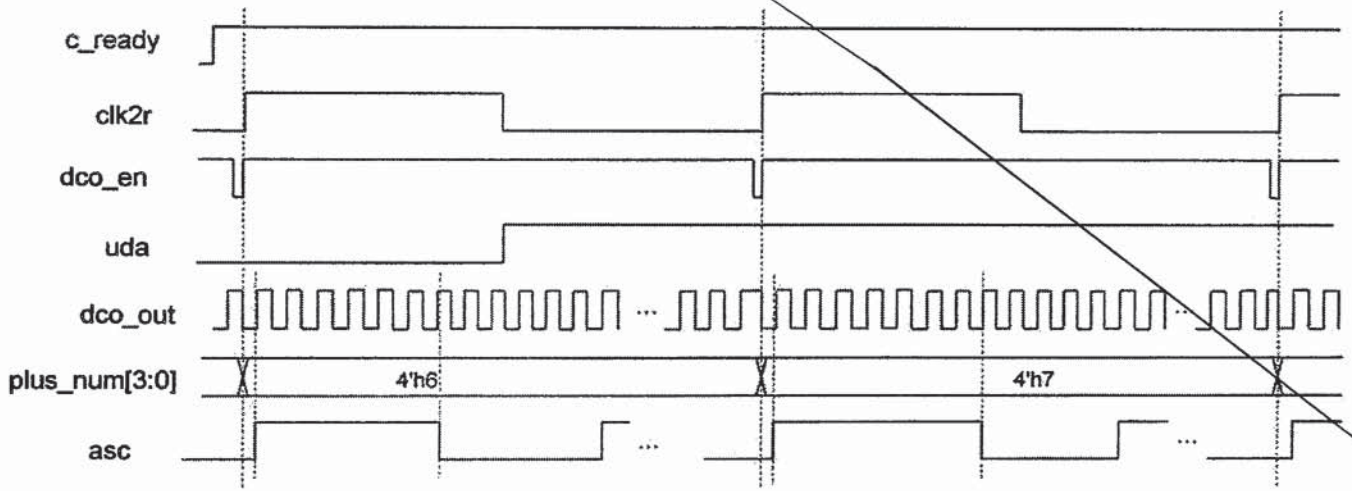
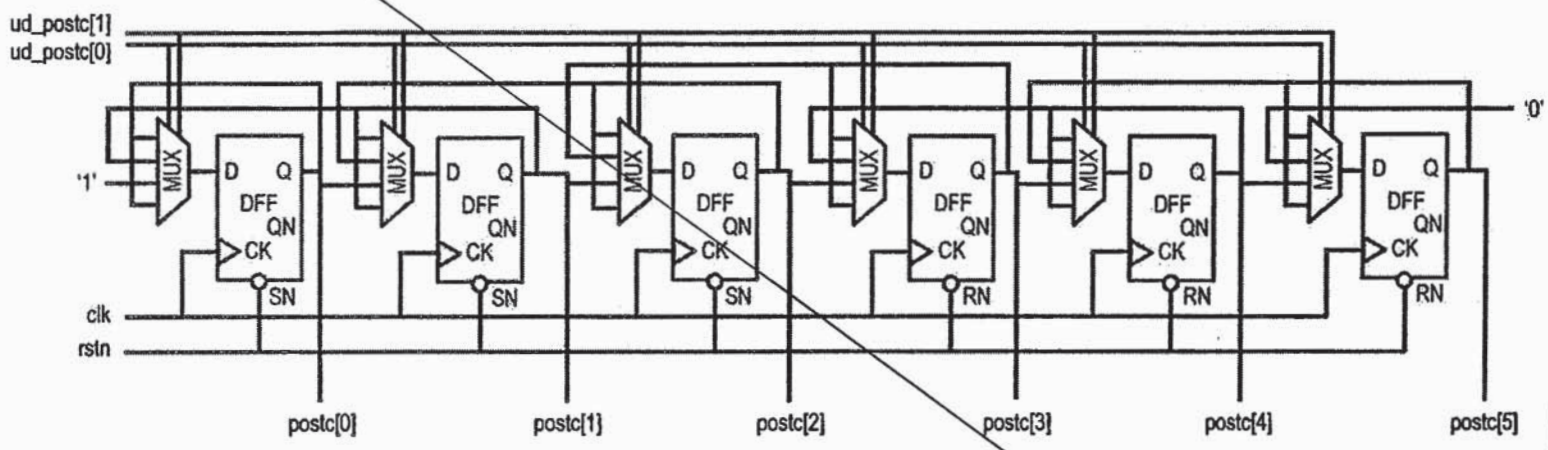

c_ready
clk2r
dco_en
uda
dco_out
plus_num[3:0]
4'h6
4'h7
asc

Fig. 7B

Fig. 8


ud_postc[1]
ud_postc[0]
'1'
'0'
MUX
D
Q
DFF
QN
CK
SN
RN
clk
rstn
postc[0]
postc[1]
postc[2]
postc[3]
postc[4]
postc[5]

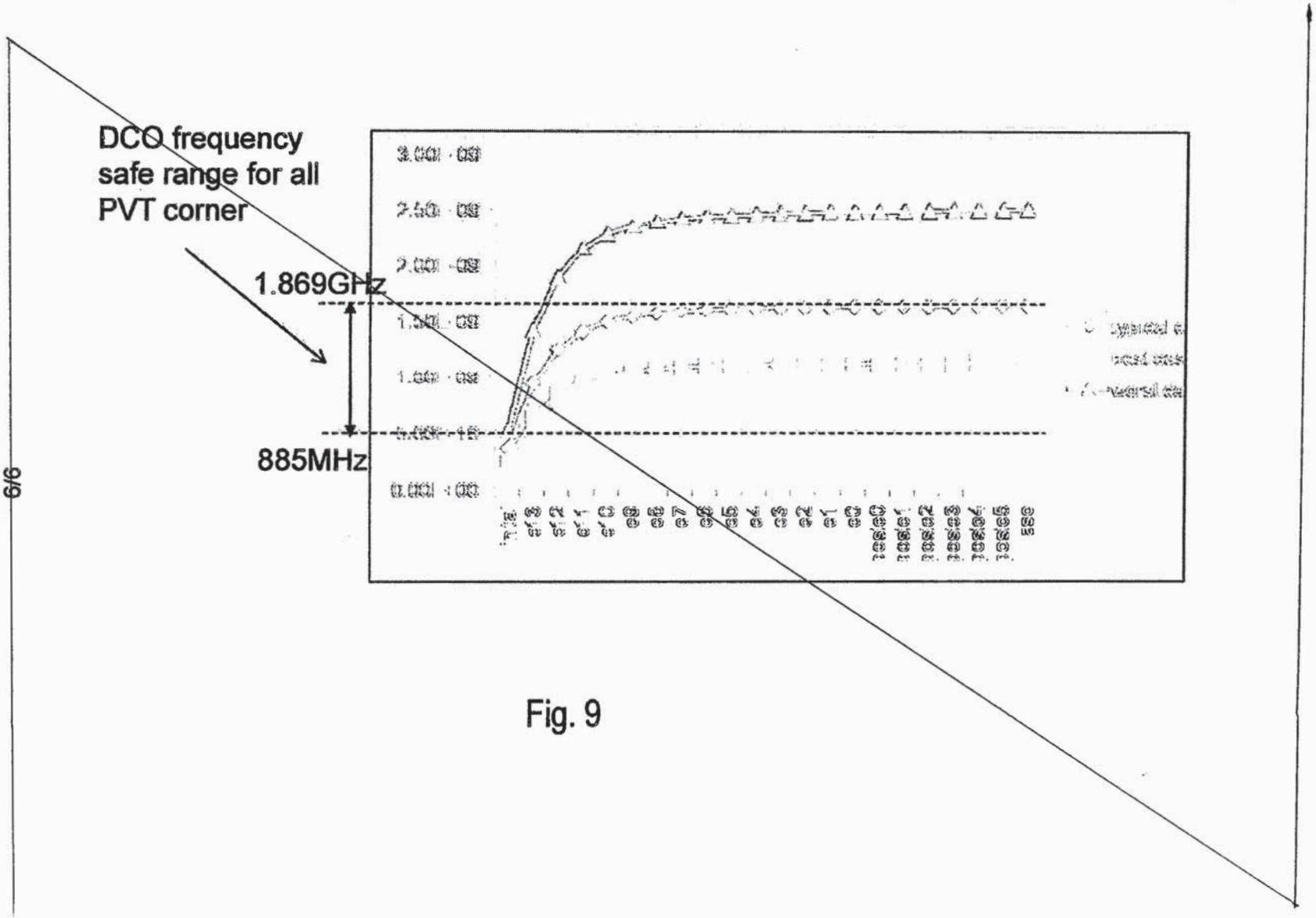


Fig. 9

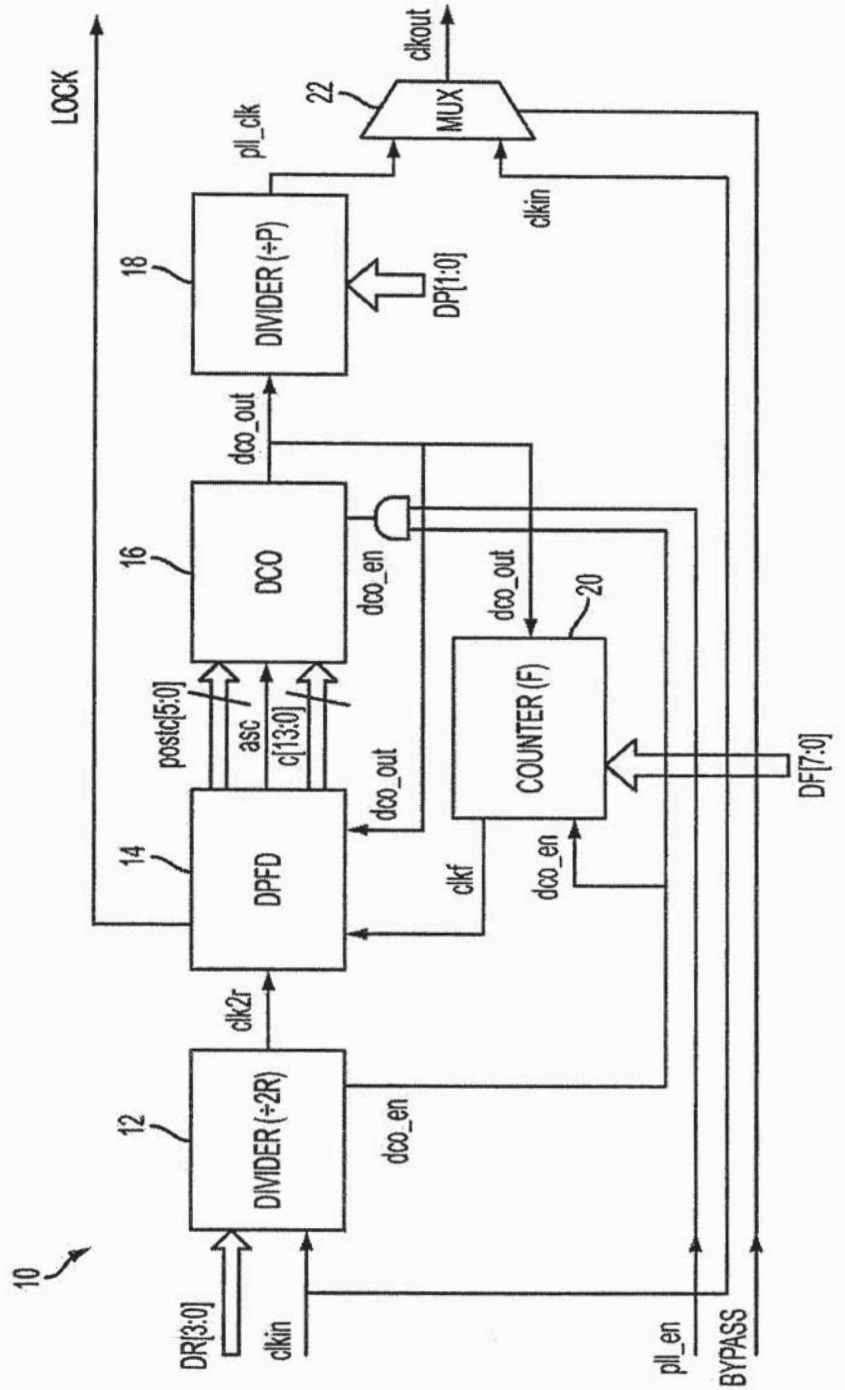

10
DR[3:0]
clkin
12
DIVIDER (÷2R)
clk2r
14
DPFD
postc[5:0]
asc
c[13:0]
16
DCO
dco_out
18
DIVIDER (÷P)
DP[1:0]
pll_clk
22
MUX
clkout
LOCK
dco_en
clkf
dco_out
COUNTER (F)
20
DF[7:0]
pll_en
BYPASS
clkin

FIG. 1

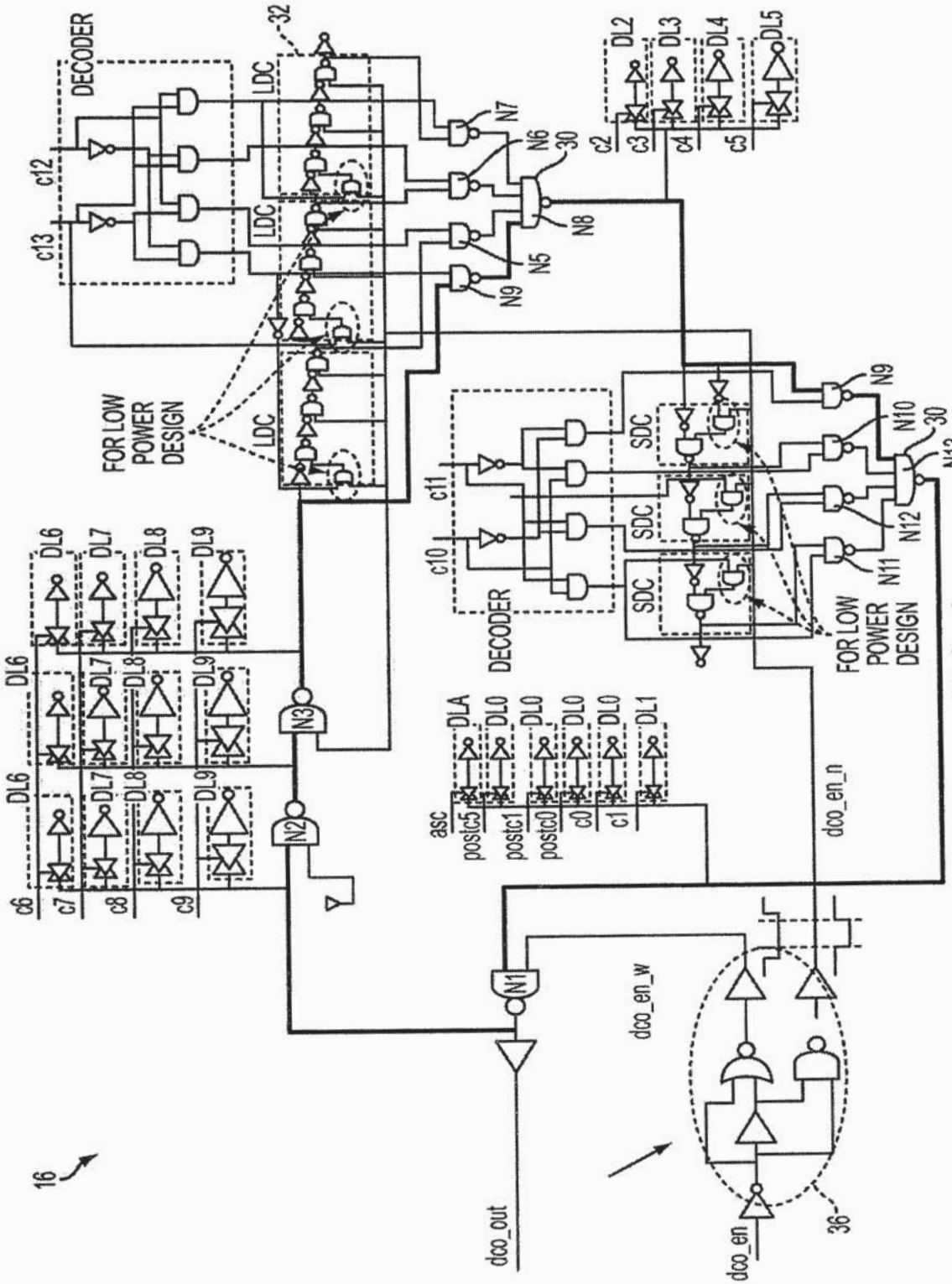

DECODER
LDC
32
c12
c13
N7
N6
30
N8
N5
N9
DL2
DL3
DL4
DL5
c2
c3
c4
c5
FOR LOW POWER DESIGN
SDC
c11
c10
N10
N12
N11
N13
DL6
DL7
DL8
DL9
c6
c7
c8
c9
N3
N2
DLA
DL0
DL1
asc
postc5
postc1
postc0
c0
c1
dco_en_n
N1
dco_en_w
dco_out
dco_en
36
16

FIG. 2

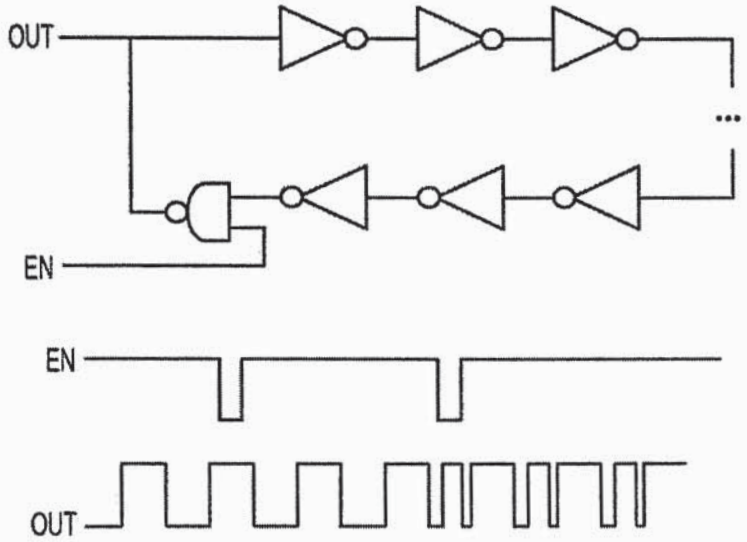

OUT
EN
EN
OUT

FIG. 3A

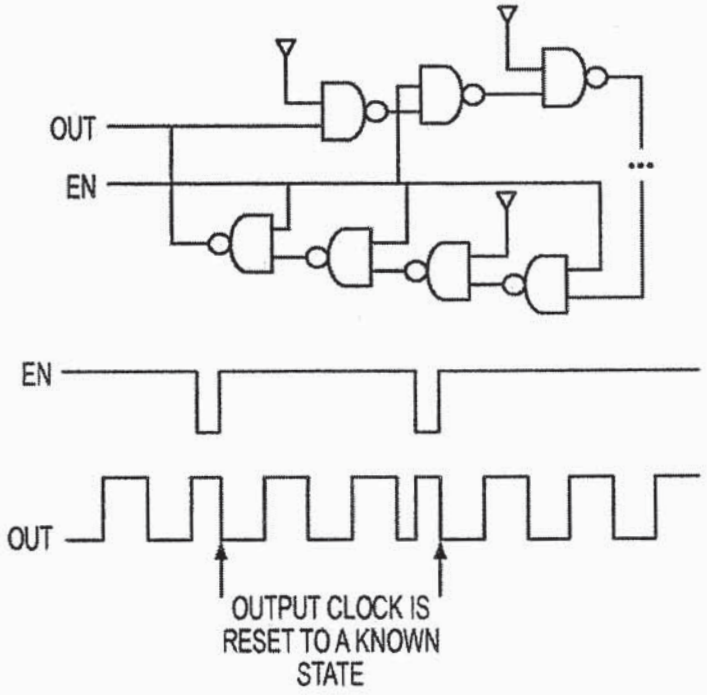

OUT
EN
EN
OUT
OUTPUT CLOCK IS RESET TO A KNOWN STATE

FIG. 3B

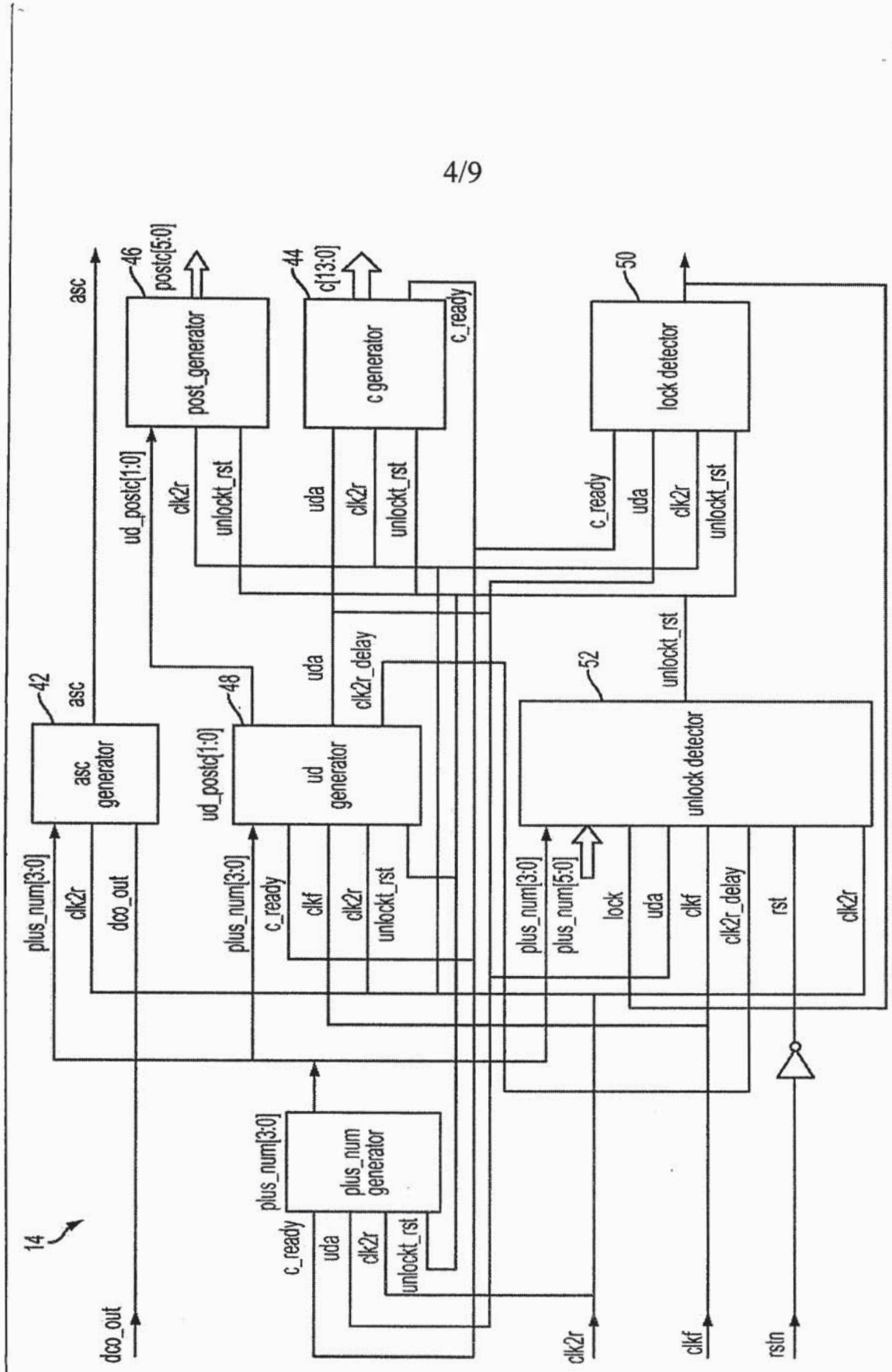

14
dco_out
asc
42
asc generator
plus_num[3:0]
clk2r
dco_out
46
postc[5:0]
post_generator
ud_postc[1:0]
clk2r
unlockt_rst
44
c[13:0]
c generator
c_ready
uda
clk2r
unlockt_rst
50
lock detector
c_ready
uda
clk2r
unlockt_rst
48
ud_postc[1:0]
ud generator
plus_num[3:0]
c_ready
clkf
clk2r
unlockt_rst
uda
clk2r_delay
52
unlock detector
unlockt_rst
plus_num[3:0]
plus_num[5:0]
lock
uda
clkf
clk2r_delay
rst
clk2r
plus_num[3:0]
plus_num generator
c_ready
uda
clk2r
unlockt_rst
clk2r
clkf
rstn

FIG. 4

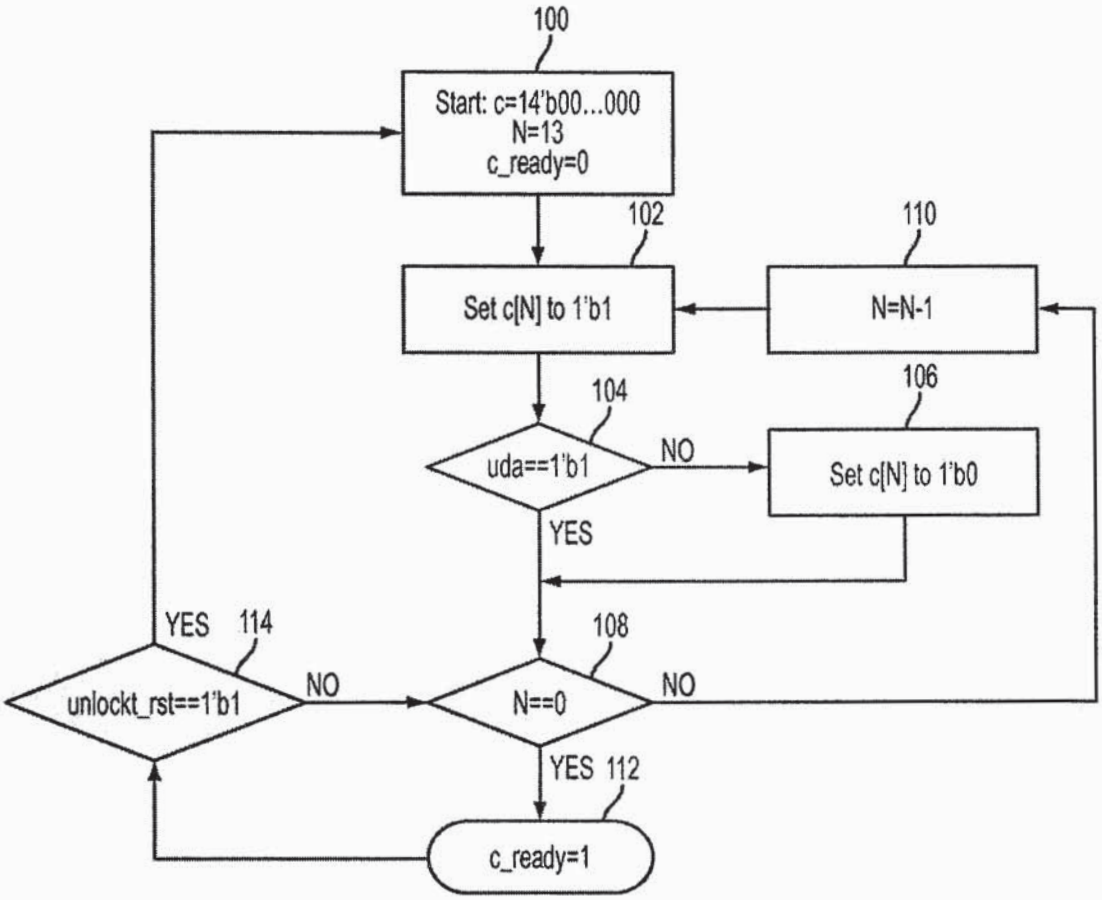

100
Start: c=14'b00...000
N=13
c_ready=0
102
Set c[N] to 1'b1
110
N=N-1
104
uda==1'b1
NO
106
Set c[N] to 1'b0
YES
YES
114
unlockt_rst==1'b1
NO
108
N==0
NO
YES
112
c_ready=1

FIG. 5

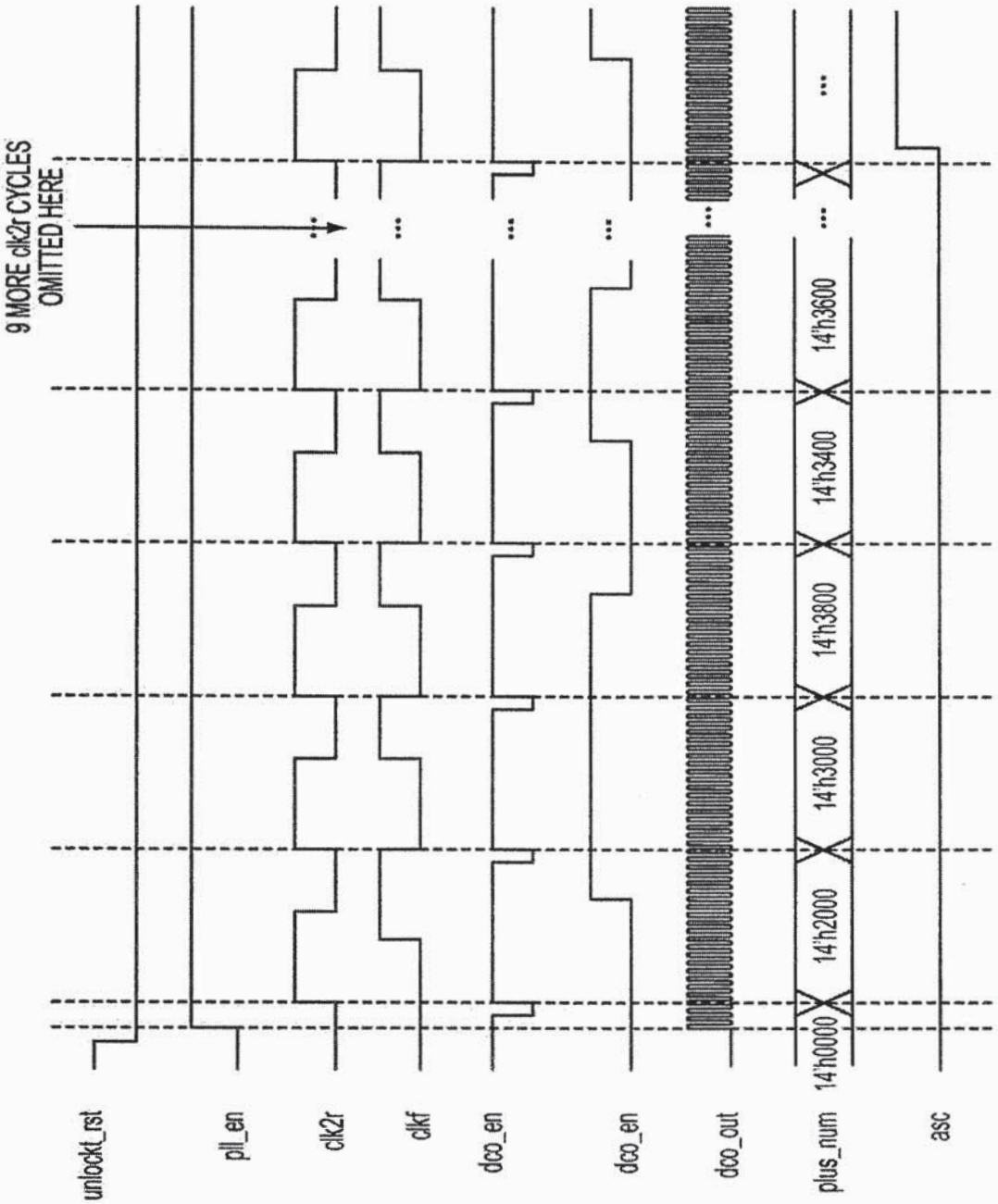

9 MORE clk2r CYCLES
OMITTED HERE
unlockt_rst
pll_en
clk2r
clkf
dco_en
dco_en
dco_out
plus_num
asc
14'h0000
14'h2000
14'h3000
14'h3800
14'h3400
14'h3600

FIG. 6

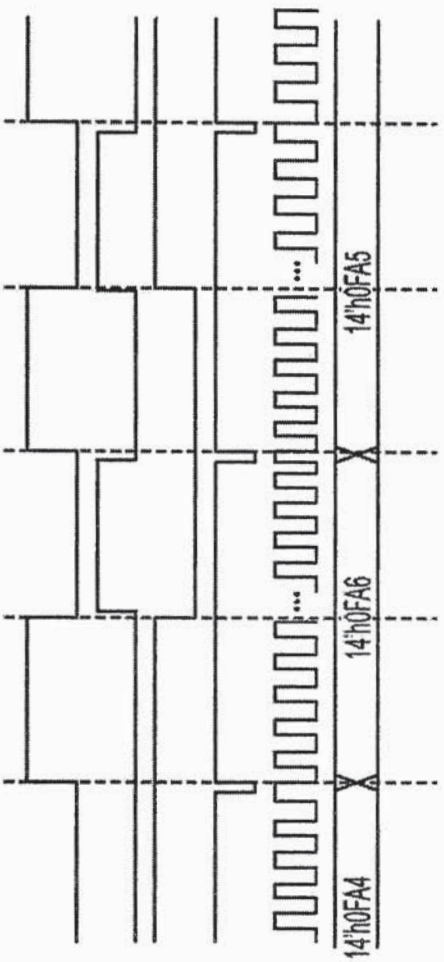

clk2r
clkf
uda
dco_en
dco_out
d[13:0]
14'h0FA4
14'h0FA6
14'h0FA5

FIG. 7A

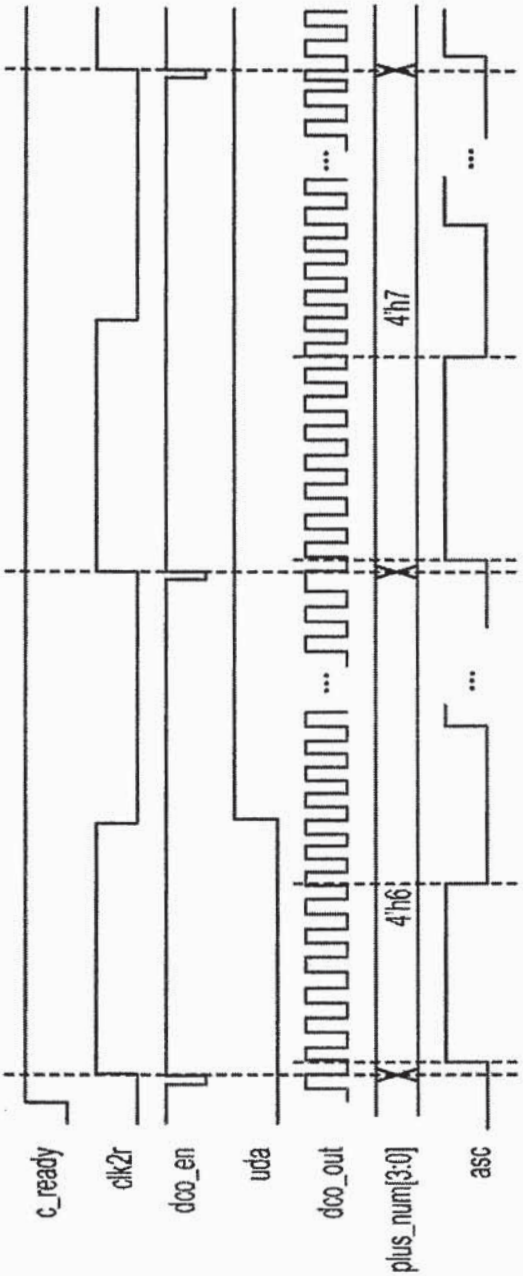

c_ready
clk2r
dco_en
uda
dco_out
plus_num[3:0]
4'h6
4'h7
asc

FIG. 7B

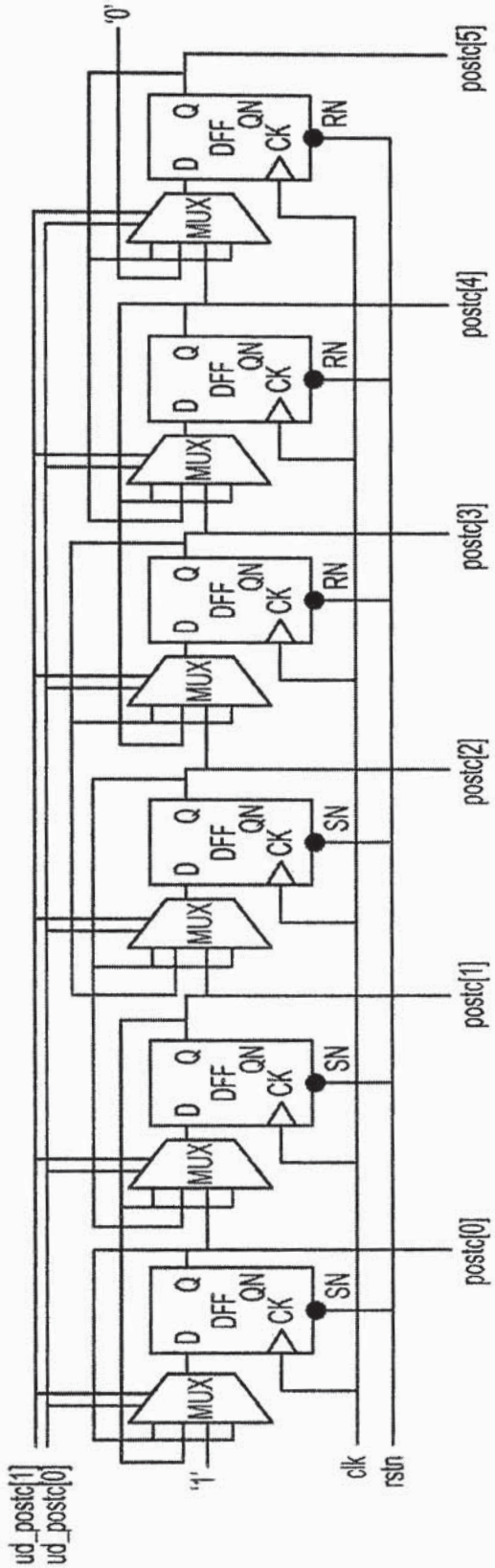

'0'
'1'
ud_postc[1]
ud_postc[0]
clk
rstn
MUX
DFF
D
Q
QN
CK
RN
SN
postc[5]
postc[4]
postc[3]
postc[2]
postc[1]
postc[0]

FIG. 8

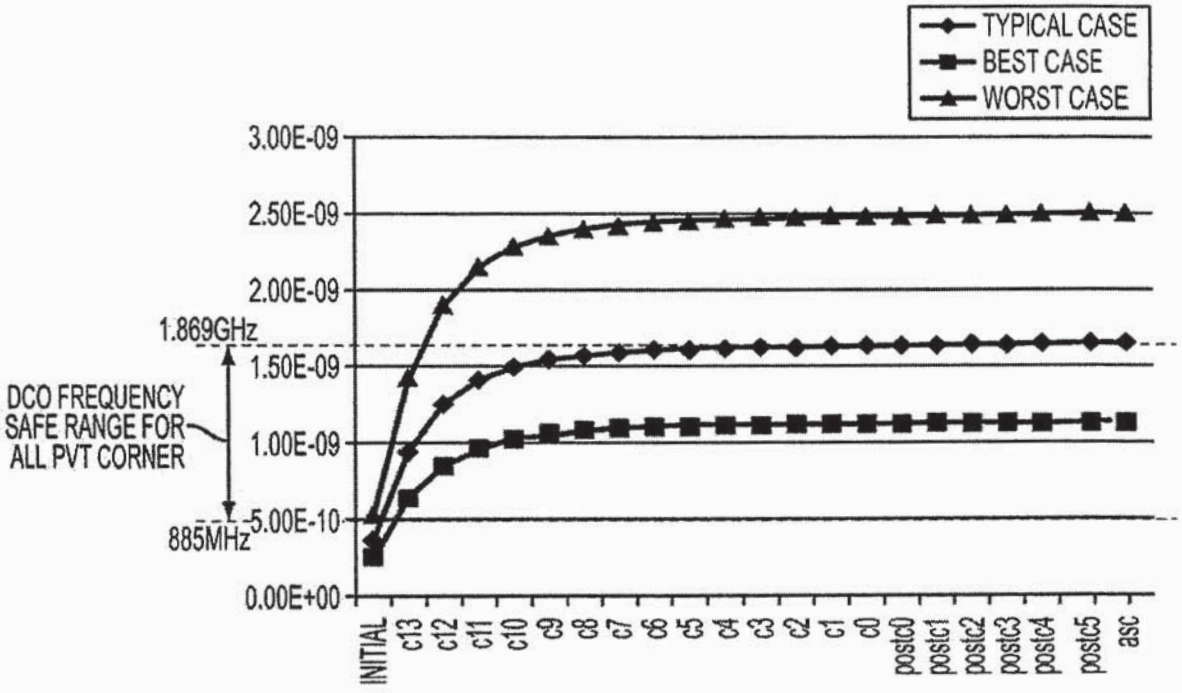

TYPICAL CASE
BEST CASE
WORST CASE
3.00E-09
2.50E-09
2.00E-09
1.869GHz
1.50E-09
1.00E-09
5.00E-10
885MHz
0.00E+00
DCO FREQUENCY
SAFE RANGE FOR
ALL PVT CORNER
INITIAL
c13
c12
c11
c10
c9
c8
c7
c6
c5
c4
c3
c2
c1
c0
postc0
postc1
postc2
postc3
postc4
postc5
asc

FIG. 9