## ABSTRACT

A memory device includes a plurality of memory cells, where each memory cell is configured to be in an erased state or one of a plurality of program states according to data stored therein. The memory device also includes a peripheral circuit configured to, in a program operation on the plurality of memory cells, perform a first program voltage application operation on first memory cells, the first memory cells being to be programmed to first respective program states. The peripheral circuit is also configured to perform, after the first program voltage application operation, a pre-program voltage application operation on second memory cells, the second memory cells being to be programmed to second respective program states.

FIG. 6B