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TITLE OF THE INVENTION

CIRCUIT ARRAY SUBSTRATE AND
FLAT PANEL DISPLAY DEVICE PROVIDED WITH THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

5 This application is based upon and claims the benefit
of priority from the prior Japanese Patent Application No.
2003-367276, filed on October 28, 2003, the entire contents of
10 which is incorporated in this application by reference.

FIELD OF THE INVENTION

This invention generally relates to a circuit array
substrate with switching elements and a flat panel display
15 device provided with such a circuit array substrate.

BACKGROUND OF THE INVENTION

A prior art flat panel display device, such as an active
matrix type liquid crystal display device (AMLCD) includes
20 amorphous silicon thin-film transistors as switching elements
of pixels because their active semiconductor layers, such as
amorphous silicon films, can be uniformly formed on a

large-area optically-transparent substrate at relatively low temperatures. Recently, thin-film transistors for driver circuits have been also formed at circumferences on the same substrate as those for such switching elements. It is disclosed
5 in Japanese Unexamined Patent Publication 2000-187248, and, particularly, at its pages 4 through 6 and Figs. 1 through 3 that the active semiconductor layers of such thin-film transistors are made from polycrystalline silicon because the mobility of the polycrystalline silicon by electric field effect is
10 greater than that of the amorphous silicon.

Since the substrate of a prior art AMLCD, however, is made of a glass plate which is optically transparent and electrical insulation, static electricity is charged on the
15 substrate. The static electricity may destroy the switching elements or the driver circuits to significantly lower a yield of the AMLCD. The static electricity has been higher as a size of the substrate has been bigger. As a result, electrostatic destruction of the switching elements and driver circuits
20 becomes a more critical problem.

When the substrate charged with static electricity, for instance, is lifted up by pins or is placed on projected pads from a grounded stage, grounded states at portions of the
25 substrate on the pins or pads differ from those of the other portions of the substrate. They cause redistribution of charges

of the static electricity so that voltages at the portions of the substrate on the pins or pads are induced several-tens of times or more than those of the other portions of the substrate.

5 In the case, particularly, that a gate insulation film is formed at small polycrystalline silicon patterns isolated from major ones on the substrate, that long gate-electrode leads are formed on the gate insulation film, and that electric capacitors are formed between the polycrystalline silicon patterns and the gate-electrode leads, such redistribution of charges
10 of the static electricity has a more adverse affect than when the substrate is lifted up by pins or is placed on projected pads from the grounded stage. Electrostatic destruction may occur between the polycrystalline silicon patterns and the gate electrode lines. In other words, it is highly possible for the static electricity to destroy the thin-film transistors.

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SUMMARY OF THE INVENTION

Accordingly, the present invention provides a circuit array substrate to prevent the occurrence of such electrostatic destruction in thin-film transistors and a flat panel display with the same.

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According to a first aspect of this invention, there is provided a circuit array substrate as defined in claim 1 of the appended claims.

According to a second aspect of this invention, there is provided a flat
5 panel display device as defined in claim 7 of the appended claims.

Since the electrode lines are separated by the separating portions, lengths of the electrode lines are shortened. Thus, when transparent substrate is lifted up while it is charged with static electricity, the increase in voltages between the electrode lines and switching elements are effectively suppressed
10 so that electrostatic destruction of the switching elements can be prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic plan view of a part of a flat panel display device in accordance with the first embodiment of the present invention;

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Fig. 2 is another schematic partial plan view of the flat panel display device shown in Fig. 1;

Fig. 3 is a schematic cross-sectional view of the flat panel display device shown in Fig. 2.;

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Fig. 4 is a schematic plan view of a part of a flat panel display device in accordance with the second embodiment of the present invention;

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Fig. 5 is a schematic cross-sectional view of the flat panel display device shown in Fig. 4;

Fig. 6 is a schematic partial plan view of a flat panel display device of the third embodiment in accordance with the present invention;

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Fig. 7 is a schematic cross-sectional view of the flat panel display shown in Fig. 6;

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Fig. 8 is a schematic plan view of a prior art flat panel

display device;

Fig. 9 is an equivalent circuit diagram of the flat panel display device shown in Fig. 8;

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Fig. 10 is an equivalent circuit of the flat panel display device shown in Fig. 8 in a state different from that in Fig. 9; and

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Fig. 11 is a characteristic curve relevant to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

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A flat panel display device such as a liquid crystal display device of the first embodiment in accordance with the present invention will be described below with reference to Figs. 1-3.

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Liquid crystal display device 1 shown in Figs. 1-3 includes top gate type or reverse-stagger type polycrystalline silicon thin-film transistors. Further, liquid crystal display device 1 is an AMLCD provided with a substantially rectangular plate-like circuit array substrate 2. Circuit array
25 substrate 2 has glass substrate 3 which is substantially rectangular and optically transparent but electrically

insulated. One main surface of glass substrate 3 includes substantially rectangular display region 4 formed on its major portion. Display region 4 is provided with a plurality of pixels 5 disposed in a dotted matrix.

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Further, display region 4 of glass substrate 3 contains gate electrode lines 11, i.e., gate electrodes of thin-film transistors and scanning lines connected to the gate electrodes. Gate electrode lines 11 are disposed in parallel
10 with the horizontal direction of glass substrate 3 and are equally spaced in the vertical direction of glass substrate 3. Common capacitor lines 12 are provided between gate electrode lines 11, are disposed in the horizontal direction of glass substrate 3 as electrode and auxiliary capacitor lines,
15 and are equally spaced in the vertical direction of glass substrate 3.

Further, signal electrode lines 13 are formed on glass substrate 3 and are disposed in the vertical direction of glass
20 substrate 3 as signal and electrode lines. Signal electrode lines 13 are made from the same materials as gate electrode lines 11 and common capacitor lines 12. Signal electrode lines 13, gate electrode lines 11 and common capacitor lines 12 each are provided for pixels 5, which are arranged in grid-like
25 structure.

Meanwhile, an undercoat film not shown but stacked with silicon nitride, silicon oxide, etc. is deposited on the main surface of glass substrate 3. Thin-film transistors 21 are formed on the undercoat film as pixel components provided for each pixel 5. Thin-film transistors 21 include polycrystalline silicon films 22 as polycrystalline semiconductor layers.

Polycrystalline semiconductor films 22 such as polycrystalline silicon (p-Si) films are made by the irradiation of excimer laser beams to anneal amorphous silicon (a-Si) films, i.e., by melting and crystallizing the a-Si films. Polycrystalline semiconductor films 22 are semiconductor patterns for thin-film transistors with which active semiconductor layers 23 are provided at the central portions as channel regions. Ohmic contact regions 24 are formed on both sides of active semiconductor layers 23 which function as source and drain electrode regions.

Gate insulation films 31 made from silicon oxide insulation films are formed on the undercoat film to cover active semiconductor layers 23 and ohmic contact regions 24 of thin-film transistors 21. A plasma chemical vapor deposition method is applied to deposit silicon oxide for gate insulation films 31 on the undercoat film.

Gate electrode lines 11 are formed on portions

corresponding to active semiconductor layer 23 of thin-film transistors 21 and are equally spaced in the lengthwise direction of active semiconductor layer 23.

5 Here, gate electrode lines 11 are separated from each other by separating portions 32 as shown in Fig. 2. Separating portions 32 are electrically discontinued between gate electrode lines 11 and are provided in the horizontal direction of gate electrode lines 11 for respective pixels 5. Separating
10 portions 32 each are disposed between thin-film transistors 21 of pixels 5 to shorten the length of each gate electrode line 11 arranged for pixel 5.

 Accumulation capacitors 34 are formed on gate
15 insulation films 31 separated from gate electrode lines 11 and are provided with common capacitors 12. Common capacitors 12 are electrically isolated from, and are disposed in parallel with, gate electrode lines 11. Here, common capacitors 12 are made from the same materials, and in the same process, as
20 gate electrode lines 11.

 Common capacitors 12 and gate electrode lines 11 are covered with interlayer insulation film 35. A plasma chemical vapor deposition is applied to deposit and stack silicon nitride
25 and silicon oxide to form interlayer insulation film 35. Further, contact holes 36 and 37 are made through gate

insulation films 31 and interlayer insulation film 35 for electric conduction.

Contact holes 36 and 37 are provided for, and
5 electrically connected to, ohmic contact regions 24 on both sides of gate electrode lines 11 of thin-film transistors 21.

Contact holes 36 are filled with electrically conductive films to connect ohmic contact regions 24 to signal electrode
10 lines 13 which function as source electrodes of thin-film transistors 21.

Further, contact holes 37 are filled with electrically conductive films to connect ohmic contact regions 24 to drain
15 electrodes 41 of thin-film transistors 21. Drain electrodes 41 face common capacitor lines 12 of accumulation capacitors 34 to define auxiliary capacitors with common capacitor lines 12 through interlayer insulation film 35. Drain electrodes 41 are placed in the same layer, made from the same materials and
20 formed by the same process as signal electrode lines 13. Thin-film transistors 21 are composed of signal electrode lines 13, drain electrodes 41, polycrystalline semiconductor films 22, gate electrode lines 11, gate insulation film 31 and interlayer insulation film 35.

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On the other hand, a pair of contact holes 38 and 39

are provided on both sides of separating portion 32 of gate electrode line 11 and are connected to edge portions of gate electrode lines 11 separated by separating portion 32. Island-like electrically conductive films 42 are filled in
5 contact holes 38 and 39 and are formed on interlayer insulation film 35 to connect one edge portion to another of gate electrode lines 11 separated by separating portions 32 through contact holes 38 and 39. Thus, electrically conductive films 42 are deposited in contact holes 38 and 39 and on
10 interlayer insulation film 35. Conductive film 42 is similar to a character of "T" in cross-section as shown in Fig. 3 by dotted lines.

In other words, parts of gate electrode lines 11 extend
15 to connect electrically conductive film 42. Conductive films 42 are placed in the same layer, made from the same materials, and formed by the same process, as signal electrode lines 13.

Signal electrode lines 13, drain electrodes 41 and
20 interlayer insulation films 35 are covered with protection film 43. Contact holes 44 are made through protection film 43 are filled with electrically conductive films as electrically conductive portions. Contact holes 44 are made to reach to drain electrodes 41 of thin-film transistors 21.

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Protection film 43 and contact holes 44 are covered

with transparent pixel electrodes 45 made from indium-tin-oxide (ITO) films. Transparent pixel electrodes 45 are electrically connected to drain electrodes 41 through contact holes 44. Further, transparent pixel electrodes 45 are disposed at places facing common capacitor lines 12 through protection film 43 and interlayer insulation film 35. Transparent pixel electrodes 45 are controlled by thin-film transistors 21 provided in pixels 5. Alignment film 46 is deposited on protection film 43.

Circuit array substrate 2 faces rectangular plate-like counter substrate 51 provided with transparent glass substrate 52. Red, green and blue dotted color filters 53 are disposed on a main surface of counter substrate 51 facing circuit array substrate 2. Those color filters 53 are provided opposite to respective pixels 5.

Rectangular plate-like counter electrode 54 is formed on a surface of color filters 53. When the surface of counter substrate 51 is opposite to that of circuit array substrate 2, rectangular counter electrode 54 entirely faces display region 4 on glass substrate 3 of array substrate 2. Alignment film 55 is formed on the surface of counter substrate 51.

Circuit array and counter substrates 2 and 51 are provided opposite to each other while alignment film 46 of

circuit array substrate 2 faces alignment film 55 of counter substrate 51. Thus, transparent pixel electrodes 45 of circuit array substrate 2 are opposite to counter electrode 54 of counter substrate 51. Liquid crystal composition 56 is held
5 between alignment films 46 of circuit array substrate 2 and alignment film 55 of counter substrate 51 as an optical modulator. Circumferences of liquid crystal composition 56 are tightly sealed.

10 A manufacturing method of circuit array substrate 2 will be described below with reference to Figs. 1-3.

First, after the formation of the undercoat film on glass substrate 3, a plasma chemical vapor deposition is
15 carried out to form an amorphous silicon film, not shown, on the undercoat film.

Excimer laser beams are then irradiated to anneal the amorphous silicon film so that the same is melted and
20 crystallized into a polycrystalline film.

Further, photolithography and etching processes are carried out to make the polycrystalline film island-like polycrystalline silicon patterns for polycrystalline silicon
25 semiconductor films 22 of thin-film transistors 21.

Next, a plasma chemical vapor deposition is applied to form gate insulation film 31 on island-like polycrystalline silicon patterns and the undercoat film.

5 Subsequently, a metal film, not shown, is deposited on gate insulation film 31. Photolithography and etching processes are then carried out for the metal film to form gate electrode lines 11 and common capacitors 12. Separating portions 32 are also provided on gate electrode lines 11.

10 Next, through a photomask of gate electrode lines 11, impurities are doped into portions where ohmic contact regions 24 are formed in polycrystalline semiconductor film 22 of thin-film transistors 21. Such doping of impurities can be
15 an ion implantation, for instance. Thermal treatment is then carried out to activate the doped impurities so that the same can become as low in electric resistance as ohmic contact regions 24 in polycrystalline semiconductor film 22 of thin-film transistors 21.

20 A plasma chemical deposition is applied to form interlayer insulation film 35 on gate electrode lines 11 and common capacitor lines 12.

25 Subsequently, photolithography and etching processes are performed to make contact holes 36 and 37 connected to

ohmic regions 24 in polycrystalline semiconductor film 22 of thin-film transistors 21 and contact holes 38 and 39 connected to the edge portions of gate electrode lines 11 separated by separating portions 32.

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Subsequently, a metal film, not shown, is deposited on contact holes 36 and 37 and interlayer insulation film 35. Photolithography and etching processes are then carried out for the metal film to form signal electrode lines 13, drain electrodes 41 and electrically conductive films 42.

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Thus, electrically conductive films 42 are extended through contact holes 36 and 37 to connect the edge portions of separated gate electrode lines 11 to each other.

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Next, protection film 43 is formed on signal electrode lines 13, drain electrodes 41, electrically conductive films 42 and interlayer insulation film 35. Photolithography and etching processes are carried out for protection film 43 to form contact holes 44 connected to drain electrodes 41.

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Further, a transparent pixel electrode layer, not shown, is formed on contact holes 44 and protection film 43. The transparent pixel electrode layer is subjected to photolithography and etching processes to form transparent pixel electrodes 45. Alignment film 46 is coated on pixel

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electrodes 45 and protection film 43 to complete circuit array substrate 2.

Alignment film 46 of circuit array substrate 2 is then
5 provided opposite to alignment film 55 of counter substrate 51. Circuit array substrate 2 is assembled with counter substrate 51. Subsequently, liquid crystal composition 56 is filled in a gap defined between circuit array substrate 2 and counter substrate 51, and circumferences of liquid crystal composition
10 56 are then tightly sealed.

System circuits, polarizers, a rear light source, etc., not shown, are further assembled with circuit array substrate 2 and counter substrate 51 to produce liquid crystal display
15 device 1.

As described above, according to the first embodiment, liquid crystal display device 1 includes gate electrode lines 11 separated on glass substrate 3 by separating portions 32 and
20 when gate electrode lines 11 are continuously linear, gate electrode lines 11 define auxiliary capacitors with polycrystalline semiconductor films 22 of thin-film transistors 21 unlike a prior art liquid crystal display device 1 shown in Fig. 8.

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In the prior art liquid crystal display device 1, when

glass substrate 3 is lifted up by movable pins, not shown, and grounded states of glass substrate 3 are changed, electrostatic charges are redistributed. As a result, voltages induced at gaps between gate electrode lines 11 and polycrystalline semiconductor films 22 through gate insulation film 31 may increase enough to cause electrostatic destruction of gate insulation film 31.

Here, in the case that glass substrate 3 on which polycrystalline semiconductor films 22 and gate electrode lines 11 are formed is grounded on stage 61, an equivalent circuit of display region 4 on glass substrate 3 will be explained below with reference to Fig. 9.

It is assumed in the equivalent circuit that electrostatic charge Q_0 is accumulated at gate electrode line 11, voltage V_0 occurs at gate electrode line 11, length A is a length of the first portion of gate electrode line 11 not overlapped with movable pin 62 and length B is a length of the second portion of gate electrode line 11 overlapped with movable pin 62. Further, capacitor C_a is defined between the first portion of gate electrode line 11 and stage 61 while, capacitor C_b is defined between the second portion of gate electrode line 11 and stage 61.

Since display region 4 of glass substrate 3 has

repeated layouts of the same pattern as for respective pixels, capacitor C_b is expressed by the following equation:

$$C_b = B/(A \times C_a)$$

and the relationship between electrostatic charge Q_0 and voltage V_0 is expressed by the following equation:

$$Q_0 = (C_a + C_b) \times V_0.$$

Next, another equivalent circuit of display region 4 on glass substrate 3 will be described in the case that glass substrate 3 is supported and lifted up by movable pin 62. It is assumed in the equivalent circuit as shown in Fig. 10 that gate electrode line 11 is of potential V and capacitor C_s is defined between the first portion of gate electrode lines 11 and stage 61. Even when glass substrate 3 is lifted up by movable pin 62, the following relationship is established in accordance with the principle of conservation of electric charge:

$$Q_0 = \{C_a \times C_s / (C_a + C_s) + C_b\} \times V$$

From those three equations, the following relationship is derived:

$$V/V_0 = (A + B)/\{A \times C_s / (C_a + C_s) + B\}$$

The voltage ratio V/V_0 defined immediately above will be described below in the case that a pattern of polycrystalline silicon semiconductor film 22 is formed on glass substrate 3 with a dielectric constant of "4" and a thickness of 100 nm, for instance, gate insulation film 31 is formed on polycrystalline

silicon semiconductor film 22, gate electrode lines 11 is formed on gate insulation film 31 and glass substrate 3 is lifted up by electrically conductive movable pin 62 by 50 mm.

5 At that time, while length B of gate electrode line 11 on movable pin 62 is fixed at 5 mm, the entire length of gate electrode line 11 is subjected to change. As a consequence, as shown in Fig. 11, when glass substrate 3 is lifted up by movable pin 62, it is effective to shorten the length of gate
10 electrode line 11 in order to control voltages imposed between gate electrode line 11 and movable pin 62.

 Thus, as described above, gate electrode line 11 is separated at each pixel 5 by separating portions 32 and
15 electrically conductive films 42, which are made from the same materials as signal electrode lines 13 formed on interlayer insulation film 35, connect one edge portion of separated gate electrode line 11 to another to shorten the length of gate electrode line 11 for each pixel 5.

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 As a result, the increase in voltage imposed on gate insulation film 31 between gate electrode line 11 and polycrystalline silicon semiconductor film 22 and electrostatic destruction of gate insulation film 31 is effectively suppressed
25 so that productivity of circuit array substrate 2 and liquid crystal display device 1 can be significantly improved.

Next, the second embodiment of the present invention will be described below with reference to Figs. 4 and 5.

5 Liquid crystal display device 1 shown in Fig. 4 and 5 is basically the same as liquid crystal display device 1 shown in Figs. 1-3 but separating portions 32 are provided not for every pixel 5 but for a plurality of pixels 5. Separating portions 32 are disposed at respective pixels 5 of a predetermined color,
10 for instance.

Here, dummy patterns 71 are prepared for pixels 5 where no separating portions 32 are formed. Dummy patterns 71 are the same in structure as conductive films 42. Both
15 conductive films 42 and dummy patterns are formed on interlayer insulation film 35 which is different from gate insulation film 31 on which gate electrode lines 11 are formed. Both end portions of each conductive film 42 and dummy pattern 71 are electrically connected to gate electrode line 11
20 through contact holes 72.

Thus, even though separating portion 32 are provided only for every predetermined number of pixels 5 in display region 4 of glass substrate 3, when static-electricity charged
25 glass substrate 3 moves, the increase of voltages at gate insulation film 31 between gate electrode lines 11 and

polycrystalline silicon semiconductor film 22 on glass substrate 3 can be suppressed effectively in the same way as liquid crystal display device 1 of the first embodiment shown in Figs. 1-3.

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Further, the number of separating portions 32 decreases in comparison with that of the first embodiment and, as such, malfunctions hardly occur at contact holes 72 and conductive films 42 so that the decrease in yield rate can be prevented.

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As described above, dummy patterns 71 are provided for pixels 5 where no separating portions 32 are formed and both end portions of each dummy pattern 71 are electrically connected to gate electrode lines 11. As a result, capacitors defined between transparent pixel electrodes 45 of pixels 5, where dummy patterns 71 are formed, and gate electrode lines 11 have the same capacitance as those defined between transparent pixel electrodes 45 of pixels 5, where separating portions 32 are formed and electrically connected by conductive films 42, and gate electrode lines 11. Thus, no substantially uneven display is caused by pixels 5 with dummy patterns 71 and separating portions 32 and uneven display of display region 4 on glass substrate 3 is prevented.

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Although dummy patterns 71 are formed on pixels 5

where no separating portions 32 are provided in liquid crystal display device 1 of the second embodiment, dummy patterns 71 in the third embodiment can be provided for pixels 5, the color of which is the same as that of all pixels 5 where separating portions 32 are formed as shown in Figs. 6 and 7. In this case, capacitors defined between transparent pixel electrodes 45 in pixels 5, where dummy patterns 71 are formed, and gate electrode lines 11 are equal to those defined between transparent pixel electrodes 45 in pixels 5, where separating portions 32 are formed, and gate electrode lines 11. Thus, liquid crystal display device 1 of the third embodiment has substantially the same functions as that of the second embodiment.

In the embodiments described above, separating portions 32 are provided at gate electrode lines 11 and both end portions of gate electrode line 11 separated by separating portion 32 are electrically connected to each other by conductive films 42. Separating portions 32, however, can be provided at common capacitor lines 12 and both end portions of common capacitor line 12 are connected to each other to obtain substantially the same functions as the previous embodiments.

The present invention can be also applied to other electrode lines than gate electrode lines 11, such as signal or

scanning lines connected to electrodes of thin film transistors
in a stagger type liquid crystal display device. The invention
can be applied a liquid crystal display device which makes use
of diodes or other switching elements than thin-film
5 transistors.

Further, the present invention can be applied to a
liquid crystal display device composed of amorphous silicon
thin-film transistors.

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Although, by way of example, a liquid crystal
composition 56 is held between circuit array substrate 2 and
counter substrate 51 as an optical modulator of liquid crystal
display device 1, the present invention can be applied to flat
15 panel display devices provided with other optical modulators
than liquid crystal compositions.

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CLAIMS

1. A circuit array substrate comprising:
an optically transparent substrate;
5 pixels having switching elements formed on said transparent substrate;
gate electrode lines connected to said switching elements, said gate electrode lines being provided on a first insulation film with separating portions in said pixels; signal lines connected to said switching elements,
10 said signal lines being provided on a second insulation film which is different from the first insulation film; and
electrically conductive portions provided on the second film to electrically connect said gate electrode lines with said separating portions to each other, wherein said separating portions reduce electrostatic
15 capacitances defined between said gate lines and said switching elements when said conductive portions are not connected between said separating portions.

2. A circuit array substrate according to Claim 1 wherein said
20 switching elements are disposed in a matrix form, and each of said separating portions is provided for one of said pixels.

3. A circuit array substrate according to Claim 1, further comprising dummy patterns provided for said pixels where no separating portions are provided, wherein said dummy patterns are substantially the same in shape as said conductive portions.

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4. A circuit array substrate according to Claim 1, wherein said pixels are provided for colors,

said switching elements are disposed in a matrix form and are provided for respective ones of said pixels, and

10 said separating portions are provided for every said pixel of one of said colors.

5. A circuit array substrate according to Claim 1, further comprising dummy patterns provided for said pixels where said separating
15 portions are not provided,

wherein said pixels are provided for colors,

said switching elements are disposed in a matrix form and are provided for respective ones of said pixels, and

20 said separating portions are provided for every said pixel of one of said colors.

6. A circuit array substrate according to claim 1, wherein said conductive portions are made from the same materials as said signal electrode lines.

5 7. A flat panel display device comprising:
an optically transparent substrate;
pixels having switching elements formed on said transparent substrate;
gate electrode lines connected to said switching elements, said
10 gate electrode lines being provided on a first insulation film with separating portions in said pixels;
signal lines connected to said switching elements, said signal lines being provided on a second insulation film which is different from the first insulation film;
15 electrically conductive portions provided on the second film to electrically connect said gate electrode lines with said separating portions to each other; and
an optical modulator, wherein said separating portions reduce electrostatic capacitances defined between said gate lines and said
20 switching elements when said conductive portions are not connected between said separating portions.