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(54) IMPROVEMENTS IN OR RELATING TO FLIP-FLOP CIRCUITS

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese company, of 3-4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to flip-flop circuits and has for its object to provide improved flip-flop circuits suitable for frequency dividers or ring counters which shall be of wide application, simple, reliable, easy to manufacture and such as to lend themselves to a very high degree of miniaturisation by adopting integrated circuit techniques.

According to this invention a flip-flop circuit comprises first and second positive logic NAND circuits formed from a series connection of source-drain circuits of N-channel insulating gate field effect transistors; first and second negative logic NAND circuits formed from a series connection of source-drain circuits of P-channel insulating gate field effect transistors; and an inverter circuit formed from a pair of N-channel and P-channel field effect transistors, said first and second positive logic NAND circuits being connected in parallel in an AND configuration to define a positive logic such that an output appears from this pair of NAND circuits only in the absence of a "1" signal at either gate of one series pair of transistors and a similar absence at either gate of the other series part of transistors, said first and second negative logic NAND circuits being connected in parallel in an AND configuration, to define a negative logic circuit such that an output appears from this pair of NAND circuits only in the absence of a "1" signal at either gate of one series pair of transistors and a similar absence at either gate of the other series pair of transistors the complementary positive and negative logic circuits thus formed being connected in series and disposed between the terminals of a source of potential, a connecting point terminal between said complementary positive and negative logic circuits generating a first output as well as connecting same to an input of said inverter circuit, an output of said inverter circuit generating a second output as well as connecting same to a gate of one transistor of each of said first positive and first negative logic NAND circuits, a write input being connected to a gate of one transistor of each of said second positive and second negative logic NAND circuits, a first control input being connected to a gate of one transistor of each of said first positive and second negative logic NAND circuits which gate is not connected with said second output nor with said write input, a second control input in anti-phase with said first control input being connected to a gate of one transistor of each of said second positive and first negative logic NAND circuits which gate is not connected with said second output nor with said write input.

According to another aspect of the present invention there is provided a ring counter comprising four flip-flop circuits as recited in the preceding paragraph connected in cascade. Preferably, the output of the second flip-flop circuit is fed back to the input of the first flip-flop circuit so as to form a divide-by-2 ring counter.

According to another aspect of the present invention there is provided a ring counter comprising a plurality of flip-flop circuits each as recited above connected in cascade the output of the last flip-flop circuit being fed back to the input of the first flip-flop circuit so as to form a divide-by-2N ring counter.

The invention is illustrated in and further explained in connection with the accompanying drawings, in which:—

Figure 1 shows a conventional known divide-by-two flip-flop circuit,

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Figure 2 is a block diagram of a ring counter in accordance with this invention, and

Figure 3 is a circuit diagram of the ring counter of Figure 2.

Hitherto frequency division of a relatively high frequency down to a relatively low frequency has commonly been accomplished by utilising divide-by-two flip-flop circuits as shown in Figure 1, division by the required ratios of 1/6 and 1/12 (or 1/24) being effected by feedback frequency division of some suitably chosen frequency by a dividing ratio of $(1/2)^n$. In this figure C_1 and C_2 are capacitors, R_1 , R_2 , R_3 and R_4 are resistors and T_1 and T_2 are transistors. The circuit of Figure 1 is too well known to require further description here. However, in some cases, complex requirements as regards frequency division may arise—for example, in an electronic timepiece the division of the relatively high time standard frequency of the timepiece down to relatively low frequency coded signals for actuating the time display means of said timepiece usually involves the provision of divide-by-six counters, decimal (divide-by-ten) counters and divide-by-twenty (or divide-by-twelve) counters—and such requirements as these cannot be complied with in a satisfactory manner merely by decimal counters and attempts to do so result in complex circuitry which does not lend itself to a really high degree of miniaturisation even though integrated circuit construction is employed. From this point of view divide-by- 2^n counters are much superior to divide-by- 2^n counters. Moreover, divider circuits of the kind incorporating a divide-by- 2^n counter are advantageous, as compared with divider circuits of the kind incorporating a divide-by- 2^n counter when integrated circuit construction is required. This is because, with a divide-by- 2^n counter, each flip-flop circuit can be of the same design or pattern and connection made merely by a thin metal connector. Thus the choice of this type of counter results in considerable simplification of integrated circuit construction with external wiring reduced to a minimum and all the active elements embodied and inter-connected in the structure.

Figure 2 is a block diagram of a divide-by-four divider in accordance with this invention and constituted by a two-stage ring counter. It consists of two delay circuits 9 and 10 which form the two stages and are in cascade, with the output of the second stage 10 fed back to the input of the first, the divide-by-four ring counter being thus formed by NAND and AND logic circuits. In

Figure 2 the references ϕ_1 , ϕ_2 , $\bar{\phi}_1$, $\bar{\phi}_2$

D_1 , D_2 , Q_1 , Q_2 and $\bar{Q}_1$, $\bar{Q}_2$ have their customary significance in logic circuit representation.

The detailed circuitry and construction of the divider of Figure 2 are shown in Figure 3 in which the portions indicated by the arrow headed lines 9 and 10 correspond with the blocks 9 and 10 of Figure 2. Referring to

Figure 3, ϕ and $\bar{\phi}$ are oppositely phased control inputs, 21 is a "write" input terminal and 23 is an output terminal. 16 and 17 are N-channel IGFETS the drain-source circuits of which are connected in series to form a first positive logic NAND circuit. Similarly 15 and 18 are N-channel IGFETS forming a second positive logic NAND circuit. These first and second positive logic NAND circuits are connected in parallel in an AND configuration to form a positive logic circuit such that an output appears from this pair of NAND circuits only in the absence of a "1" signal at either gate of one series pair of IGFETS and a similar absence at both gates of the other series pair of IGFETS.

12 and 14 are P-channel IGFETS the drain-source circuits of which are connected in series to form a first negative logic NAND circuit. Similarly 11 and 13 are P-channel IGFETS forming a second negative NAND circuit. These first and second negative logic NAND circuits are connected in parallel with one another in an AND configuration to form a negative logic circuit such that an output appears from this pair of NAND circuits only in the absence of a "1" signal at either gate of one series pair of IGFETS and a similar absence at both gates of the other series pair of IGFETS.

The positive logic circuit and the negative logic circuit thus formed are connected in series between voltage source terminals V_{SS} and V_L and the output terminal 22 is connected to the input of a complementary inverter composed of an N-channel IGFET 20 and a P-channel IGFET 19. The output terminal 23 of the complementary inverter is connected to the gate of an N-channel IGFET (16) belonging to the first positive logic NAND circuit and also to the gate of a P-channel IGFET (14) belonging to the first negative NAND circuit. A "write" input 21 is connected to the gate of an N-channel IGFET (15) belonging to the second positive logic NAND circuit and also to the gate of a P-channel IGFET (13) belonging to the second negative logic NAND circuit.

The control input ϕ is connected to the gate of an N-channel IGFET (17) belonging to the first positive logic NAND circuit and also to the gate of a P-channel IGFET (11) belonging to the second negative logic

NAND circuit. The control input $\bar{\phi}$ is connected to the gate of an N-channel IGFET (18) belonging to the second positive NAND circuit and also to the gate of a P-

channel IGFET (12) belonging to the first negative logic NAND circuit.

In this way there is provided a circuit constituting a flip-flop circuit which "writes" the "write" input (21) or keeps the output (23) by synchronizing with the control input ϕ (or $\bar{\phi}$).

The foregoing is a simple description of the circuitry.

The circuit block indicated by reference 9 is constituted by using the flip-flop circuits as above described as a master flip-flop circuit and a slave flip-flop circuit as indicated by the references 24 and 25 respectively. By applying the output (23) of the master flip-flop circuit 24 as the input to the slave flip-flop circuit 25 and by arrang-

ing the control inputs ϕ and $\bar{\phi}$ of the slave flip-flop circuit 25 to be in phase opposition, there is obtained a master-slave type of delay flip-flop having two-stage operation.

By connecting n stages, each similar to the circuit block 9, in cascade and driving the circuit thus formed by a common clock

signal ϕ ($\bar{\phi}$), an n -bit delay circuit is obtained. If the output is fed back to the input in the opposite phase, the circuit becomes a $2n$ divider. The arrangement actually shown in Figure 4 is a $1/4$ divider in which $n=2$.

The following brief description of the operation of a flip-flop circuit in accordance with the invention and as herein illustrated will assist in a better understanding of the said invention. The description which follows is given with respect to three different operating conditions, numbered respectively 1, 2 and 3.

Condition 1. "Write" state of data $\phi=0$

Transistors 12 and 17 are cut off and transistors 11 and 18 are conductive. Accordingly a signal applied from 21 is inverted by a series circuit comprising transistors 12, 14, 16 and 17 and appears at 22. This signal is inverted by an inverter comprising transistors 19 and 20 and appears at 23.

Condition 2. "Memory" state of data $\phi=1$

Transistors 11 and 18 are cut off and transistors 12 and 17 are conductive. Accordingly a signal appearing at 23 is inverted by a series circuit comprising transistors 12, 14, 16 and 17 and appears at 22. This signal is inverted by an inverter comprising transistors 19 and 20 and appears at 23. Because this signal is of the same polarity at that previously appearing at 23 it is held there and a "memory" state is established.

Condition 3. Transient state from $\phi=0$ to $\phi=1$

Theoretically and in principle, if an "ideal" signal wave form which can be changed instantaneously from $\phi=0$ to $\phi=1$ is assumed, the illustrated circuit can change over from the "write" state to the "memory" state without there being any parasitic capacity in the transistor gate circuit. In practice, however, the signal change from $\phi=0$ to $\phi=1$ is not instantaneous though it does not occupy more than a few microseconds and is accomplished in a limited time in an integrating circuit as usual. Capacitances C_1 and C_2 , as shown in broken lines in Figure 3, should accordingly be present so that data written in can be held during the transient state. These capacitances are shown in broken lines to indicate that they are not condensers but are necessarily present in the form of the parasitic capacitances of the transistor gates and of the wiring connected thereto, the parasitic capacitance values being, in any practical case, adequate to ensure the holding of data during the very short limited time in which the transient condition exists. It should be particularly noted that this use of parasitic capacitance to hold data during the very short transient condition is fundamentally different from the provision of capacitors in a known dynamic type of flip-flop circuit for achieving "memory". So as to simplify the figure, the parasitic capacitances C_1 and C_2 are shown only in the first (numerical referenced) part of Figure 3.

The remarks under "condition 3" above, apply equally, of course, to the case of a ring counter embodying the invention.

Attention is directed to our co-pending "divisional" application No. 14469/72 (Serial No. 1386293) the claims in which are directed to electronic timepieces. No claim is made in this specification to anything claimed in our said divisional application and the claims which follow are subject to the disclaimer.

Subject to the foregoing disclaimer,
WHAT WE CLAIM IS:—

1. A flip-flop circuit comprising first and second positive logic NAND circuits formed from a series connection of source-drain circuits of N-channel insulating gate field effect transistors; first and second negative logic NAND circuits formed from a series connection of source-drain circuits of P-channel insulating gate field effect transistors; and an inverter circuit formed from a pair of N-channel and P-channel field effect transistors, said first and second positive logic NAND circuits being connected in parallel in an AND configuration to define a positive

channel IGFET (12) belonging to the first negative logic NAND circuit.

In this way there is provided a circuit constituting a flip-flop circuit which "writes" the "write" input (21) or keeps the output (23) by synchronizing with the control input ϕ (or $\bar{\phi}$).

The foregoing is a simple description of the circuitry.

The circuit block indicated by reference 9 is constituted by using the flip-flop circuits as above described as a master flip-flop circuit and a slave flip-flop circuit as indicated by the references 24 and 25 respectively. By applying the output (23) of the master flip-flop circuit 24 as the input to the slave flip-flop circuit 25 and by arrang-

ing the control inputs ϕ and $\bar{\phi}$ of the slave flip-flop circuit 25 to be in phase opposition, there is obtained a master-slave type of delay flip-flop having two-stage operation.

By connecting n stages, each similar to the circuit block 9, in cascade and driving the circuit thus formed by a common clock signal ϕ ($\bar{\phi}$), an n -bit delay circuit is obtained. If the output is fed back to the input in the opposite phase, the circuit becomes a $2n$ divider. The arrangement actually shown in Figure 4 is a $1/4$ divider in which $n=2$.

The following brief description of the operation of a flip-flop circuit in accordance with the invention and as herein illustrated will assist in a better understanding of the said invention. The description which follows is given with respect to three different operating conditions, numbered respectively 1, 2 and 3.

Condition 1. "Write" state of data $\phi=0$
Transistors 12 and 17 are cut off and transistors 11 and 18 are conductive. Accordingly a signal applied from 21 is inverted by a series circuit comprising transistors 12, 14, 16 and 17 and appears at 22. This signal is inverted by an inverter comprising transistors 19 and 20 and appears at 23.

Condition 2. "Memory" state of data $\phi=1$
Transistors 11 and 18 are cut off and transistors 12 and 17 are conductive. Accordingly a signal appearing at 23 is inverted by a series circuit comprising transistors 12, 14, 16 and 17 and appears at 22. This signal is inverted by an inverter comprising transistors 19 and 20 and appears at 23. Because this signal is of the same polarity at that previously appearing at 23 it is held there and a "memory" state is established.

Condition 3. Transient state from $\phi=0$ to $\phi=1$

Theoretically and in principle, if an "ideal" signal wave form which can be changed instantaneously from $\phi=0$ to $\phi=1$ is assumed, the illustrated circuit can change over from the "write" state to the "memory" state without there being any parasitic capacity in the transistor gate circuit. In practice, however, the signal change from $\phi=0$ to $\phi=1$ is not instantaneous though it does not occupy more than a few microseconds and is accomplished in a limited time in an integrating circuit as usual. Capacitances C_1 and C_2 , as shown in broken lines in Figure 3, should accordingly be present so that data written in can be held during the transient state. These capacitances are shown in broken lines to indicate that they are not condensers but are necessarily present in the form of the parasitic capacitances of the transistor gates and of the wiring connected thereto, the parasitic capacitance values being, in any practical case, adequate to ensure the holding of data during the very short limited time in which the transient condition exists. It should be particularly noted that this use of parasitic capacitance to hold data during the very short transient condition is fundamentally different from the provision of capacitors in a known dynamic type of flip-flop circuit for achieving "memory". So as to simplify the figure, the parasitic capacitances C_1 and C_2 are shown only in the first (numerical referenced) part of Figure 3.

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Attention is directed to our co-pending "divisional" application No. 14469/72 (Serial No. 1386293) the claims in which are directed to electronic timepieces. No claim is made in this specification to anything claimed in our said divisional application and the claims which follow are subject to the disclaimer.

Subject to the foregoing disclaimer,
WHAT WE CLAIM IS:—

1. A flip-flop circuit comprising first and second positive logic NAND circuits formed from a series connection of source-drain circuits of N-channel insulating gate field effect transistors; first and second negative logic NAND circuits formed from a series connection of source-drain circuits of P-channel insulating gate field effect transistors; and an inverter circuit formed from a pair of N-channel and P-channel field effect transistors, said first and second positive logic NAND circuits being connected in parallel in an AND configuration to define a positive



logic circuit such that an output appears from this pair of NAND circuits only in the absence of a "1" signal at either gate of one series pair of transistors and a similar absence at either gate of the other series pair of transistors said first and second negative logic NAND circuits being connected in parallel in an AND configuration to define a negative logic circuit such that an output appears from this pair of NAND circuits only in the absence of a "1" signal at either gate of one series pair of transistors and a similar absence at either gate of the other series pair of transistors, said complementary positive and negative logic circuits thus formed being connected in series and disposed between the terminals of a source of potential, a connecting point terminal between said complementary positive and negative logic circuits generating a first output as well as connecting same to an input of said inverter circuit, an output of said inverter circuit generating a second output as well as connecting same to a gate of one transistor of each of said first positive and first negative logic NAND circuits, a write input being connected to a gate of one transistor of each of said second positive and second negative logic NAND circuits, a first control input being connected to a gate of one transistor of each of said first positive and second

negative logic NAND circuits which gate is not connected with said second output nor with said write input, a second control input in anti-phase with said first control input being connected to a gate of one transistor of each of said second positive and first negative logic NAND circuits which gate is not connected with said second output nor with said write input.

2. A flip-flop circuit substantially as herein described with reference to the accompanying drawings.

3. A ring counter comprising four flip-flop circuits each as claimed in claim 1 or 2.

4. A ring counter as claimed in claim 3 in which the output of the second of the four flip-flop circuits is fed back to the input of the first flip-flop circuit so as to form a divide-by-2 ring counter.

5. A ring counter comprising a plurality of flip-flop circuits each as claimed in claim 1 or 2 connected in cascade the output of the last flip-flop circuit being fed back to the input of the first flip-flop circuit so as to form a divide-by-2N ring counter.

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