Packaged Combination Memory For Electronic Devices

Background

This invention relates generally to memories or storage for electronic devices.

A wide variety of memory is available for a variety of specialized applications. For example, volatile memories, such as dynamic random access memory (DRAM) and static random access memory (SRAM), may be utilized for fast access to data. However, DRAM memory is difficult to integrate and SRAM memory is relatively high in cost.

Another type of memory is flash memory. However, flash memory is slower in write mode and has a limited number of write and erase cycles. Because it is non-volatile memory, flash memory may be applicable to both code and data storage applications.

In a wide variety of electronic devices, there is a need for relatively low cost memory that performs a variety of different functions. Examples of such devices include portable devices, such as cellular telephones, personal digital assistants (PDAs), notebook computers, wearable computers, in-car computing devices, web tablets, pagers, digital imaging devices, and wireless communication devices, to mention a few examples.

Currently, the storage on processor-based systems is largely handled by semiconductor memories, such as SRAMs and DRAMs, and by mechanical devices, such as optical and magnetic disk drives. Disk drives are relatively inexpensive but have relatively slower read and write access times. Semiconductor memories are more expensive, but have relatively fast access times. Thus, electronic devices using a combination of disk drive and semiconductor memories for storage may place the bulk of the data and code in the disk drive and store frequently used or cache data on semiconductor memories.

However, none of the existing technologies adequately provide the needed attributes for a truly portable device including lower cost, lower power consumption, non-volatile memory compactness and easy integration. Thus, there is a need for new types of memory.

One new memory type is the polymer memory. The polymer memory involves polymer chains with dipole moments. Data may be stored by changing the polarization of a polymer between conductive lines. For example, a polymeric film may be coated with a large number of conductive lines. A memory location at a cross-point of two lines is

selected when the two transverse lines are both charged. Because of this characteristic, polymer memories are one type of cross-point memory. Another cross-point memory being developed by Nantero, Inc. (Woburn, MA) uses crossed carbon nanotubules.

Cross-point memories are advantageous since no transistors are need to store each bit of data and the polymer layers can be stacked to a large number of layers, increasing the memory capacity. In addition, the polymer memories are non-volatile and have relatively fast read and write speeds. They also have relatively low costs per bit and lower power consumption. Thus, the polymer memory has a combination of low cost and high capacity that fits well in handheld data storage applications.

Phase-change materials may also be utilized to create memories. In phase-change memories, a phase-change material may be exposed to temperature to change the phase of the phase-change material. Each phase is characterized by a detectable electrical resistivity. To determine the phase of the memory during a read cycle, current may be passed through the phase-change material to detect its resistivity.

The phase-change memories are non-volatile and high density. They use relatively low power and are easy to integrate with logic. The phase-change memory may be suitable for many code and data storage applications. However, some high-speed volatile memory may still be needed for cache and other frequent write operations.

Thus, there is still a need for a memory solution for low cost, portable applications.

Brief Description of the Drawings

Figure 1 is a block diagram of one embodiment of the present invention;

Figure 2 is a schematic depiction of a package in accordance with one embodiment of the present invention;

Figure 3 is a schematic depiction of a package in accordance with another embodiment of the present invention;

Figure 4 is a schematic depiction of a package in accordance with still another embodiment of the present invention;

Figure 5 is a schematic depiction of a package in accordance with yet another embodiment of the present invention;

Figure 6 is a cross-sectional view of a package in accordance with one embodiment of the present invention; and

Figure 7 is a cross-sectional view of a package according to another embodiment of the present invention.

Detailed Description

Referring to Figure 1, a packaged integrated circuit device 10 may include a bus 12 that couples a plurality of memories of different memory types to a processor 14. By combining a plurality of different types of memory within the same package with a processor 14, a solution may be provided to the varying memory needs of a wide variety of portable device equipment manufacturers.

A cross-point memory 16 may be a polymer memory and may primarily be utilized for mass storage of data. A volatile memory 22 may be provided for cache and frequent write functions. A phase-change memory 18 may be utilized for both data and code storage needs and a non-volatile memory 20 may also be provided for code storage purposes.

The memories 16, 18, 20 and 22 may be integrated within the same integrated circuit package as separate dice in one embodiment of the present invention. In one embodiment of the present invention, the bus 12 may be integrated in the same die with the processor 14. Thus, each of the dice containing the memories 16, 18, 20 and 22 may be electrically coupled to a die including the processor 14 and the bus 12 in accordance with one embodiment of the present invention. For example, the dice containing the memories 16, 18, 20 and 22 may simply be stacked over a die containing the processor 14 and bus 12 and then the dice may be encapsulated within the same package 10.

By encapsulating the various memory types within a single package 10 with the processor 14, a solution may be provided to virtually any memory need of any portable device. Thus, portable device manufacturers may simply use the package 10 and may be assured that a complete solution is available for all their memory needs. This may improve the standardization of portable devices and, as a result, may reduce costs.

Referring to Figure 2, the package 10a may include a stack of four separate dice in accordance with one embodiment of the present invention. The lowermost die may include the processor 14. Moving upwardly, the next die above the processor 14 die may contain the non-volatile storage 20 and the next die above the non-volatile storage 20 die

may include the cross-point memory 16. The uppermost die may include a volatile memory 22. Each of the dice may be electrically coupled to one another.

Referring next to Figure 3, the processor 14, bus 12, and non-volatile memory 20 may be integrated into the same die in the package 10b. In such an embodiment, a stack may include the die for the processor 14 and non-volatile memories 14 and 20 at the bottom, followed by the dice for the cross-point memory 16 and volatile memory 22, if needed.

Referring to Figure 4, in still another embodiment, a package 10c may include a die integrating the processor 14, volatile memory 20 and non-volatile memory 22 and a separate die may include the cross-point memory 16 in accordance with one embodiment of the present invention. Of course, a wide variety of other integrated combinations of memory types may be included as well.

Referring to Figure 5, a package 10d may include a processor 14 and non-volatile memories 16 and 20, integrated into the same die. Another die may include the phase-change memory 18, still another die may include the cross-point memory 16 and yet another die may include the volatile memory 22. In various embodiments, one or more of the memory types may be omitted.

Finally, referring to Figure 6, a specific package architecture is illustrated for the package 10e in accordance with one embodiment of the present invention. In this case, a substrate 30 may provide electrical connections as well as the bus 12. A separate die 42 may be provided, for example, for the processor 14, and one or more of the other memories 16, 18, 20 or 22. Still another die 40 may contain another one of the memories 16, 18, 20 or 22 and a third die 38 in the stack may contain still another memory type, such as one of the memories 16, 18, 20 or 22.

Electrical connections 34 may be provided from each die 38, 40 or 42 to the substrate 30 to provide electrical connections between the processor 14 and the memories 16, 18, 20 and 22 (as well as the bus 12). Any type of electrical connection to the external world may be provided on the package 10e including solder balls 32, in accordance with one embodiment of the present invention.

Referring to Figure 7, still another embodiment of the present invention may use a folded stacked package 10f. In this case, the package 10f may be formed by providing the dice 54 connected by flexible foldable tape 50. The tape 50 may be divided into sections,

one section including the solder balls 32 and the die 52c, another section including the die 54a and still another section including the die 54b. The sections may be wing folded towards the center. As a result, surface mount interconnections 56 can be made between the various dice 54. Solder ball connections 58 may also be provided. Thus, in some embodiments, the dice 54 may include the processor 14, and one or more of the memories 16, 18, 20 or 22. Folded stacked packaging technology is available, from Tessera Technologies, Inc., San Jose, California, 95134.

In addition, the folded stacked packages may in turn be stacked to form a stack of folded stacked packages.

As still another alternative, a larger die such as a processor may have multiple stacks of other dice stacked on top of the processor. For example, a processor may have two sets of stacked dice on top of the processor die.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A packaged combination memory comprising:

an integrated non-volatile memory first circuit comprising a first memory type, said first circuit to mass store data;

an integrated volatile memory circuit to cache and make frequent writes;

an integrated non-volatile second circuit comprising a second memory type, said second circuit to store both data and code;

an integrated non-volatile third circuit comprising a third memory type, said third circuit to store code, said first, second, and third memory types all being different from one another;

a processor die coupled to said first, second, third, and non-volatile memory circuits to store information in a selected one of said circuits; and

a semiconductor integrated circuit package containing said first, second, third, and non-volatile memory circuits as well as said processor.

2. The memory of claim 1 wherein said first circuit is a polymer memory.

3. The memory of claim 1 wherein said volatile memory circuit is a dynamic random access memory.

4. The memory of claim 1 wherein said second circuit is a phase change memory circuit.

5. The memory of claim 1 wherein said third circuit is a flash memory circuit.

6. The memory of claim 1 including at least two integrated circuit memory die and said processor die within said integrated circuit package.

7. The memory of claim 1 wherein said package includes contacts and said processor is coupled most directly to said contacts.

8. The memory of claim 1 including a polymer memory, a dynamic random

access memory, a phase change memory, and a flash memory.

9. A method comprising:

packaging within one integrated circuit package a first circuit comprising a first memory type, said first circuit to mass store data, an integrated volatile memory circuit to cache and make frequent writes, an integrated circuit non-volatile second circuit comprising a second memory type, said second circuit to store both data and code, a third circuit to store code, said first, second, and third circuits all being non-volatile memories and being different from one another; and

forming within said same package, a processor die coupled to said first, second, and third non-volatile memories and said volatile memory such that said processor to store information in a selected one of said circuits.

10. The method of claim 9 including packaging in said package a polymer memory as said first memory type.

11. The method of claim 9 including packaging in said package a dynamic random access memory as said volatile memory circuit.

12. The method of claim 9 including packaging a phase change memory as said second memory type.

13. The method of claim 9 including packaging a flash memory as said third circuit.

14. The method of claim 9 including packaging at least two integrated circuit memory die with said processor die in said package.

15. The method of claim 14 including coupling said memory die to package contacts through said processor die.

16. The method of claim 9 including packaging a polymer phase change and flash memory in said package.