WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate that includes an active pattern;

a channel pattern disposed on the active pattern, wherein the channel pattern includes a plurality of semiconductor patterns that are vertically stacked and spaced apart from each other;

a source/drain pattern connected to the plurality of semiconductor patterns; and

a gate electrode disposed on the plurality of semiconductor patterns,

wherein the gate electrode includes a plurality of portions that are respectively interposed between the plurality of semiconductor patterns,

the source/drain pattern includes a buffer layer in contact with the plurality of semiconductor patterns and a main layer disposed on the buffer layer,

the buffer layer contains silicon germanium (SiGe) and includes a first semiconductor layer and a first reflow layer disposed on the first semiconductor layer, wherein the first semiconductor layer is a silicon germanium layer, and the first reflow layer is a silicon germanium layer having a germanium concentration that is less than a germanium concentration of the first semiconductor layer,

a side surface of the first semiconductor layer includes a protruding side surface that protrudes toward a first portion of the plurality of portions of the gate electrode, and a concave side surface in contact with a first semiconductor pattern of the plurality of semiconductor patterns, and

the first reflow layer includes a protruding portion that corresponds to the protruding side surface and a concave portion that corresponds to the concave side surface.

2. The semiconductor device of claim 1, wherein

the side surface of the first semiconductor layer has a wavy profile, and

the first reflow layer has a wavy shape that corresponds to the side surface of the first semiconductor layer.

3. The semiconductor device of claim 1 or claim 2, wherein a mean thickness of the first reflow layer is less than a mean thickness of the first semiconductor layer.

4. The semiconductor device of any one of claims 1 to 3, wherein

the germanium concentration of the first reflow layer ranges from 2 at% to 5 at%, and

the germanium concentration of the first semiconductor layer ranges from 4 at% to 8 at%.

5. The semiconductor device of any one of claims 1 to 4, wherein

a germanium concentration of the buffer layer ranges from 2 at% to 8 at%, and

a germanium concentration of the main layer ranges from 30 at% to 70 at%.

6. The semiconductor device of any one of claims 1 to 5, wherein a thickness of the first reflow layer adjacent to the first semiconductor layer is less than a thickness of the first reflow layer adjacent to a bottom of the source/drain pattern.

7. The semiconductor device of any one of claims 1 to 5, wherein

the first reflow layer includes a filler portion that is configured to fill a hole in the first semiconductor layer.

8. The semiconductor device of any one of claims 1 to 7, wherein

the buffer layer further comprises a second semiconductor layer disposed on the first reflow layer and a second reflow layer interposed between the second semiconductor layer and the main layer,

the second semiconductor layer is a silicon germanium layer, and

the second reflow layer is a silicon germanium layer having a germanium concentration that is less than a germanium concentration of the second semiconductor layer.

9. The semiconductor device of claim 8, wherein

the germanium concentration of the second reflow layer is greater than the germanium concentration of the first reflow layer, and

the germanium concentration of the second semiconductor layer is greater than the germanium concentration of the first semiconductor layer.

10. The semiconductor device of any one of claims 1 to 9, wherein the first reflow layer has a super lattice structure that includes germanium.

11. A semiconductor device, comprising:

a substrate that includes an active pattern;

a pair of channel patterns disposed on the active pattern;

a source/drain pattern interposed between the pair of channel patterns;

a pair of gate electrodes disposed on the pair of channel patterns, respectively; and

a gate spacer disposed on a side surface of each of the pair of gate electrodes,

wherein, when viewed in a plan view, the source/drain pattern comprises:

a buffer layer interposed between a first end and a second end of the gate spacer; and

a main layer disposed on the buffer layer,

wherein the buffer layer includes a semiconductor layer and at least one reflow layer disposed on the semiconductor layer, the semiconductor layer is a silicon germanium layer, and the reflow layer is a silicon germanium layer having a germanium concentration that is less than a germanium concentration of the semiconductor layer,

an edge portion of the buffer layer has a first thickness,

a center portion of the buffer layer has a second thickness greater than the first thickness, and

a ratio of the first thickness to the second thickness ranges from 0.2 to 0.8.

12. The semiconductor device of claim 11, wherein

the buffer layer contains silicon germanium (SiGe) and the semiconductor layer is in direct contact with the pair of channel patterns, and

a thickness of the at least one reflow layer is less than a thickness of the semiconductor layer.

13. The semiconductor device of claim 12, wherein

the germanium concentration of the reflow layer ranges from 2 at% to 5 at%, and

the germanium concentration of the semiconductor layer ranges from 4 at% to 8 at%.

14. The semiconductor device of any one of claims 11 to 13, wherein the edge portion of the buffer layer is in contact with the first or second end of the gate spacer.

15. The semiconductor device of any one of claims 11 to 14, wherein

a germanium concentration of the buffer layer ranges from 2 at% to 8 at%, and

a germanium concentration of the main layer ranges from 30 at% to 70 at%.

16. A semiconductor device, comprising:

a substrate that includes a PMOSFET region and an NMOSFET region that are spaced apart from each other;

a first active pattern disposed on the PMOSFET region and a second active pattern disposed on the NMOSFET region;

a first channel pattern and a first source/drain pattern disposed on the first active pattern;

a second channel pattern and a second source/drain pattern disposed on the second active pattern;

a gate electrode disposed on the first and second channel patterns;

a gate insulating layer interposed between the gate electrode and the first and second channel patterns;

a gate spacer disposed on a side surface of the gate electrode;

a gate capping pattern disposed on a top surface of the gate electrode;

a gate cutting pattern that penetrates the gate electrode;

an interlayer insulating layer disposed on the gate capping pattern and the gate cutting pattern;

first and second active contacts that penetrate the interlayer insulating layer and are electrically connected to the first and second source/drain patterns, respectively;

metal-semiconductor compound layers respectively interposed between the first and second active contacts and the first and second source/drain patterns;

a gate contact that penetrates the interlayer insulating layer and the gate capping pattern and is electrically connected to the gate electrode;

a first metal layer disposed on the interlayer insulating layer, wherein the first metal layer includes a power line that vertically overlaps the gate cutting pattern, and first interconnection lines that are electrically and connected to the first and second active contacts and the gate contact, respectively; and

a second metal layer disposed on the first metal layer,

wherein the second metal layer includes second interconnection lines electrically connected to the first metal layer,

the first channel pattern includes a plurality of semiconductor patterns that are vertically stacked and are spaced apart from each other,

the first source/drain pattern includes a buffer layer in contact with the plurality of semiconductor patterns and a main layer disposed on the buffer layer, and

the buffer layer comprises a first semiconductor layer and a first reflow layer disposed on the first semiconductor layer, wherein the first semiconductor layer is a silicon germanium layer, and the first reflow layer is a silicon germanium layer having a germanium concentration that is less than a germanium concentration of the first semiconductor layer.

17. The semiconductor device of claim 16, wherein

the gate electrode comprises a plurality of portions, which are respectively provided between the plurality of semiconductor patterns,

a side surface of the first semiconductor layer comprises a protruding side surface, which protrudes toward a first portion of the plurality of portions of the gate electrode, and a concave side surface, which is in contact with a first semiconductor pattern of the plurality of semiconductor patterns, and

the first reflow layer comprises a protruding portion corresponding to the protruding side surface and a concave portion corresponding to the concave side surface.

18. The semiconductor device of claim 16 or claim 17, wherein

the buffer layer contains silicon germanium (SiGe).

19. The semiconductor device of any one of claims 16 to 18, wherein

the buffer layer further comprises a second semiconductor layer disposed on the first reflow layer and a second reflow layer interposed between the second semiconductor layer and the main layer,

the second semiconductor layer is a silicon germanium layer, and

the second reflow layer is a silicon germanium layer having a germanium concentration that is less than a germanium concentration of the second semiconductor layer.

20. The semiconductor device of any one of claims 16 to 19, wherein a mean thickness of the first reflow layer is less than a mean thickness of the first semiconductor layer.