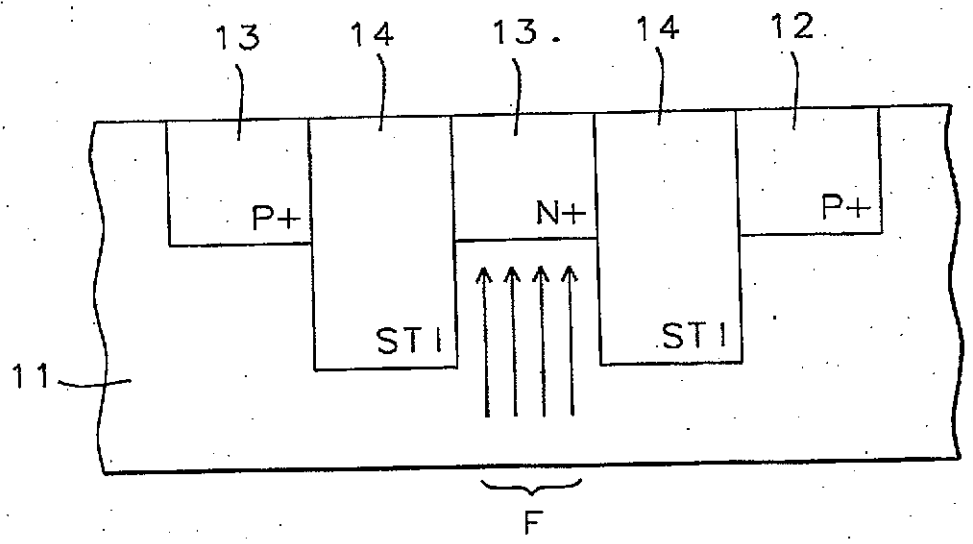


FIG. 1

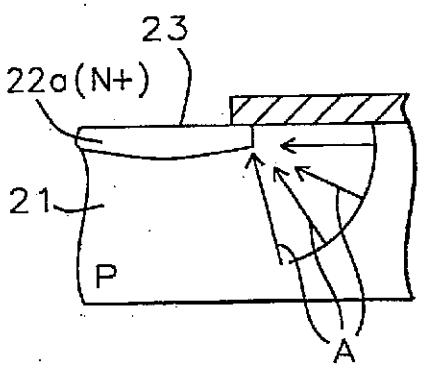


FIG. 2a

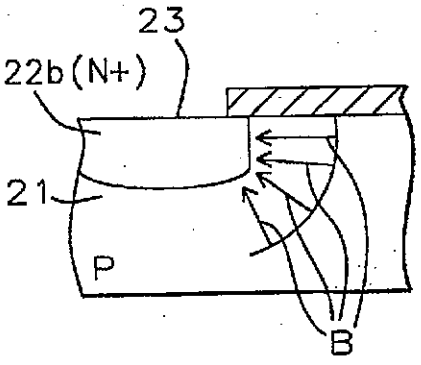


FIG. 2b

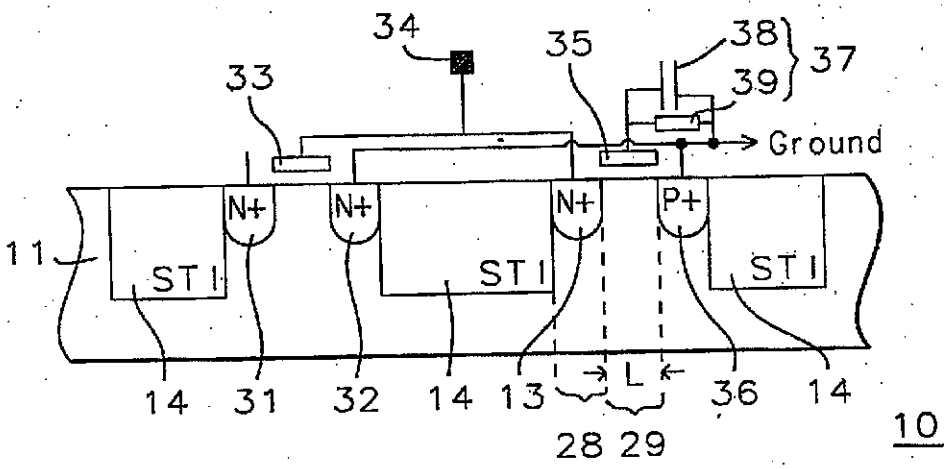


FIG. 3a

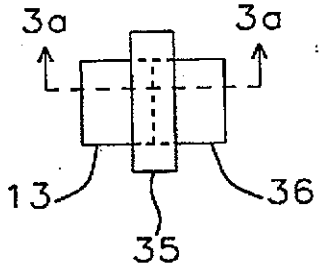


FIG. 3b

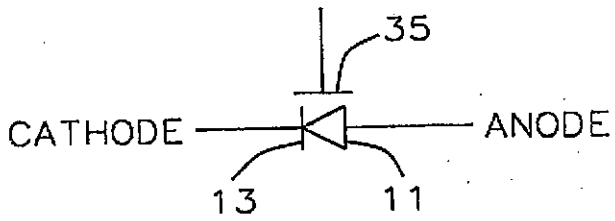


FIG. 4

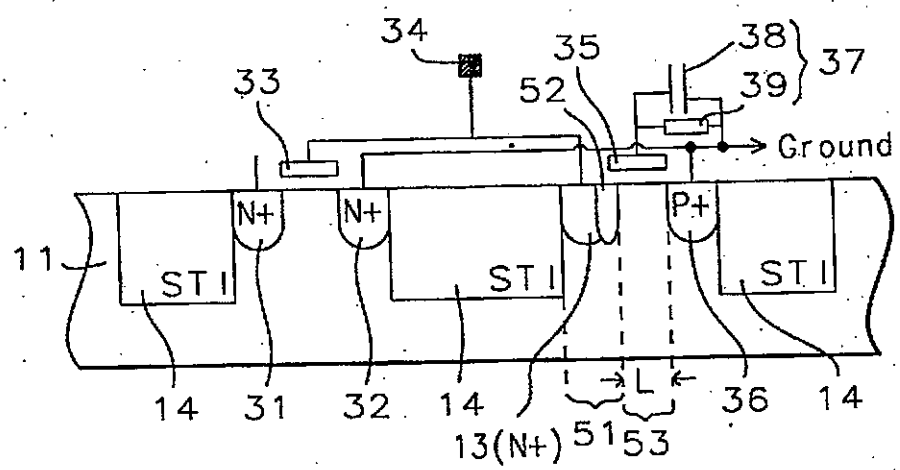


FIG. 5a

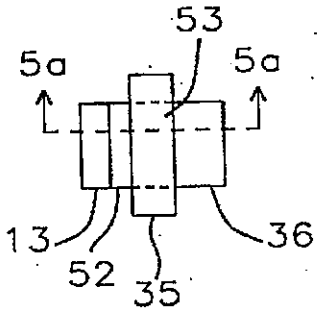


FIG. 5b

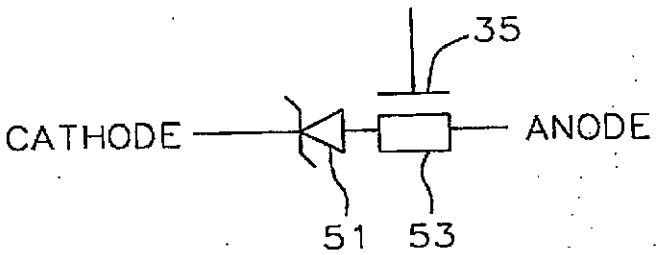


FIG. 6

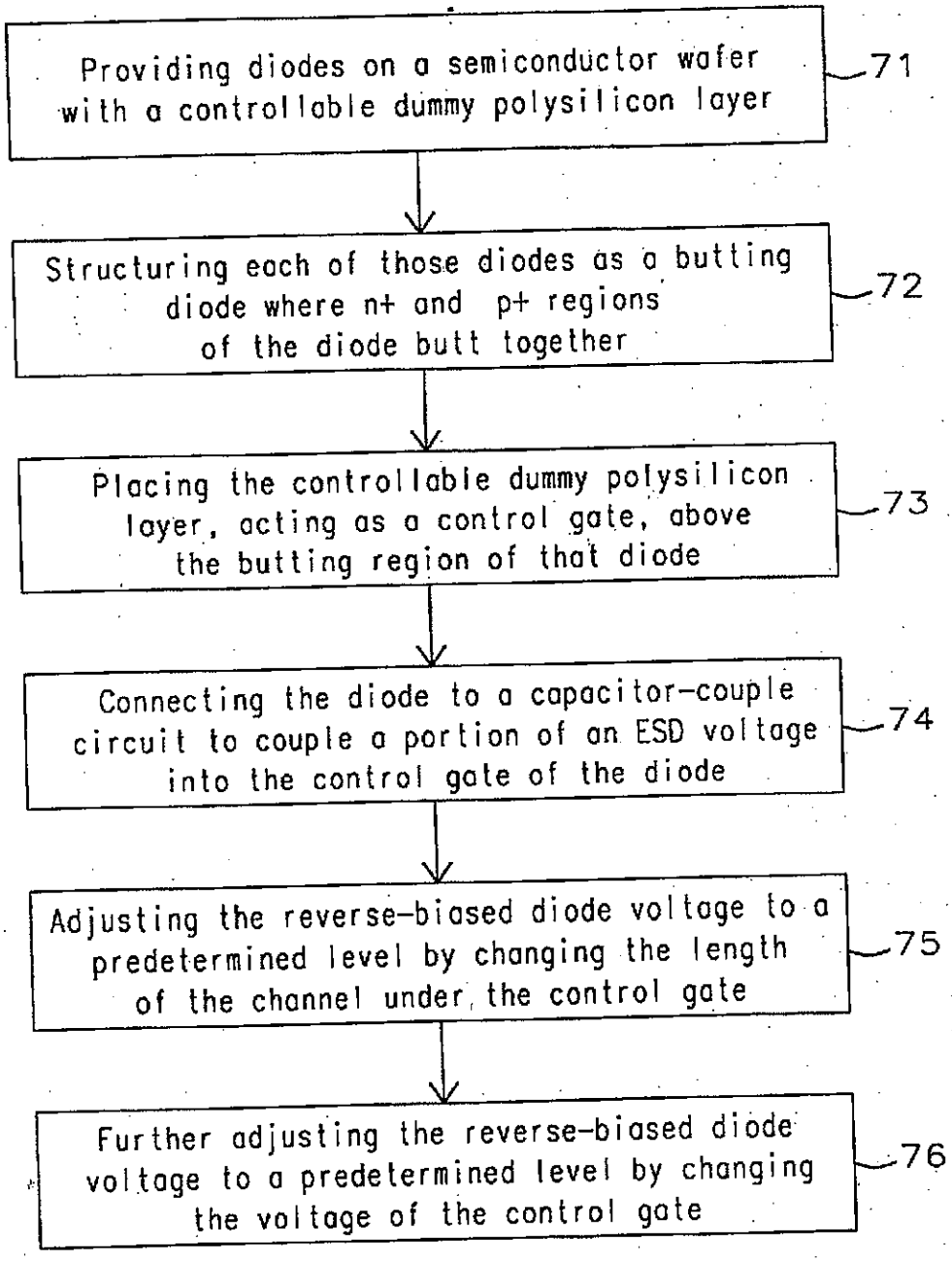

Providing diodes on a semiconductor wafer with a controllable dummy polysilicon layer
71
Structuring each of those diodes as a butting diode where n+ and p+ regions of the diode butt together
72
Placing the controllable dummy polysilicon layer, acting as a control gate, above the butting region of that diode
73
Connecting the diode to a capacitor-couple circuit to couple a portion of an ESD voltage into the control gate of the diode
74
Adjusting the reverse-biased diode voltage to a predetermined level by changing the length of the channel under the control gate
75
Further adjusting the reverse-biased diode voltage to a predetermined level by changing the voltage of the control gate
76

FIG. 7