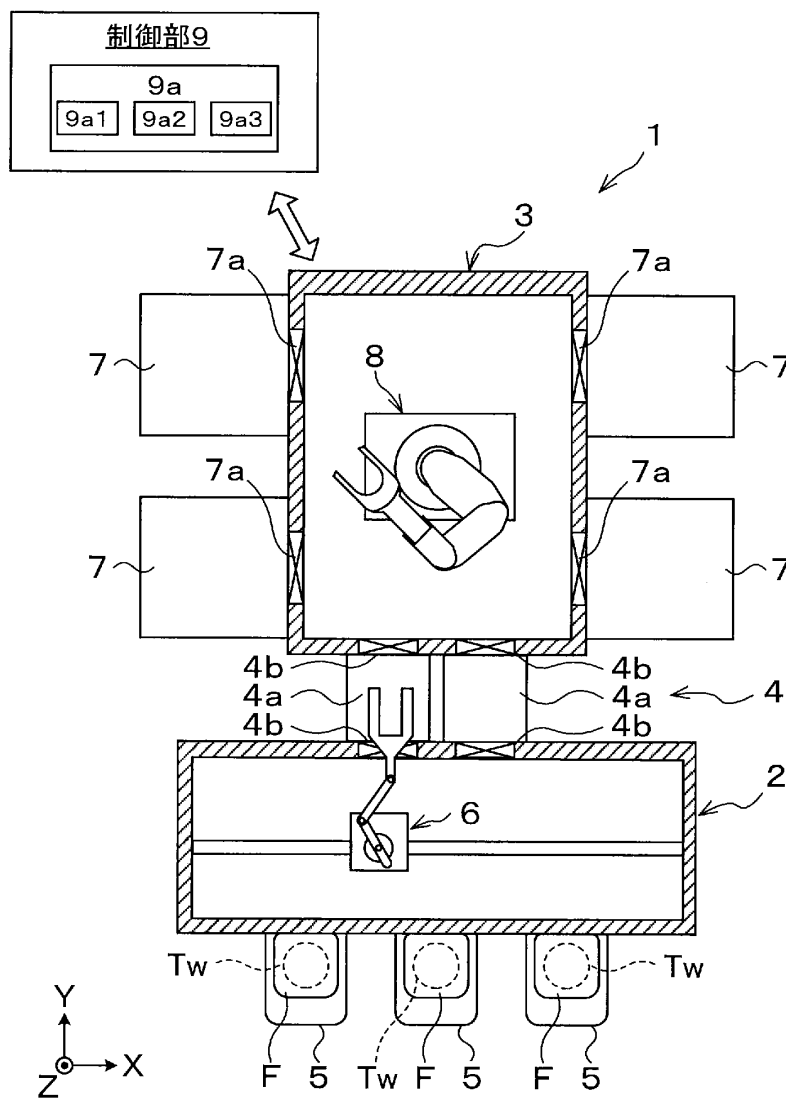
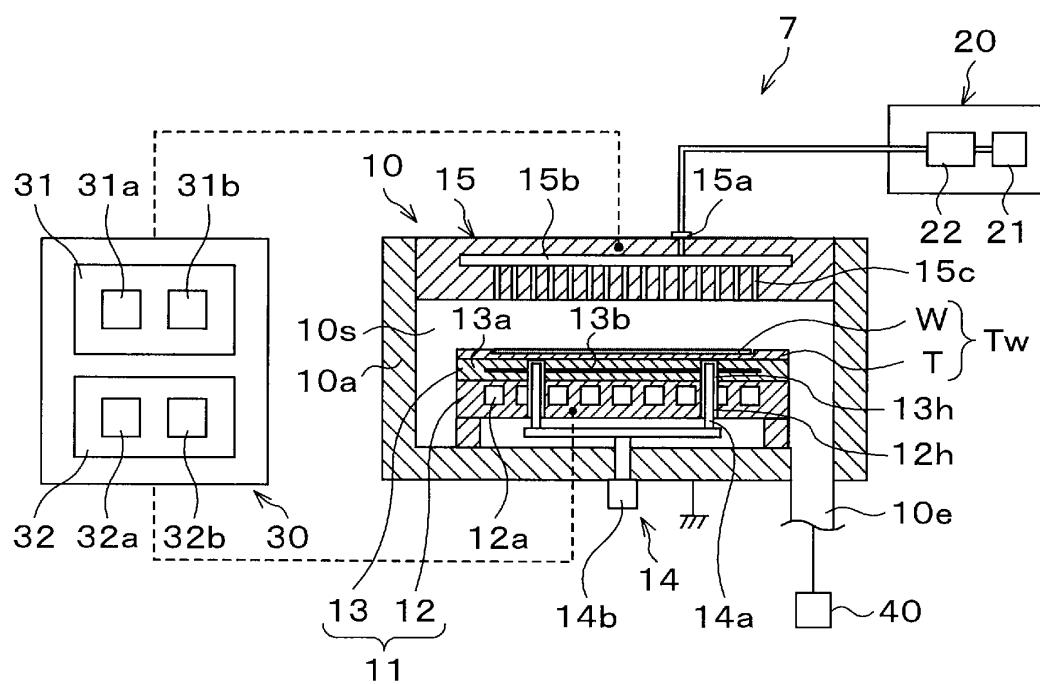


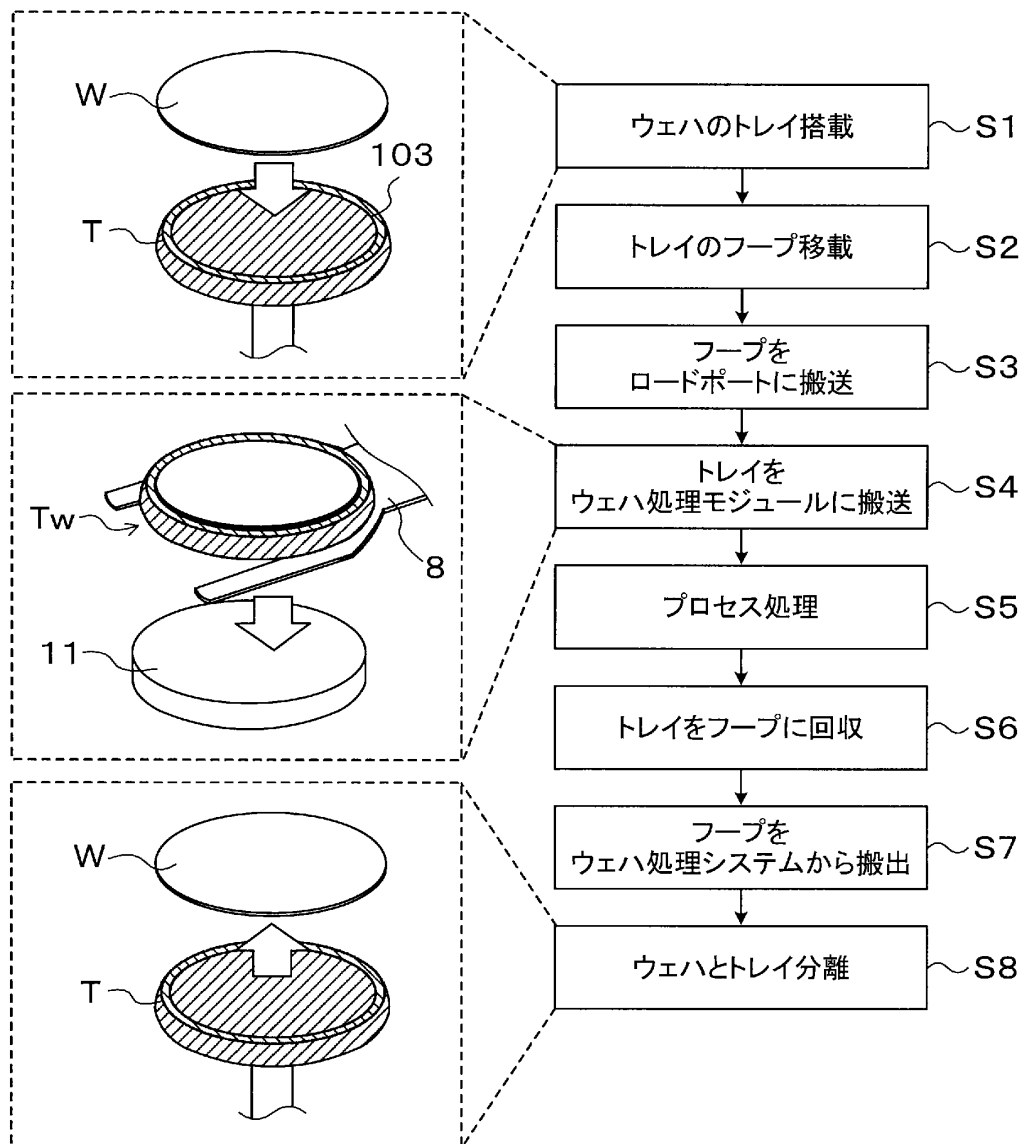
[図1]



[図2]

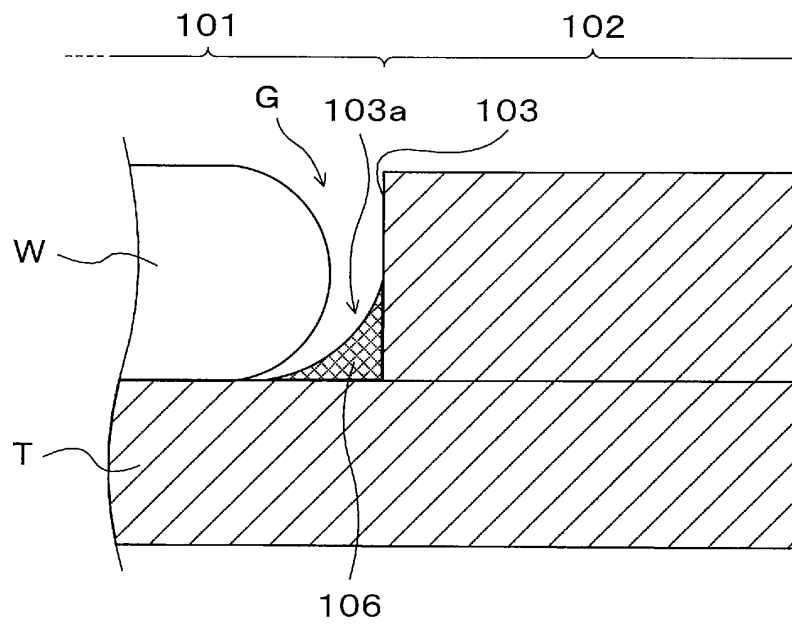


[図3]

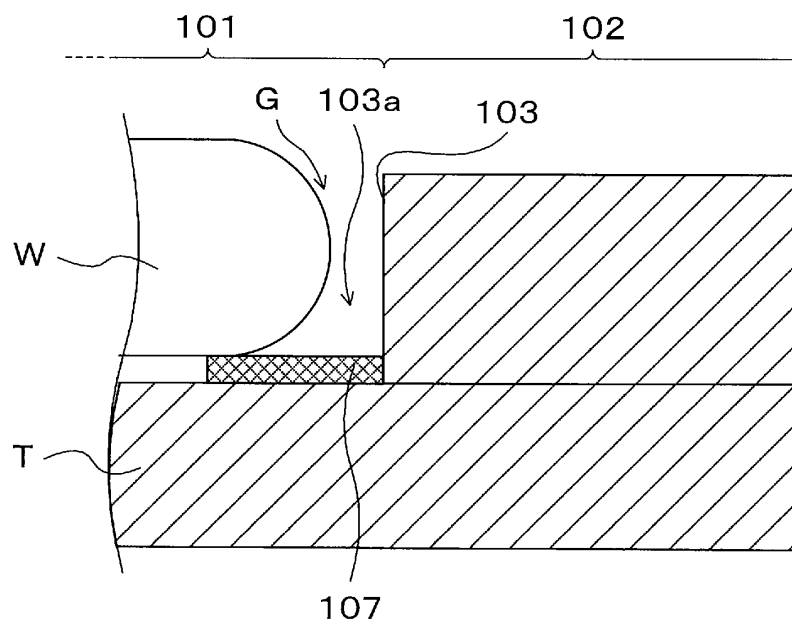




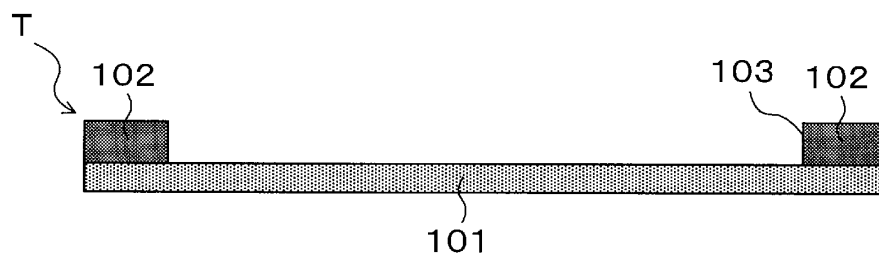
[図5]



[図6]



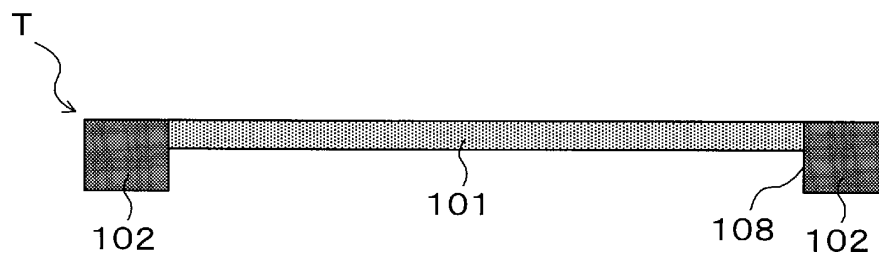
[図7]



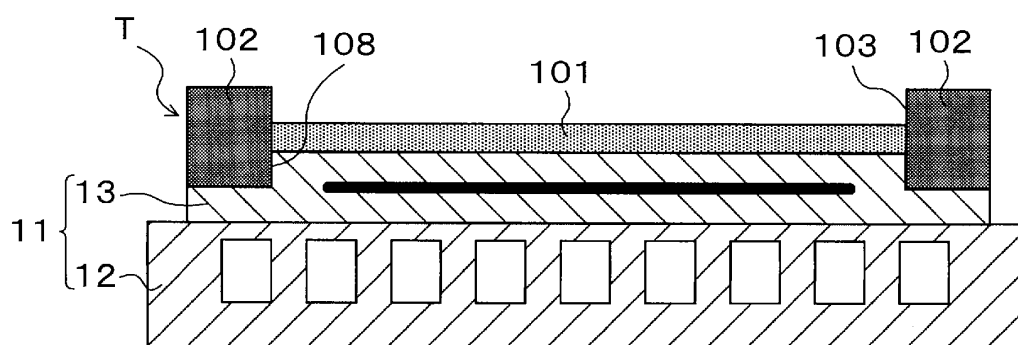
[図8]



[図9]

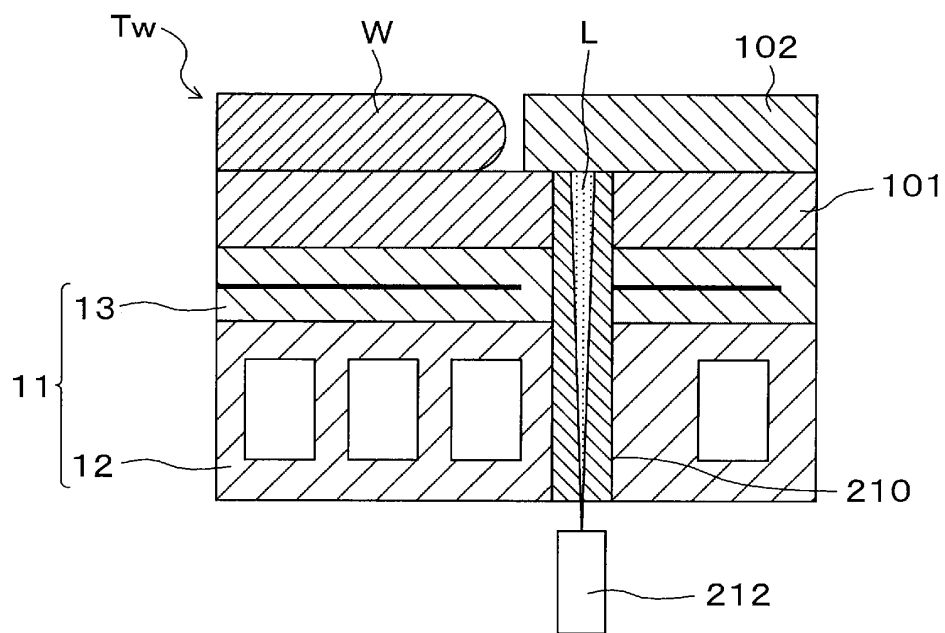


[図10]



[illegible]

[図14]



[図15]

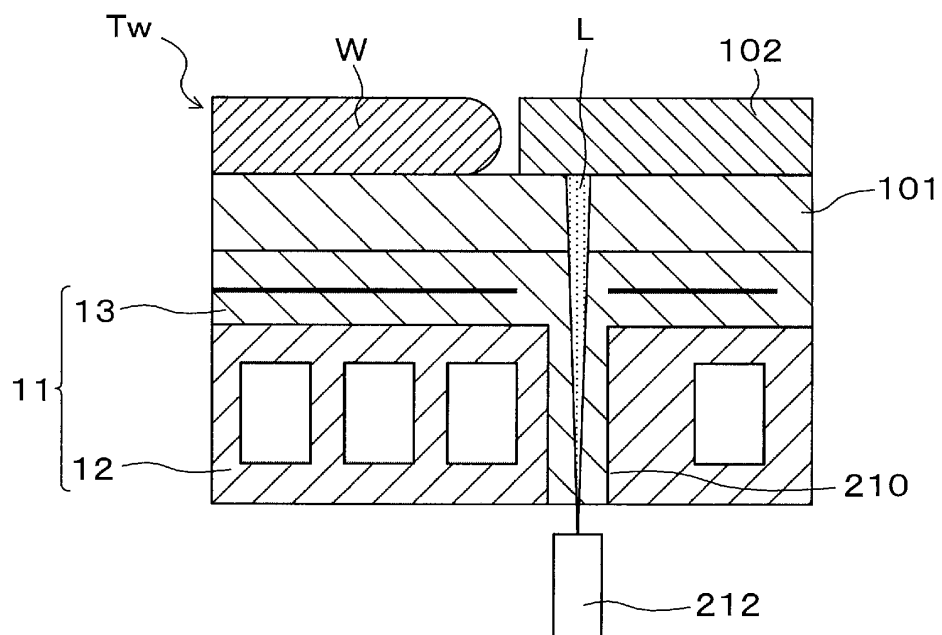
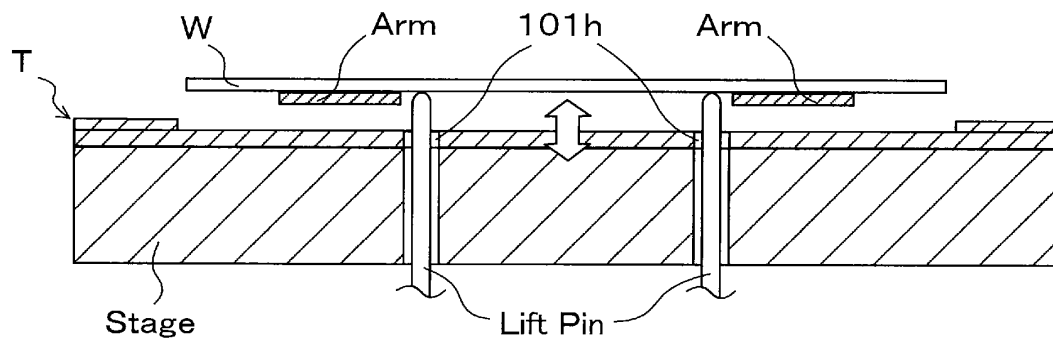


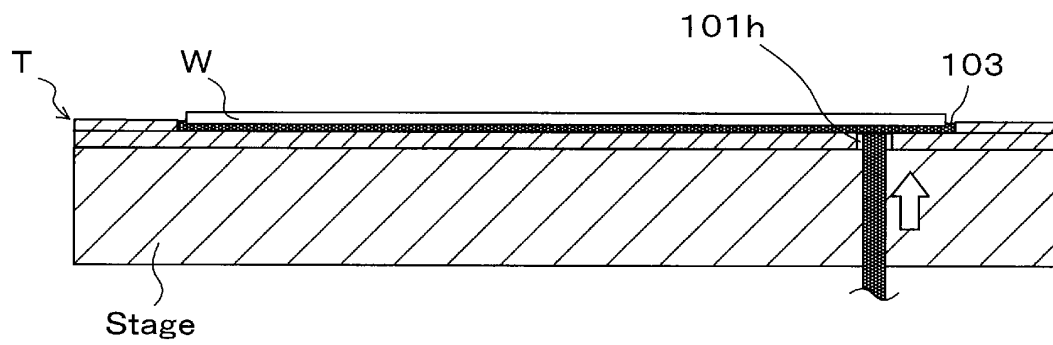
Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 101. A top layer 102 is formed on the substrate 101. A trench 202 is formed in the substrate 101, with a bottom layer 202a and a side layer 202b. A gate stack 11 is formed on the top layer 102, with a gate dielectric 13 and a gate electrode 12. A contact plug 32 is formed in the trench 202, connecting the gate electrode 12 to a ground symbol.

Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 101. A top layer 102 is formed on the substrate. A central vertical structure 202a (202) is formed, with a bottom layer 202b (202) on the substrate. A layer 8 is on the left side. A layer 11 is on the right side, containing regions 12 and 13. A layer 32 is at the bottom, connected to a voltage source symbol.

[図18]

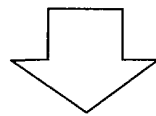
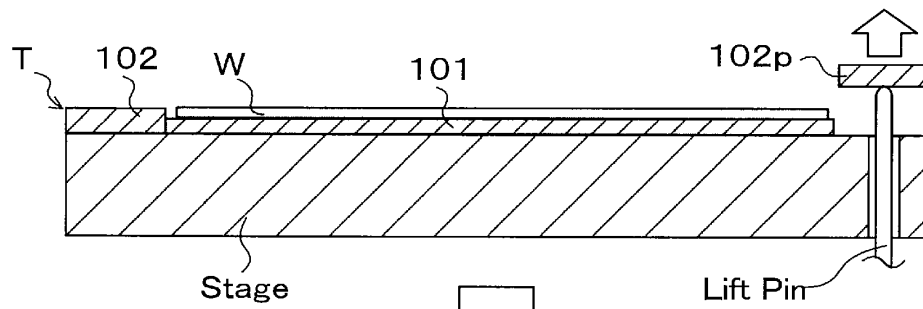


[図19]



[図20]

(a)



(b)

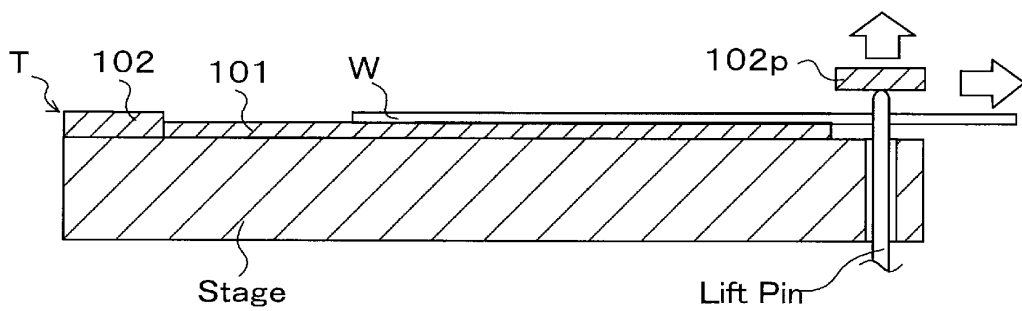
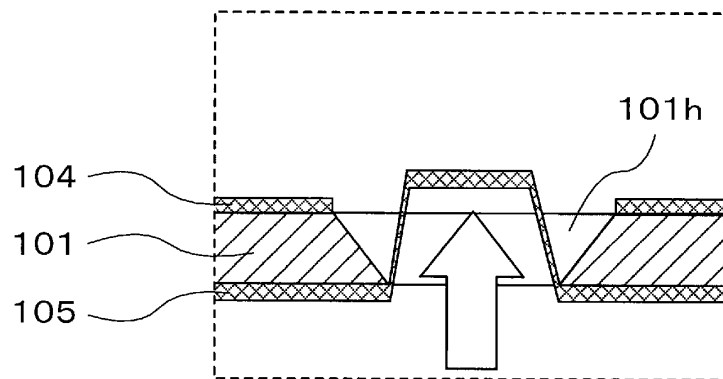


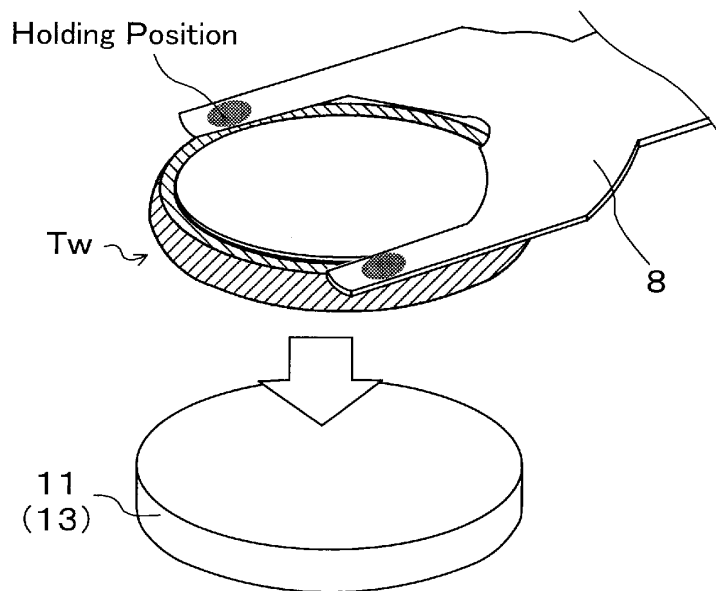
Fig. 10 is a cross-sectional view of a semiconductor device. It shows a central protrusion on a substrate (105). The protrusion has a trapezoidal top layer (101p) and a trapezoidal bottom layer (101h) separated by a thin layer (104). The device is on a substrate (105) with a central opening.

Fig. 10 is a cross-sectional view of a semiconductor device. The device includes a central channel region 101, a gate stack 104, and a top layer 105. A dashed box 101p highlights a portion of the device, and a label 101h points to the channel region.

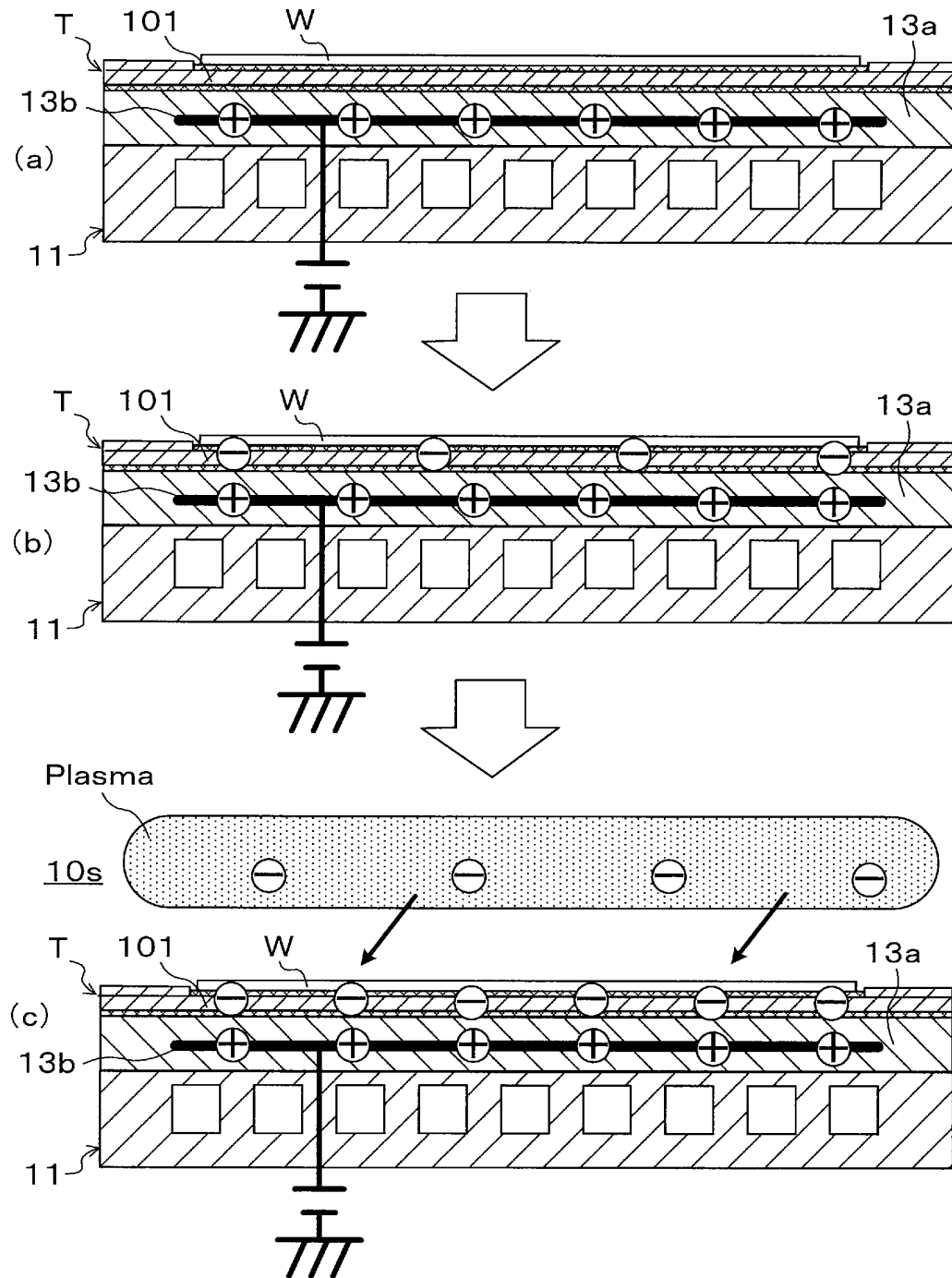
[図24]



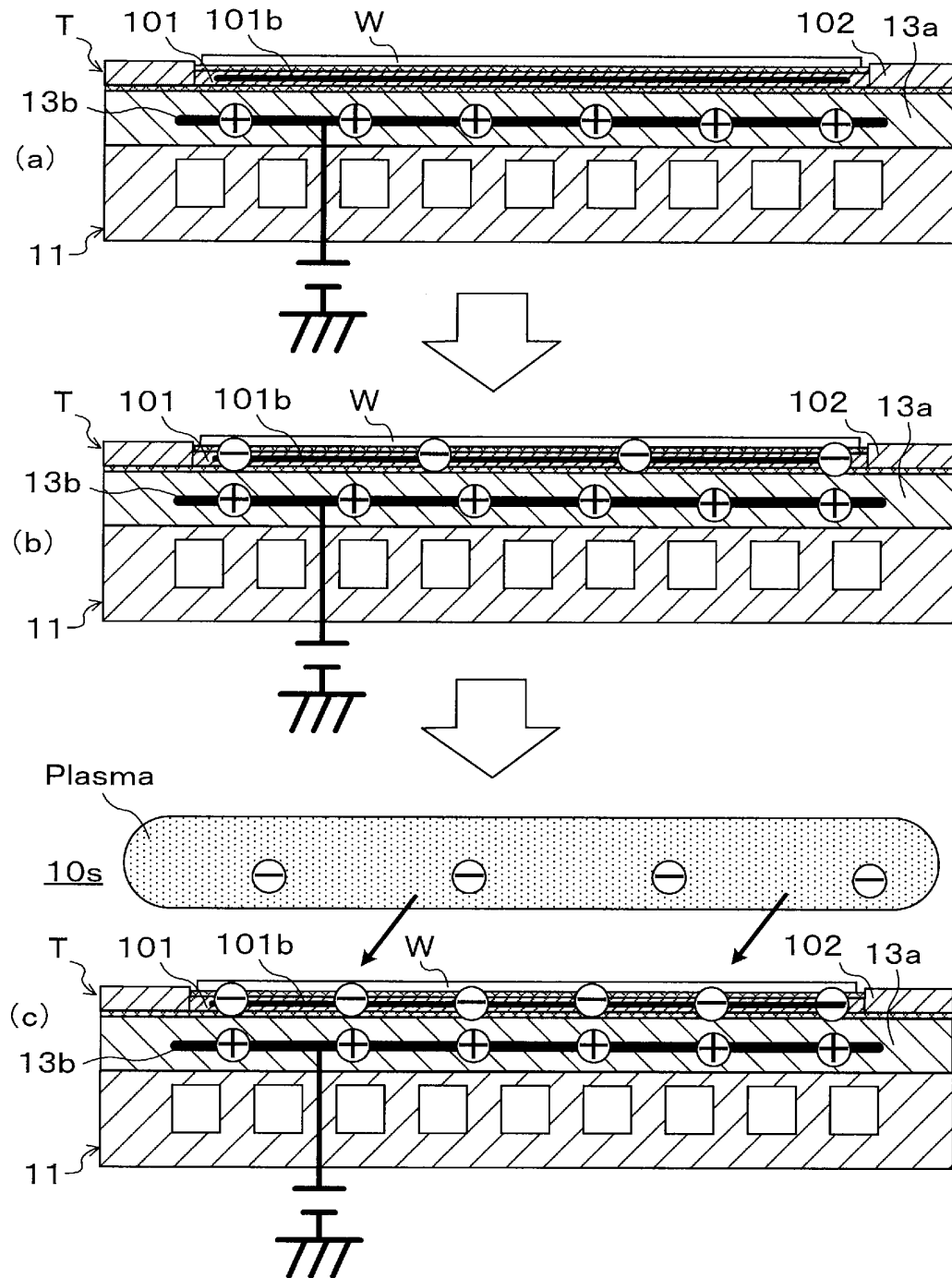
[図25]



[図26]

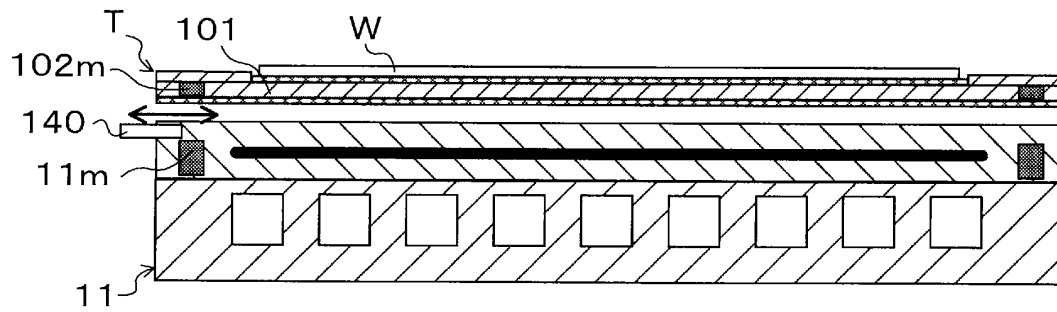


[図27]





[図30]



[図31]

