NOVEL DRAM ACCESS TRANSISTOR

FIELD OF THE INVENTION

[0001] The present invention relates to dynamic random access memory (DRAM) cells and, in particular, to a novel process for their formation.

BACKGROUND OF THE INVENTION

[0002] A dynamic random access memory cell typically comprises a charge storage capacitor (or cell capacitor) coupled to an access device, such as a Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). The MOSFET functions to apply or remove charge on the capacitor, thus affecting a logical state defined by the stored charge. The amount of charge stored on the capacitor is determined by the electrode (or storage node) area and the interelectrode spacing. The conditions of DRAM operation such as operating voltage, leakage rate and refresh rate, will generally mandate that a certain minimum charge be stored by the capacitor.

[0003] In the continuing trend to higher memory capacity, the packing of storage cells must increase, yet each will maintain required capacitance levels. This is a crucial demand of DRAM fabrication technologies if future generations of expanded memory array devices are to be successfully manufactured. Recently, attempts to increase the packing density of cell capacitors and/or to simultaneously reduce the transistor size have been made but with limited results. For example, one approach is reducing the length of a transistor gate electrode formed atop a

substrate and a source/drain region, to increase therefore the integration density. Unfortunately, reduction of the threshold voltage and/or the so-called short channel effect such as the punch-through phenomenon are likely to appear. A well-known scaling method is effective to improve the above-mentioned disadvantages. However, this approach increases of the substrate density and requires reduction of the supply voltage, which in turn leads to reduction of the margin concerning the electric noise and fluctuations in the threshold voltage.

[0004] Accordingly, there is a need for an improved method of forming MOS semiconductor devices, which permits achieving an increased integration of semiconductor circuitry as well as preventing the occurrence of the short-channel effect.

SUMMARY OF THE INVENTION

[0005] The present invention provides a method of forming memory devices, such as DRAM access transistors, having recessed gate structures. Field oxide areas for isolation are first formed over a semiconductor substrate subsequent to which transistor grooves are patterned and etched in a silicon nitride layer. The field oxide areas adjacent to the transistor grooves are then recessed, so that subsequently deposited polysilicon for gate structure formation can be polished relative to adjacent and elevated silicon nitride structures.

[0006] These and other advantages and features of the present invention will be more apparent from the detailed description and the accompanying drawings, which illustrate exemplary embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figure 1 illustrates a three dimensional view of a portion of a semiconductor device on which a DRAM access transistor will be formed according to a method of the present invention.

[0008] Figure 2 illustrates a three dimensional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 1.

[0009] Figure 3 illustrates a three dimensional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 2.

[0010] Figure 4 illustrates a three dimensional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 3.

[0011] Figure 5 illustrates a three dimensional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 4.

[0012] Figure 6 illustrates a three dimensional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 5.

[0013] Figure 7 illustrates a three dimensional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 6.

[0014] Figure 8 illustrates a cross-sectional view of the Figure 7 device taken along line 8-8′.

[0015] Figure 9 illustrates a cross-sectional view of the Figure 7 device taken along line 9-9′.

[0016] Figure 10 illustrates a cross-sectional view of the Figure 7 device taken along line 10-10′

[0017] Figure 11 illustrates a cross-sectional view of the Figure 10 device at a stage of processing subsequent to that shown in Figure 10.

[0018] Figure 12 illustrates a cross-sectional view of the Figure 10 device at a stage of processing subsequent to that shown in Figure 11.

[0019] Figure 13 illustrates a cross-sectional view of the Figure 10 device at a stage of processing subsequent to that shown in Figure 12.

[0020] Figure 14 illustrates a cross-sectional view of the Figure 7 device taken along line 14-14′ and at a stage of processing subsequent to that shown in Figure 12.

[0021] Figure 15 illustrates a cross-sectional view of the Figure 7 device taken along line 15-15′ and at a stage of processing subsequent to that shown in Figure 12.

[0022] Figure 16 illustrates a cross-sectional view of the Figure 10 device at a stage of processing subsequent to that shown in Figure 13.

[0023] Figure 17 illustrates a cross-sectional view of the Figure 10 device at a stage of processing subsequent to that shown in Figure 16 and in accordance with a first embodiment of the invention.

[0024] Figure 18 illustrates a cross-sectional view of the Figure 10 device at a stage of processing subsequent to that shown in Figure 16 and in accordance with a second embodiment of the invention.

[0025] Figure 19 illustrates a cross-sectional view of the Figure 18 device at a stage of processing subsequent to that shown in Figure 18.

[0026] Figure 20 illustrates a cross-sectional view of the Figure 18 device at a stage of processing subsequent to that shown in Figure 19.

[0027] Figure 21 illustrates a cross-sectional view of the Figure 18 device at a stage of processing subsequent to that shown in Figure 20.

[0028] Figure 22 illustrates a cross-sectional view of the Figure 18 device at a stage of processing subsequent to that shown in Figure 21.

[0029] Figure 23 is an illustration of a computer system having a DRAM access transistor be formed according to a method of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0030] In the following detailed description, reference is made to various specific exemplary embodiments in which the invention may be practiced. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be employed, and that structural, logical, and electrical changes may be made.

[0031] The terms "wafer" or "substrate" used in the following description may include any semiconductor-based structure that has an exposed semiconductor surface. Wafer and structure must be understood to include silicon-on insulator (SOI), silicon-on sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. The semiconductor need not be silicon-based. The semiconductor could be silicon-germanium, germanium, or gallium arsenide.

[0032] Referring now to the drawings, where like elements are designated by like reference numerals, Figures 1-22 illustrate a method of forming a DRAM memory device 100 (Figure 22) having access transistors formed according to exemplary embodiments of the present invention. Figure 1 illustrates a semiconductor substrate 10 over which a thin thermally grown oxide layer 12, with a thickness of about 50 Angstroms to about 200 Angstroms, has been formed according to conventional semiconductor processing techniques. An insulating layer 14 such as silicon nitride (Si_3N_4) layer 14 (Figure 1) of about 100 Angstroms

to about 1,000 Angstroms is next disposed over the substrate 10 and the oxide layer 12. The silicon nitride layer 14 may be formed by known deposition processes such as sputtering by chemical vapor deposition (CVD) or low temperature deposition by electron cyclotron resonance plasma enhanced CVD, among others. Although reference to the insulating layer 14 will be made as to the silicon nitride layer 14, it must be understood that the insulating layer 14 may be also formed of silicon oxide, for example, or other insulating materials, and thus the invention is not limited to the use of silicon nitride.

[0033] Next, the silicon nitride layer 14 is patterned using a photoresist layer 15 (Figure 2) formed over the silicon nitride layer 14 to a thickness of about 1,000 Angstroms to about 10,000 Angstroms. The photoresist layer 15 is patterned with a mask (not shown) and the silicon nitride layer 14 is anisotropically etched through the patterned photoresist to obtain a plurality of silicon nitride columns 18 having a width W of about 1,000 Angstroms to about 2,000 Angstroms and shallow trenches for isolation (STI) 20, as shown in Figure 3. To obtain the shallow trenches for isolation 20, the silicon nitride layer 14, the oxide layer 12 and the substrate 10 are all etched to a depth of about 1,000 Angstroms to about 10,000 Angstroms, preferably of about 5,000 Angstroms. Subsequent to the formation of the shallow trenches for isolation 20, the photoresist layer 15 is removed by conventional techniques, such as oxygen plasma, for example, or by flooding the substrate 10 with UV irradiation to degrade the photoresist and obtain the structure of Figure 4.

[0034] Subsequent to the formation of the shallow trenches for isolation 20 (Figures 3-4), the trenches are filled with an isolation dielectric 21, illustrated in Figure 5. Any dielectric suitable for isolation may be employed to fill trenches 20. In an exemplary embodiment, trenches 20 are filled with high density plasma (HDP) oxide, a material which has a high ability to effectively fill narrow trenches. Alternatively, an insulating layer (not shown) formed of an oxide or of silicon

nitride, for example, may be formed on the trench sidewalls, prior to filling the trenches 20 with the isolation dielectric 21, to aid in smoothing out the corners in the bottom of the trenches and to reduce the amount of stress in the dielectric used to later fill in the trenches.

[0035] Reference is now made to Figure 6. The silicon nitride columns 18 are patterned and etched to form regions A adjacent to the isolation dielectric 21 and transistor grooves 22. The silicon nitride layer 14, the oxide layer 12 and the substrate 10 are all etched, by reactive ion etching, for example, to a depth of about 1,000 Angstroms to about 10,000 Angstroms to obtain the transistor grooves 22 where gate structures of the DRAM memory device 100 (Figure 22) will be later formed as it will be described in detail below. To form the transistor grooves 22, substrate 10 is etched to a depth λ (Figure 6) of about 500 Angstroms to about 5,000 Angstroms.

[0036] Subsequent to the formation of the transistor grooves 22 (Figure 6) and regions A (Figure 6), the isolation dielectric 21 is partially etched with a selective etchant to obtain recessed structures 24 adjacent to isolation regions B, as shown in Figure 7. The isolation dielectric 21 is etched to a depth δ (Figure 7) of about 500 Angstroms to about 3,000 Angstroms, by a directional etching process such as plasma etching, for example. As it will be explained below, the isolation dielectric 21 is recessed to allow a subsequently deposited polysilicon to be chemical mechanically polished relative to the remaining silicon nitride from the silicon nitride layer 14. Cross-sectional views of the recessed structures 24 (Figure 7) and the isolation regions B (Figure 7) in relation to the transistor grooves 22 are illustrated in Figures 8 and 9 for a better understanding of the invention.

[0037] Reference is now made to Figure 10, which is a cross-sectional view of the structure of Figure 7 taken along line 10-10′ and illustrating the regions A and the transistor grooves 22. At this point, processing steps for transistor gate structure formation proceed according to conventional semiconductor processing

techniques. As such, a thin gate oxide layer 29 is first formed on the sidewalls and bottoms of the transistor grooves 22, as shown in Figure 11. The thin gate oxide layer 29 may be thermally grown in an oxygen ambient, at a temperature between about 600°C to about 1,000°C and to a thickness of about 30 Angstroms to about 100 Angstroms.

[0038] A polysilicon layer 30 (Figure 12) is then formed over both regions A, B as well as inside the transistor grooves 22 and the recessed structures 24 of the substrate 10. The polysilicon layer 30 may be deposited over the thin gate oxide layer 29 via LPCVD procedures, at a temperature of about 300°C to about 700°C. After its deposition, polysilicon layer 30 is planarized down to or near the planar surface of the silicon nitride layer 14 of the regions A, to form polysilicon gate layers 32, as shown in Figure 13. Chemical mechanical polishing (CMP) may be used for planarizing, but other suitable methods could be used also, as desired. For a better understanding on how the CMP of the polysilicon stops on the nitride layer 14, reference is made to Figures 14-15, which are cross sectional views of the structure of Figure 7, taken along lines 14-14′ and 15-15′ respectively, but after the deposition and polishing of the conductive layer 30.

[0039] Reference is now made to Figure 16, which illustrates the structure of Figure 13 but with the polysilicon gate layers 32 and portions of the thin gate oxide layer 29 etched about 100 Angstroms to about 500 Angstroms. The polysilicon gate layers 32 and portions of the thin gate oxide layer 29 and etched selective to the silicon nitride 14 of the regions A to obtain recessed regions 34 and polyisilicon gates 33, shown in Figure 16.

[0040] In an exemplary embodiment of the invention, a dielectric layer 35 (Figure 17) is next formed over the polyisilicon gates 33 to completely fill the recessed regions 34 of Figure 16. The dielectric layer 35 may include an oxide material, for example, and may be formed by conventional deposition methods followed by polishing by CMP, for example.

[0041] Alternatively, a layer of metal capable of forming a silicide (not shown) may be deposited over the polysilicon gates 33 to a thickness of about 200 Angstroms to about 500 Angstroms. For deposition, sputtering by RF or DC may be employed but other similar methods such as CVD may be used. Subsequent to the deposition of the metal capable of forming a silicide, substrate 10 undergoes a rapid thermal anneal (RTA), typically for about 10 to 60 seconds, using a nitrogen ambient, at about 600°C to about 850°C so that the metal in direct contact with the polysilicon gates 33 is converted to its silicide. As shown in Figure 18, silicide regions 37 form conductive regions on top of the polysilicon gates 33. Preferably, the refractory metal has low resistance and low resistivity as a silicide. However, the refractory metal silicide may comprise any refractory metal, including but not limiting to titanium, cobalt, tungsten, tantalum, molybdenum, and platinum.

[0042] After the removal with a selective etchant of any unreacted metal, the nitride portions of regions A are removed (Figure 19) by etching, for example, so that the formation of gate stacks 90 (Figure 20) of DRAM memory device 100 be completed. Although the following processing steps for the completion of the gate stacks 90 will refer to and illustrate the silicide regions 37 formed over the polysilicon gates 33, it must be understood that the present invention is not limited to this embodiment, and other embodiments such as the formation of gate stacks comprising a dielectric material, such as the dielectric material 35 (Figure 17), formed over the polysilicon gate, are also contemplated. In any event, a cap material is deposited over substrate 10 and the substrate top surface is planarized so that cap regions 60 (Figure 20) are formed over the silicide regions 37. The cap material may be formed of silicon dielectrics such as silicon nitride or silicon oxide, but TEOS or carbides may be used also.

[0043] At this point recessed gate stacks 90 (Figure 20) each having gate oxide layer 29, polysilicon gate 33, silicide region 37 and nitride cap 60 have been formed. The recessed gate stacks 90 may now be used in a conventional implant

process where the gate structures are needed to mask the dopant implantation of source regions 92 (Figure 21) and drain regions 94 (Figure 21) of the adjacent transistors defined by the gate stacks.

[0044] The next step in the flow process is the formation of nitride spacers 95a, 95b also illustrated in Figure 21. The recessed gate stacks 90 protected by nitride spacers 95a, 95b can now undergo conventional processing steps for the formation of contact openings for conductors and/or capacitors into semiconductor substrate 10 through an oxide layer 93 such as BPSG, for example. Thus, conventional processing steps can be carried out to form a conductor 96 and capacitors 97 as well as other interconnect structures necessary to produce a semiconductor device such as the DRAM memory device 100, all illustrated in Figure 22.

[0045] The recessed gate stacks 90 (Figures 20-22) formed in accordance with embodiments of the present invention could be used in any integrated circuit structure such as in a processor-based system 400 which includes a memory circuit 448, for example the DRAM memory device 100, as illustrated in Figure 23. A processor system, such as a computer system, generally comprises a central processing unit (CPU) 444, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 446 over a bus 452. The memory 448 communicates with the system over bus 452.

[0046] The above description and drawings are only to be considered illustrative of exemplary embodiments which achieve the features and advantages of the present invention. Modification and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the present invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

CLAIMS

[0047] What is claimed is:

1. A method of forming gate structures for a semiconductor device, comprising:

forming an insulating layer over a semiconductor substrate;

defining a first set of trenches in said semiconductor substrate and extending through said insulating layer;

filling said first set of trenches with an insulating material to form isolation trenches;

defining a second set of trenches in said semiconductor substrate which extend through said insulating layer in a direction orthogonal to said first set of trenches;

etching regions of said isolation trenches to form recessed isolation trenches adjacent to said second set of trenches;

forming a gate oxide within said second set of trenches;

forming a conductive layer over said gate oxide and said recessed isolation trenches; and

polishing said conductive layer relative to said recessed isolation trenches to form a conductive gate.

2. The method of claim 1 further comprising forming a protective layer over said conductive gate.

3. The method of claim 1 further comprising forming an oxide layer between said semiconductor substrate and said insulating layer.

4. The method of claim 1, wherein said first set of trenches are etched to a depth of about 1,000 Angstroms to about 10,000 Angstroms.

5. The method of claim 1, wherein said second set of trenches are etched to a depth of about 1,000 Angstroms to about 10,000 Angstroms.

6. The method of claim 1, wherein said second set of trenches are etched thorough said semiconductor substrate to a depth of about 500 Angstroms to about 5,000 Angstroms.

7. The method of claim 1, wherein said act of etching regions of said isolation trenches includes plasma etching said insulating material.

8. The method of claim 7, wherein said insulating material is etched about 500 Angstroms to about 3,000 Angstroms.

9. The method of claim 1, wherein said conductive layer is formed of polysilicon.

10. The method of claim 1, wherein said conductive layer is formed by deposition.

11. The method of claim 1 further comprising etching said conductive gate to form a recessed conductive gate.

12. The method of claim 11, wherein said conductive gate is etched about 100 Angstroms to about 300 Angstroms

13. The method of claim 12 further comprising forming a dielectric layer over said recessed conductive gate.

14. The method of claim 12 further comprising forming a silicide layer over said recessed conductive gate.

15. The method of claim 1, wherein said insulating layer is formed of a material selected from the group consisting of silicon nitride and silicon oxide.

16. The method of claim 1 further comprising forming insulating spacers on sidewalls of said gate structures.

17. The method of claim 1, wherein said insulating material is formed of an oxide material.

18. A method of forming a memory cell, comprising providing an insulating layer over a silicon substrate and forming a transistor including a gate structure fabricated within said silicon substrate, a source/drain region in said silicon substrate disposed adjacent to said gate structure, and a capacitor formed over said source/drain region, wherein said act of forming said gate structure further comprises:

forming at least one isolation trench filled with an insulating material in said silicon substrate, said isolation trench extending through said insulating layer;

defining at least one transistor trench in said silicon substrate which extends through said insulating layer in a direction orthogonal to said isolation trench;

etching regions of said isolation trench to form at least one recessed isolation trench adjacent to said transistor trench;

forming a gate oxide layer within said transistor trench;

forming a conductive layer over said gate oxide layer and extending over said recessed isolation trench;

polishing said conductive layer relative to said recessed isolation trench to form a conductive gate; and

forming a protective layer over said conductive gate.

19. The method of claim 18, wherein said isolation trench is etched to a depth of about 1,000 Angstroms to about 10,000 Angstroms.

20. The method of claim 18, wherein said transistor trench is etched to a depth of about 1,000 Angstroms to about 10,000 Angstroms.

21. The method of claim 18, wherein said transistor trench is etched through said silicon substrate to a depth of about 500 Angstroms to about 5,000 Angstroms.

22. The method of claim 18, wherein said act of etching regions of said isolation trench comprises plasma etching said insulating material.

23. The method of claim 22, wherein said insulating material is etched about 500 Angstroms to about 3,000 Angstroms.

24. The method of claim 18, wherein said conductive layer is formed of polysilicon.

25. The method of claim 18, wherein said conductive layer is formed by deposition.

26. The method of claim 18 further comprising etching said conductive gate to form a recessed conductive gate.

27. The method of claim 26, wherein said conductive gate is etched about 100 Angstroms to about 300 Angstroms

28. The method of claim 26 further comprising forming a dielectric layer over said recessed conductive gate.

29. The method of claim 26 further comprising forming a silicide layer over said recessed conductive gate.

30. The method of claim 18, wherein said insulating layer is formed of a material selected from the group consisting of silicon nitride and silicon oxide.

31. The method of claim 18, wherein said insulating material is formed of an oxide material.

32. The method of claim 18 further comprising forming insulating spacers on sidewalls of said gate structure.

33. The method of claim 18, wherein said memory cell is a DRAM memory cell.

34. The method of claim 18, wherein said memory cell is part of an integrated circuit.

35. The method of claim 18, wherein said memory cell is part of a memory circuit coupled to a processor, wherein at least one of said processor and said memory circuit contains said gate structure.