memory strings MS in the X and Y directions, the plurality of memory cells MC are arranged 3-dimensionally in the X, Y, and Z directions.

[0036]FIG. 1 illustrates a region of an end of the foregoing first memory cell array 10a in the X direction. A stair structure 29 of the electrode layers WL extending in the X direction is formed at an end of a first memory cell array region 28a in which the plurality of memory cells MC are arranged. In the stair structure 29, the ends of each of the electrode layers WL of the layers in the X direction are formed in a stair shape. A plurality of contact plugs 30 connected to each of the electrode layers WL of the layers formed in the stair shape are formed in the stair structure 29. The contact plugs 30 are connected to each of the electrode layers WL of the layers in the stair shape to penetrate through the interlayer insulating layer 31.

[0037]In the stair structure 29, the selection gates SG (the drain-side selection gate SGD and the source-side selection gate SGS) are connected to contact plugs (first plugs) 32.

[0038]The contact plug 30 connected to the electrode layer WL is connected a word wiring layer 33. The contact plug 32 connected to the selection gate SG is connected to a selection gate wiring layer 34. The word wiring layer 33 and the selection gate wiring layer 34 are formed in the same layer.

[0039]The first memory cell array layer 200 does not include

a substrate. A first source-side wiring layer 19a is formed to be closer to the second surface side than a first source line SL.

At least parts of the word wiring layer 33 and the selection gate wiring layer 34 are led as a word-line lead portion (a first wiring layer) 35 and a selection-gate-line lead portion 36, by other wiring layers or plugs, to the outside of the first memory cell array region 28a when viewed in a direction vertical to the first surface. The word-line lead portion 35 and the selection-gate-line lead portion 36 led to the outside of the first memory cell array region 28a are connected to a first signal line extraction electrode (a signal line extraction electrode) 37a formed outside the first memory cell array region 28a.

[0040]The channel body 20 of the first columnar portion 13a is electrically connected to the first bit line BL and the first source line SL. Similarly, at least parts of the first bit line BL and the first source line SL are led as a first bit-line lead portion and a first source-line lead portion (not illustrated) by other wiring layers or plugs to the outside of the first memory cell array region 28a when viewed in a direction vertical to the first surface. The first bit-line lead portion and the first source-line lead portion led outside the first memory cell array region 28a are connected to the first signal line extraction electrode 37a formed outside the first memory cell array region 28a.

[0041]A first surface wiring layer (a second junction metal) 38a and a second surface wiring layer (a third junction metal) 39a are formed on the first surface Sa1 and the second surface Sa2 of the first memory cell array layer 200. The first surface wiring layer 38a and the second surface wiring layer 39a are embedded in the first surface Sa1 and the second surface Sa2, respectively, so that front surfaces are exposed from interlayer insulating layers (not illustrated). Here, for example, the first signal line extraction electrode 37a is electrically connected to the first surface wiring layer 38a and the second surface wiring layer 39a formed on the first surface Sa1 and the second surface Sa2 of the first memory cell array layer 200, respectively. The first signal line extraction electrode 37a, the first surface wiring layer 38a, and the second surface wiring layer 39a penetrate through the first memory cell array layer 200.

[0042]First external connection electrodes (first contacts) 40a are formed outside the first memory cell array region 28a. That is, the first external connection electrodes 40a are formed in a region further outside than the stair structure in the memory cell array. The first external connection electrodes 40a are electrically connected to the first surface wiring layer 38a and the second surface wiring layer 39a formed on the first surface Sa1 and the second surface Sa2 of the first memory cell array layer 200. The first surface wiring layer 38a and the second surface wiring layer 39a are embedded in the first

surface Sa1 and the second surface Sa2, respectively, so that front surfaces are exposed from the interlayer insulating layers (not illustrated). The first external connection electrode 40a, the first surface wiring layer 38a, and the second surface wiring layer 39a penetrate through the first memory cell array layer 200.

[0043]The peripheral circuit layer 100 includes a circuit board 1. The circuit board 1 of the peripheral circuit layer 100 is, for example, a silicon substrate. A control circuit is formed on a circuit formation surface of the circuit board 1 of the peripheral circuit layer. As the control circuit, an integrated circuit including a transistor is formed. The transistor has a MOSFET structure that has a gate electrode and a source/drain region. The source/drain region of the MOSFET is connected to a circuit-side connection electrode 41 by another wiring layer or a plug. The circuit-side connection electrode 41 is electrically connected to a circuit-side wiring layer (a first junction metal) 42 formed on the circuit formation surface of the peripheral circuit layer 100. The circuit-side wiring layer 42 is embedded in the circuit formation surface so that a front surface is exposed from an interlayer insulating layer (not illustrated).

[0044]The second memory cell array layer 300 has the same configuration as the first memory cell array layer 200 illustrated in FIGS. 1 to 4. That is, the second memory cell

array layer 300 includes a third surface (lower surface) Sb1 and a fourth surface (upper surface) Sb2 opposite to the third surface in FIG. 1 and includes a second memory cell array 10b with a 3-dimensional structure. The other same configuration will not be described.

[0045]The second memory cell array layer 300 does not include a substrate. A second source-side wiring layer 19b is further formed to be closer to the fourth surface than the second source line SL.

As in the first memory cell array layer 200, at least parts of the word wiring layer 33 and the selection gate wiring layer 34 are led as a word-line lead portion 35 and a selection-gate-line lead portion 36 by other wiring layers or plugs to the outside of a second memory cell array region 28b when viewed in a direction vertical to the third surface. The word-line lead portion 35 and the selection-gate-line lead portion 36 led outside the second memory cell array region 28b are connected to a second signal line extraction electrode 37b formed outside the second memory cell array region 28b.

[0046]The channel body 20 of the second columnar portion 13b is electrically connected to the second bit line BL and the second source line SL. Similarly, at least parts of the second bit line BL and the second source line SL are led as a second bit-line lead portion and a second source-line lead portion by other wiring layers or plugs to the outside of the second

memory cell array region 28b when viewed in the direction vertical to the third surface. The second bit-line lead portion and the second source-line lead portion led outside the second memory cell array region 28b are connected to the second signal line extraction electrode 37b formed outside the second memory cell array region 28b. A configuration of the second memory cell array region 28b is the same as that inside the first memory cell array layer 200, and thus reference numerals are not given.

[0047]A third surface wiring layer (a fourth junction metal) 38b and a fourth surface wiring layer 39b are formed on the third surface Sb1 and the fourth surface Sb2 of the second memory cell array layer 300. The third surface wiring layer 38b and the fourth surface wiring layer 39b are embedded in the third surface Sb1 and the fourth surface Sb2, respectively, so that front surfaces are exposed from interlayer insulating layers (not illustrated). Here, for example, the second signal line extraction electrode 37b is electrically connected to the third surface wiring layer 38b and the fourth surface wiring layer 39b formed on the third surface and the fourth surface of the second memory cell array layer 300, respectively. The second signal line extraction electrode and the third and fourth surface wiring layers penetrate through the second memory cell array layer 300.

[0048]Second external connection electrodes (second contacts) 40b are formed outside the second memory cell array region 28b. That is, the

second external connection electrodes 40b are formed in a region further outside than the stair structure in the memory cell array. The second external connection electrodes 40b are electrically connected to the third surface wiring layer 38b and the fourth surface wiring layer 39b formed on the third surface Sb1 and the fourth surface Sb2 of the second memory cell array layer 300. The third surface wiring layer 38b and the fourth surface wiring layer 39b are embedded in the third surface Sb1 and the fourth surface Sb2, respectively, so that front surfaces are exposed from interlayer insulating layers (not illustrated). The second external connection electrodes 40b, the third surface wiring layer 38b, and the fourth surface wiring layer 39b penetrate through the second memory cell array layer 300. An external connection pad (a pad) 52 is formed on a surface wiring layer electrically connected to the second external connection electrodes 40b among the fourth surface wiring layers 39b.

[0049]As illustrated in FIG. 1, the first surface wiring layer 38a formed on the first surface Sa1 is attached to be bonded with the circuit-side wiring layer 42 formed on the circuit formation surface. The first surface wiring layer 38a and the circuit-side wiring layer 42 are formed of, for example, copper or copper alloys which have copper as a main component. An insulating film (not illustrated) is formed around the first surface wiring layer 38a and the circuit-side wiring layer 42.

WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a substrate;

a peripheral circuit layer having a transistor provided on the substrate and a first junction metal provided on a first surface;

a first memory cell array layer provided on the first surface including a first stacked structure in which a plurality of first electrode layers and a plurality of first insulating layers are alternately stacked in the first direction, a first columnar structure extending in the first direction in the first stacked structure and forming a plurality of memory cells at the intersection with the plurality of first electrode layers, a first wiring layer provided between the first stacked structure and the first surface, a plug first electrically connecting one of the plurality of first electrode layers with the first wiring layer and extending in the first direction and a second junction metal provided on the first junction metal and electrically connected with the first wiring layer and a third junction metal on a second surface which is an opposite the first surface; and

a second memory cell array layer provided on the first memory cell array layer including a second stacked structure in which a plurality of second electrode layers and a plurality of second insulating layers are alternately stacked in the first direction, a second columnar structure extending in the first direction in the second stacked structure and forming a plurality of memory cells at the intersection with the plurality of second electrode layers, a second wiring layer provided between the first stacked structure and the second stacked structure, a second plug electrically connecting one of the plurality of second electrode layers with the second wiring layer and extending in the first direction and a fourth junction metal provided on the third junction metal and electrically connected with the second wiring layer and an electrode pad on a fourth surface which is an opposite the second surface.

2. The semiconductor memory device according to claim 1,

wherein the first junction metal and the second junction metal are directly bonded and the third junction metal and the fourth junction metal are directly bonded.

3. The semiconductor memory device according to claim 1, wherein the memory cell array layer comprises:

a signal line extraction electrode that electrically connecting the first wiring layer and the second wiring layer and extending in the first direction.

4. The semiconductor memory device according to claim 3, further comprising,

a first bit line electrically connected to the first surface side of the first columnar structure; and

a first source line electrically connected to the second surface side of the first columnar structure,

wherein the second wiring layer is provided on the second surface side of the first source line.

5. The semiconductor memory device according to any preceding claim, further comprising,

a memory string having memory cells storing the ID of the first memory cell array layer and the second memory cell layer provided in at least one of the first memory cell array layer and the second memory cell array layer,

a transistor provided in at least one of the first memory cell array layer and the second memory cell array layer.

6. The semiconductor memory device according to claim 5,

wherein the transistor is provided in each of the first memory cell array layer and the second memory cell array layer.

7. The semiconductor memory device according to claim 1, further comprising a first contact electrically connected to the pad and through the second memory cell array layer; and

a second contact electrically connected to the first contact and through the first memory cell array layer,

wherein the second contact electrically connected to the peripheral circuit layer.