CIRCUIT TO REDUCE GATE-INDUCED DRAIN LEAKAGE (GIDL) CURRENT IN THIN GATE OXIDE MOSFETs

Abstract:

An integrated circuit structure that provides a FET device with reduced GIDL current. The circuit includes a semiconductor layer, an oxide layer formed on the semiconductor layer, a gate structure having a defined leading edge that is formed on the oxide layer, and an overlap region beneath the gate structure and adjacent the leading edge. The overlap region has a predetermined ion implant concentration that is sufficient to increase the electrical gate oxide thickness in the overlap region without an increase in the physical gate oxide thickness in the overlap region.

Fig. 3E