

METHOD OF TESTING FOR POWER AND GROUND CONTINUITY OF A
SEMICONDUCTOR DEVICE

ABSTRACT OF THE INVENTION

A method of testing for power and ground continuity of a semiconductor device having Input and Output (IO) pins and at least a pair of power and ground pins includes identifying the power and ground pins of the device. A victim pin is selected from the IO pins of the device for each pair of the power and ground pins, and an aggressor pin for each victim pin is selected from the remaining IO pins. The aggressor pins are toggled between a high state and a low state. A level of switching noise on each victim pin is measured, and the measured levels of switching noise are compared with predetermined data to determine power and ground continuity of the device.

[FIG. 1]