

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
22 June 2023 (22.06.2023)



(10) International Publication Number
WO 2023/110850 A1

- (51) International Patent Classification:
H10B 41/27 (2023.01) *H10B 43/27* (2023.01)
- (21) International Application Number:
PCT/EP2022/085586
- (22) International Filing Date:
13 December 2022 (13.12.2022)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
21215436.3 17 December 2021 (17.12.2021) EP
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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH,

(54) Title: A MEMORY DEVICE

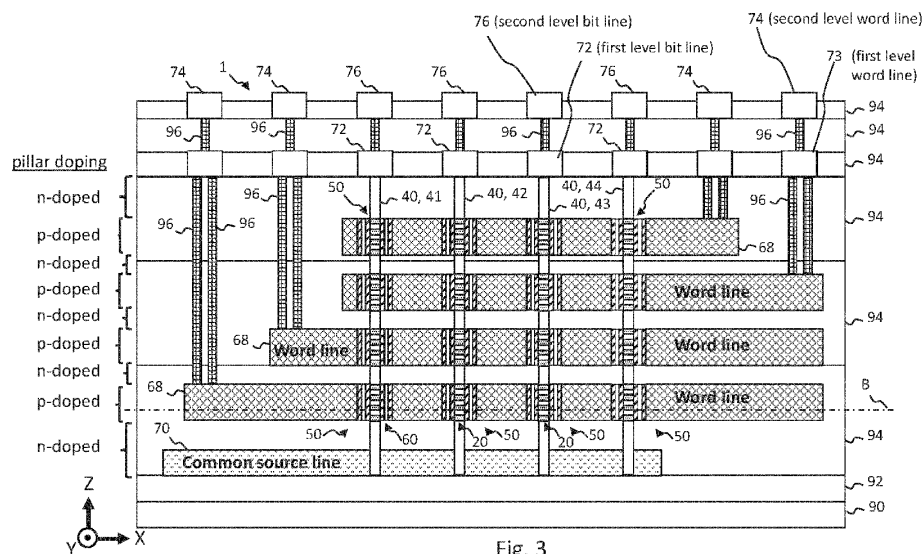


Fig. 3

(57) Abstract: A memory device (1) comprising a semiconductor pillar (40) and at least one memory cell (50) associated with the pillar (40), wherein each of the at least one memory cells (50) comprises a charge trap (60) and a transistor (2), wherein, for each of the at least one memory cells (50): the charge trap (60) of the memory cell (50) is configured to control a threshold voltage of the transistor (2) of the memory cell (50) by a stored charge; and the transistor (2) of the memory cell (50) comprises a source pillar segment (10), a drain pillar segment (14) and a body pillar segment (12), wherein at least one p-doped pillar segment (10, 12, 14) of the transistor (2) comprises a plurality of semiconductor layers (20), wherein layers of the plurality of semiconductor layers (20) are made of AlGaIn or GaN, and wherein the plurality of semiconductor layers (20) is configured such that every second layer has a lower aluminum content than the neighboring mutually opposite layers thereof.

[Continued on next page]

TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS,
ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- *with international search report (Art. 21(3))*
- *in black and white; the international application as filed contained color or greyscale and is available for download from PATENTSCOPE*