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PARALLEL ANALOG-TO-DIGITAL CONVERTER**BACKGROUND OF THE INVENTION****Field of the Invention**

The present invention relates to a parallel analog-to-digital converter (ADC) preferably used in image-display processors that require high-speed conversion. More specifically, the invention relates to a parallel ADC that can greatly reduce the number of comparators required.

Prior Art

A conventional, high-speed, n-bit parallel ADC is configured as shown in Fig. 1. In Fig. 1, numeral 2 designates a reference-voltage-generating circuit having a plurality of resistors connected serially. Four resistors 4, one at the far left, one at the far right, and two at the center are of $R/2 \Omega$, and the other resistors 6 are of $R \Omega$. To end terminals Ta and Tb of reference-voltage-generating circuit 2 are applied positive reference voltage V_{RH} and negative reference voltage V_{RL} , respectively (these reference voltages are called fundamental reference voltages in contrast to individual reference voltages mentioned below). In addition, to center terminal Tc is applied center voltage V_{RM} which has a voltage between the positive reference voltage V_{RH} and the negative reference voltage V_{RL} , e.g., 0 volt.



The voltage between terminals Ta and Tb of reference-voltage-generating circuit 2 is equally divided into 2^n levels by resistors 4 and 6. Consequently, individual-reference-voltage nodes P1 to Pk ($k = 2^n - 1$) presents individual reference voltages V1 to Vk. Any two consecutive voltages of these nodes are of a constant difference. Each of these reference voltages V1 to Vk is applied to one input of each of the comparators C1 to Ck, respectively. To the other input of each comparator thereof, analog input voltage V_{in} to be converted is simultaneously applied through input terminal T_{in} , respectively. Hence, each comparator simultaneously compares analog input voltage V_{in} with individual reference voltages V1 to Vk, and supplies the result of the comparisons to encoder 8. Encoder 8 converts the k-bit comparator outputs into an n-bit binary code. Thus, analog input voltage V_{in} applied to input terminal T_{in} is converted into n-bit digital data at a very high speed, and the digital data is produced from output terminal T_{out} .

The conventional n-bit parallel ADC described above, however, necessitates $2^n - 1$ ($= k$; the same number as that of individual reference voltages V1 to Vk) comparators because the reference voltages V1 to Vk are generated by equally dividing the voltage between positive reference voltage V_{RH} and negative reference voltage V_{RL} into 2^n . For this reason, a great number of high-precision comparators are required for an increasing number of bits of digital output data. In addition, the larger the number of bits, the more complex encoder 8 must be. These factors hinder



the production of low-cost, high-density integrated circuits of the ADC.

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a parallel ADC that can greatly reduce the required number of comparators, thus achieving a small-scale ADC while increasing the number of bits thereof.

Another object of the invention is to provide a parallel ADC of low cost and with a high density of integrated circuits.

It is a further object of the invention to provide a parallel ADC, preferably applied to image-display processors that handle video signals relating to human perception, which is subject to the Weber-Fechner Law, which says that sensory intensity is proportional to the logarithm of stimulus intensity.

According to one aspect of the present invention, there is provided a parallel analog-to-digital converter comprising:

reference-voltage-generating means for generating a plurality of individual reference voltages;

a plurality of comparator means for comparing each of the individual reference voltages with an analog input voltage; and

encoding means for encoding outputs of the comparator means into digital data corresponding to the analog input;

whereby the reference-voltage-generating means divides



fundamental reference voltage into exponential reference voltages according to an exponential scale, and further divides each voltage between two consecutive exponential reference voltages into a plurality of the individual reference voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the configuration of a conventional parallel ADC; and

Fig. 2 is a block diagram showing the configuration of a parallel ADC according to an embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention will now be described with reference to the accompanying drawings.

Figure 2 is a configuration of a parallel ADC according to an embodiment of the present invention.

In Fig. 2, numeral 12 designates a reference-voltage-generating circuit which is made up of an R-2R resistor ladder network. The R-2R resistor ladder network, as is well-known, consists of a combination of R- Ω resistors 14, and 2R- Ω resistors 16. There are (n - 1) resistors 14 which are connected serially across positive reference voltage V_{RH} and center voltage V_{RM} , and other (n - 1) resistors 14 connected across negative reference voltage V_{RL} and central voltage V_{RM} , where n is the number of bits of ADC, and 1



is an integer appropriately selected. Each connecting point of resistors 14 (called an exponential node hereafter) which is positive is designated by $NP_i, NP_{i+1}, \dots, NP_{n-2}, NP_{n-1} (= V_{RH})$; and each exponential node which is negative is denoted as $NN_i, NN_{i+1}, \dots, NN_{n-2}, NN_{n-1} (= V_{RL})$. Each exponential node NP_{i+1} to NP_{n-2} and NN_{i+1} to NN_{n-2} is connected to center terminal T_c through $2R-\Omega$ resistor 16.

The R-2R resistor ladder network 12 thus configured, as is well-known, generates individual reference voltages according to an exponential scale (these individual reference voltages are called exponential reference voltages hereafter): exponential reference voltage V_{RH} is produced from exponential node NP_{n-1} ; exponential reference voltage $V_{RH}/2$ is produced from exponential node NP_{n-2} ; exponential reference voltage $V_{RH}/2^2$, from node NP_{n-3} ; ... ; exponential reference voltage $V_{RH}/2^{(n-i-2)}$, from node NP_{i+1} ; exponential reference voltage $V_{RH}/2^{(n-i-1)}$, from node NP_i . In a similar manner, each negative exponential reference voltage $V_{RL}, V_{RL}/2, V_{RL}/2^2, \dots, V_{RL}/2^{(n-i-2)},$ and $V_{RL}/2^{(n-i-1)}$ is produced from each exponential node $NN_{n-1}, NN_{n-2}, NN_{n-3}, \dots, NN_{i+1},$ and NN_i .

Each resistor 14 placed between two consecutive exponential nodes consists of 2^i resistors 14a of equal value. As a result, between two consecutive exponential nodes, there are provided 2^i individual nodes (including one of the two exponential nodes) at an equal interval. Thus, $m (= 2^{i+1} \times (n-i))$ individual nodes $P_1, P_2, P_3, \dots, P_{m-1}, P_m$, including exponential nodes, are formed



between terminals T_a and T_b , generating individual reference voltages V_1 to V_m .

Each individual reference voltage V_j ($j = 1$ to m) is applied to one input terminal of comparator C_j , and is compared with analog input voltage V_i simultaneously applied to the other input terminal thereof via input terminal T_{in} . These comparisons are performed simultaneously by all the comparators C_1 to C_m , and the results of the comparisons are applied to encoder 18. Encoder 18 converts the m -bit input data into a n -bit binary code. Thus, analog input voltage V_{in} supplied via input terminal T_{in} , is converted into n -bit digital data, and produced from n -bit output terminal T_{out} .

A more specific case will now be described using an example of 9-bit ADC ($n = 9$). When integer i is specified as $i = 4$, the number of positive exponential nodes NP_i to NP_{n-1} is 5 ($= n - i$), which is the same number as that of the negative exponential nodes NN_i to NN_{n-1} . Additionally, between two consecutive exponential nodes, there are 16 ($= 2^4$) nodes, and so the total number of nodes is 160 ($= 16 \times 10$).

In this case, positive exponential reference voltages are V_{RH} , $V_{RH}/2$, $V_{RH}/4$, $V_{RH}/8$, $V_{RH}/16$; and negative exponential reference voltages are V_{RL} , $V_{RL}/2$, $V_{RL}/4$, $V_{RL}/8$, $V_{RL}/16$. Furthermore, each voltage across each resistor 14, i.e., each voltage between two consecutive exponential reference voltages (for example, a voltage between V_{RH} and $V_{RH}/2$, or between $V_{RH}/2$ and $V_{RH}/4$, etc.) is divided into 16 equal parts, producing 160 individual reference





What is claimed is:

1. A parallel analog-to-digital converter comprising:

reference-voltage-generating means (12) for generating a plurality of individual reference voltages;

a plurality of comparator means (C_1 to C_m) for comparing each of said individual reference voltages with an analog input voltage; and

encoding means (18) for encoding outputs of said comparator means into digital data corresponding to said analog input;

whereby said reference-voltage-generating means divides fundamental reference voltage into exponential reference voltages according to an exponential scale, and further divides each voltage between two consecutive exponential reference voltages into a plurality of said individual reference voltages.

2. A parallel analog-to-digital converter according to claim 1, wherein said reference voltage generating means consists of an R-2R resistor ladder network that is made up of R- Ω resistors (14) and 2R- Ω resistors (16).

3. A parallel analog-to-digital converter according to claim 2, wherein each of said R- Ω resistors consists of a plurality of resistors (14a) of the same value connected serially, each connecting point of said resistors of the same value producing said individual reference voltage.

