

1 COUPLER FOR MANAGING COMMUNICATION BETWEEN A PORTABLE DATA MEDIUM
2 AND A DATA EXCHANGE DEVICE, AND DATA EXCHANGE DEVICE THEREFOR
3

4 The present invention relates to a coupler for managing
5 communication between a portable data medium and a data exchange
6 device, which communication uses, on the data exchange device
7 end, at least one data transmission signal and two control
8 signals delivered by the data exchange device in one of two first
9 and second predetermined input sequences, and on the data medium
10 end, at least one data medium power supply signal, one data
11 medium reset signal, and one data transmission signal.

12 This coupler can be used for example to limit access to a
13 computer network to authorized persons who hold for this purpose
14 a portable data medium such as a chip card incorporating a
15 microprocessor or micro-wired logical circuits which define areas
16 to which access is controlled and can therefore contain secret
17 information such as cryptographic keys (see for example the
18 portable object described in US patent No. 4 211 919).

19 The protocol for exchange with a chip card is codified by
20 international standard ISO7816-3, which defines the sequence for
21 generating the signals applied to the chip card, namely a power
22 supply signal VCC, a power supply signal for the memories VPP, a
23 reset signal RST, a clock signal CLK, and a data exchange signal
24 I/O. The standard very precisely defines the order in which
25 these signals must appear and then disappear.

26 A coupler of this type can, in a known way, comprise a
27 microprocessor which controls the interface with the portable
28 data medium and is controlled by the data exchange device which
29 constitutes the central processor. This microprocessor slows
30 down the exchange process between the asynchronous data exchange
31 device and the portable data medium.

32 In order to avoid the use of a microprocessor in the
33 coupler, it has been suggested that some of the signals supplied
34 by a serial port of the data exchange device, typically a port
35 according to the standard RS 232, namely a "clear to send" signal
36 CTS, a request to send signal RTS, a "data carrier detect" signal

1 DCD, a "data terminal ready" signal DTR, a data transmission
2 signal TX and a data reception signal RX, be used to generate the
3 signals applied to the portable data medium.

4 A coupler of this type is described in US patent 5 149 945.
5 The sequencing of the signals supplied to the chip card is
6 defined exclusively by the data exchange device, without the
7 coupler's being able to intervene in this sequencing so as to
8 allow for particular operating situations on the chip card end.

9 One consequence is that the above-mentioned standard is not
10 always met, particularly when the chip card is reinserted after
11 having been removed during a communication with the data exchange
12 device, since the chip card is powered up again immediately,
13 without allowing the data exchange device the necessary time to
14 react in so as to impose a re-powering up in accordance with the
15 standardized sequence.

16 However, it appears to be desirable for the coupler to be
17 able to intervene in the sequencing of the signals delivered by
18 the data exchange device in order to supply a wider range of
19 modes for controlling or testing the chip card.

20 The object of the invention is to eliminate the above-
21 mentioned drawbacks and for this purpose it relates to a coupler
22 as described at the beginning of the disclosure, characterized in
23 that:

24 - it comprises bistable control means input-activated by at
25 least the two control signals delivered by the data exchange
26 device and designed to output at least the power supply signal
27 and reset signal of the data medium in one of two first and
28 second predetermined output sequences, which is a function of the
29 input sequence;

30 - the first input sequence alone is able to generate a first
31 output sequence which successively comprises the power supply
32 signal and reset signal of the data medium, which allow the data
33 exchange device to enter into communication with the portable
34 data medium.

35 Thus, the bistable control means make it possible to

1 intervene in the sequencing of the signals delivered by the data
2 exchange device so as to produce, or not to produce, from these
3 signals and as a function of them, the signals directed to the
4 chip card, which will be made clearer in the description of the
5 appended figures. The bistable control means make it possible to
6 control the chip card, both as a function of the instantaneous
7 behavior of the data exchange device and as a function of that of
8 the chip card.

9 The invention also relates to a data exchange device
10 designed to manage communication with a portable data medium and
11 comprising for this purpose data exchange means and coupling
12 means such as the coupler defined above, which coupling means
13 also comprise means for detecting the presence of the portable
14 data medium, designed to deliver to the data exchange means a
15 signal of the presence of the medium when the portable data
16 medium is cooperating with the coupling means, upon reception of
17 a first of the control signals, and which data exchange means are
18 designed to cyclically send to the coupling means, before a
19 communication with the portable data medium, the second input
20 sequence until they receive the signal of the presence of the
21 portable data medium.

22 Other characteristics and advantages of the invention will
23 emerge from the following description, given as an illustrative
24 and non-limiting example, in reference to the appended drawings,
25 in which:

26 Fig. 1 represents a configuration comprising a coupler
27 according to the invention,

28 Fig. 2 is a block diagram of the coupler,

29 Fig. 3 illustrates the protocol for exchange with a chip
30 card according to the standard ISO 7816-3,

31 Fig. 4 represents the sequencing of the signals supplied by
32 the data exchange device,

33 Fig. 5 is a partial diagram of the coupler relative to the
34 internal power supply,

35 Fig. 6 is a partial diagram of the coupler relative to the

1 generation of the control signals applied to the portable data
2 medium, and

3 Fig. 7 is a partial diagram of the coupler relative to the
4 transfer of the data signals.

5 Fig. 1 represents a typical configuration of a personal
6 computer 1 wherein a port connector 2, for example for a serial
7 port of the RS 232 type, is connected by a cable 3 to a serial
8 port connector 4 of a coupler 5. The coupler 5 also includes a
9 chip card connector 6 which can receive a chip card 7. The
10 interface device 5 serves to manage the data exchanges between
11 the chip card 7 and the personal computer 1; this coupler 5 can,
12 in particular, be used for security functions, for example to
13 control access to computers or to computing networks, the
14 authorized persons being provided with a chip-based
15 identification card.

16 Fig. 2 is the block diagram of the coupler 5, which receives
17 the signals RTS, DTR, CTS, TX, RX and DCD from the serial link of
18 the computer 1 through the serial port connector 4; its chip card
19 connector 6 includes plugs connected to the signals VCC, RST, CLK
20 and I/O of the chip card as well as to a card presence switch 31
21 which is closed by the chip card when the latter is inserted into
22 the connector 6.

23 The signal DTR, via a chip card switch 31, and the signal
24 RTS are sent to a bistable circuit 25 which controls a power
25 supply circuit 12 and a blocking circuit 23. The role of the
26 bistable circuit 25 is to authorize, first of all, the provision
27 of a supply voltage VCC directed to circuits of the coupler,
28 particularly to circuits 29, 32, 41, and to the chip card 7, and
29 secondly, the transmission of the signal RST through the blocking
30 circuit 23. This authorization is delivered only if the signals
31 DTR, RTS are activated in the order DTR, RTS.

32 The card presence switch 31 is connected to the signal CTS
33 in order to return to the serial port connector 4 the chip card
34 presence information.

35 The signal VCC is sent to an interface circuit 29 which

1 generates the signal RST, to a clock generator 32 which generates
2 the signal CLK, and to an interface circuit 41 which generates
3 the signal I/O, thus guaranteeing that the signals RST, CLK and
4 I/O have a voltage lower than that of the signal VCC, since they
5 are derived from the latter, in accordance with the requirements
6 of the standard ISO7816-3.

7 The coupler 5 also includes a power source 11 which drives
8 both the power supply circuit 12 supplying the regulated signal
9 VCC, and a comparison circuit 14 which compares the level of the
10 power source 11 with a reference, constituted in this case by the
11 regulated signal VCC.

12 The comparison circuit 14 outputs a so-called "low" level of
13 the power source and transmits it through the interface circuit
14 41 to the signal DCD.

15 The reference potential signal GND is transmitted directly
16 from the computer to the chip card, through the coupler 5.

17 Generally, data exchanges with a chip card are codified by
18 the standard ISO 7816 whose section 7816-3 relates to the
19 sequencing of the various signals applied to the chip card,
20 namely the reference potential signal GND, the power supply
21 signal VCC, the memory power supply signal VPP, the clock signal
22 CLK, the reset signal RST and the data exchange signal I/O, as
23 shown in the timing diagram in Fig. 3.

24 It may be seen that, during the establishment of the
25 exchange, the signals VCC, VPP, CLK and RST must be supplied in
26 that order; the signal VPP, which is generally not used, is short
27 circuited by connection with the signal VCC. At the end of the
28 exchange, the above-mentioned signals must disappear in the
29 reverse order.

30 Fig. 4 is a timing diagram of the signals from the serial
31 link of the computer that are sent to the coupler 5; it
32 distinguishes three different types of operation, which
33 correspond to the following three situations:

34 - reading (that is, testing) for the presence of the chip
35 card by the computer without supplying power to the chip card,

1 thus without drawing on the voltage source 11;

2 - normal access to the chip card while supplying it with
3 power, for the purpose of a computer-chip card dialogue;

4 - removal of the chip card during a normal access.

5 A first line of Fig. 4 defines the position of the chip card
6 relative to the coupler and includes a high state corresponding
7 to the case in which the chip card is inserted in the coupler not
8 only so as to be in electrical contact with it but also so as to
9 close the card presence switch 31, and a low state corresponding
10 to the case in which the chip card is absent. The subsequent
11 lines DTR and RST (bistable control circuit 25), CTS (chip card
12 presence state), VCC (card power supply) and RST (card reset)
13 also have two states, a high state and a low state, the first of
14 which corresponds to an active signal. Finally, a last line DCD
15 (low battery state) has alternating shaded and light areas, the
16 latter including the comment "valid" indicating that it is
17 possible to test the state of the battery.

18 In the first type of operation, it may be seen in particular
19 that the computer sends the signal RTS before the signal DTR,
20 which sequence is produced cyclically until the card is detected,
21 which detection causes the transfer of the signal DTR to the
22 signal CTS which indicates the card presence state, but not the
23 activation of the signal VCC, since hypothetically in this case
24 the DTR-then-RTS sequencing is not adhered to: consequently,
25 neither the signal RST nor the signal DCD is activated. During a
26 partial removal of the chip card while the three signals RTS, DTR
27 and CTS are activated, only the latter CTS is deactivated. In
28 order to produce a new DTR, RTS sequencing, the computer first
29 brings these to signals to the low state in reverse order.

30 In order to conform to the intrinsic operating times of the
31 bistable circuit 25, the time interval TDR which separates the
32 two signals RTS and DTR (when the signal RTS is established
33 before the signal DTR is active) is at least equal to a logic
34 gate delay, that is on the order of several microseconds. The
35 time interval TRD1 which separates the deactivation of the signal

1 RTS from that of DTR has a length on the same order.

2 Preferably, the first type of operation will be triggered
3 cyclically in order to detect the insertion of the chip card into
4 the coupler before the chip card is powered up. Moreover, when
5 it is desirable to verify the presence of the chip card at
6 regular intervals during a communication that has already been
7 established (particularly in order to make sure that the user of
8 the coupler is in fact authorized and that the chip card has not
9 been fraudulently replaced by a non-regulation chip card), this
10 first type of operation will be re-triggered as many times as
11 desired.

12 In the second type of operation, the computer sends the
13 signal DTR before RTS in accordance with the requirements of the
14 standard ISO7816-3. Unlike in the preceding type, the activation
15 of the signal DTR while the chip card is fully inserted not only
16 causes the activation of the signal CTS through which the chip
17 card responds to the computer, but also that of the signal VCC,
18 and the activation of the signal RTS causes that of the chip card
19 reset signal RST, which triggers the effective operation of the
20 chip card. It must also be noted that the activation of the
21 signal VCC causes that of the signal CLK, which is not visible in
22 Fig. 4, before that of the signal RST.

23 At the end of the communication between the computer and the
24 chip card, the computer first returns the signal RTS to the low
25 state, which causes the deactivation of the signal RST, then the
26 computer returns the signal DTR to the low state, which causes
27 the deactivation of the signal CLK, not visible in Fig. 4,
28 followed by the voltage drop of the signal VCC. As explained
29 above in reference to Fig. 2, it is the fact that the voltages of
30 the signals RST and CLK are derived from the voltage of the
31 signal VCC which guarantees the sequencing.

32 Thus, it is noted that the sequencing of the signals DTR,
33 RTS defined by the computer, in association with that defined by
34 the coupler, makes it possible to meet the requirements of the
35 standard ISO7816-3 referred to in Fig. 3 relative to the powering

up of the chip card as well as its powering down. Also in order to comply with this standard, the duration TRD3 corresponds to the minimum time for the activation of RST by RTS after a powering up by DTR and the duration TBV corresponds to the wait time after the power up of the coupler, before a reading of the state of the battery.

The "low battery" state is transferred to the signal DCD if a supply voltage VBB, defined below in reference to Fig. 5, falls below the reference voltage. The following behavior is seen from the computer:

if the chip card has been powered up (DTR active) and the battery is good, the signal DCD is at the high level (-12 V on the line)

if the "low battery" signal appears, DTR being active, the signal DCC takes the low value (+ 12 V on the line) with the time-out TBV relative to the signal VCC.

The low battery test can be performed until the end of the communication.

It will be noted that the second type of operation described above can either follow the first type of operation after an effective detection of the presence of the chip card, or be triggered directly.

In the third type of operation, while a computer-chip card dialogue has been established according to the second type described above, a removal of the chip card occurs, causing the deactivation of the signal RST, the signal CLK not visible in Fig. 4, followed by the voltage drop of the signal VCC, even if this deactivation occurs over a shorter time period relative to the second type of operation. The low battery state signal DCD is also deactivated when the chip card is removed.

Advantageously, the only effect of reintroducing the chip card is to reactivate the signal CTS, without allowing a reactivation of the signals VCC, CLK and RST. This makes it possible to avoid the drawbacks caused by a known rebound effect of the card presence switch 31 which can randomly reactivate the

1 power supply signal VCC, and consequently the signals CLK and
2 RST.

3 In this situation, the computer causes the deactivation of
4 the signals DTR then RTS as in the first type of operation, with
5 a time lag TRD2 identical to TRD1. The deactivation of the signal
6 DTR causes that of the signal CTS, which was still at the high
7 state.

8 Fig. 5 is a first partial diagram of the coupler according
9 to the invention and relates to the power supply of the coupler.
10 This coupler comprises, in reference to Fig. 2, the electrical
11 power source 11 which is integrated and constituted, in this
12 case, by a voltage source comprising, for example, an electric
13 generator such as an assembly of two batteries, a photovoltaic
14 cell or a high-capacity capacitor. The voltage of this voltage
15 source 11, VBB, available through a positive terminal of the
16 latter, is sent to the power supply circuit 12 which is of a
17 known type and supplies a standardized voltage VCC of 5 V, which
18 is used in the coupler 5 and is also applied to the chip card 7.
19 The power supply circuit 12 is controlled by a signal applied at
20 13.

21 The voltage VBB is also sent through a "low battery"
22 detection circuit which essentially comprises the comparison
23 circuit 14 of Fig. 2, which compares the voltage VBB to a
24 threshold value obtained from the voltage VCC and supplies a "low
25 battery" alarm signal through an output 15.

26 It is also possible to provide an external power supply that
27 is sent through a jack 16 and is regulated by a regulating
28 circuit 17 whose output is connected to the positive terminal of
29 the voltage source 11 and thus to the regulating circuit 12.

30 This external power supply can also be used to recharge the
31 voltage source 11 when it is rechargeable (battery or very high-
32 capacity capacitor).

33 Fig. 6 is another partial diagram of the coupler according
34 to the invention, relative to the generation of the signals
35 applied to the chip card 7 and the detection of the presence of

1 the latter.

2 The signal RTS drives a first input of a NAND gate 21
3 through an inverter 22; this first input is linked to a first
4 input of another NAND gate 23, which constitutes the blocking
5 circuit of Fig. 2, through another inverter 33. The signal DTR,
6 through two serial inverters 24, drives a second input of the
7 gate 21 and a first input of a bistable toggle 25 of the RS type
8 corresponding to the bistable circuit of Fig. 2 and constituted
9 by two NAND gates, a second input of which receives the output
10 signal from the gate 21. A first output of the toggle 25
11 supplies, at 13, a power supply control signal, which corresponds
12 to the terminal 13 of the power supply circuit 12.

13 The second output of the toggle 25 is sent to a second input
14 of the gate 23 whose output, through an inverter 27, controls an
15 NPN transistor 28 connected between the power supply voltage VCC
16 and the ground, and whose collector supplies, through an inverter
17 29 constituting the interface circuit of Fig. 2, the signal RST.
18 All the gates of the circuit in this figure disposed upstream
19 from the transistor 28 are supplied by the voltage VBB of the
20 voltage source 11 in such a way that the circuit is always on
21 standby and can generate signals in the absence of the power
22 supply signal VCC.

23 An input jack of the port connector 2 which delivers the
24 signal DTR is connected to another jack of this same connector
25 which receives the signal CTS through the card presence switch 31
26 associated with the chip card connector 6 and closed when the
27 chip card 7 is in place in the connector 6.

28 Moreover, a quartz oscillator 32, which constitutes the
29 clock generator of Fig. 2 and is activated by the power supply
30 signal VCC, supplies the clock signal CLK with a delay
31 corresponding to a logic gate delay.

32 It may be seen that the logical circuit of Fig. 6 makes it
33 possible to adhere to the sequencing of the signals VCC, CLK and
34 RST. In effect, due to the fact that during a normal access, the
35 signal DTR is applied first, which is controlled by software

1 installed in the personal computer, the toggle 25 first supplies
2 the power supply control signal 13 which activates the regulating
3 circuit 12. The regulating circuit 12 then supplies the signal
4 VCC. Next, when the signal RTS appears, the toggle 25 changes
5 state and actuates the generation of the signal RST, which can
6 only appear when the signal VCC has been established.

7 The clock signal CLK can only be produced after the
8 establishment of the power supply signal VCC because the quartz
9 oscillator 32 is controlled by the power supply signal VCC.

10 During a card presence read cycle (see Fig. 4), the signals
11 DTR and RTS are applied in the reverse order and the toggle does
12 not actuate the generation of the signals VCC, CLK and RST; in
13 particular, the voltage source 11 remains on standby. The
14 presence of the chip card closes the card presence switch 31,
15 which sends the card presence information to the computer through
16 the signal CTS; this card presence detection operation occurs
17 without drawing on the voltage source, since the power supply
18 circuit 12 is not activated.

19 The chip card presence information supplied by the signal
20 CTS makes it possible to manage the presence of the chip card
21 through the personal computer in real time; this makes it
22 possible, in particular, to detect the removal of the chip card
23 during the data exchange in order to perform a session sign-off
24 (end of task).

25 Fig. 7 is another partial diagram of the coupler, whose
26 chief function is to transfer data signals between the computer
27 and the chip card. The interface circuit 41 of Fig. 2 performs a
28 conversion of the signals TX, RX and DCD that it receives or
29 produces. An NPN transistor 42 is provided, the collector of
30 which is connected, through two series resistors 45, 46, to the
31 voltage VCC, and the emitter of which is grounded. The base of
32 the transistor 42 is driven by the signal TX issuing from the
33 interface circuit 41, while its collector is connected to the I/O
34 terminal of the chip card connector. This collector is connected
35 to an inverter of the interface circuit 41 which outputs the

1 signal RX.

2 The output 15 of the comparison circuit 14 of Fig. 5 drives
3 an inverter 44 connected at its output to an inverter of the
4 interface circuit 41 which outputs the "low battery" alarm signal
5 DCD.

6 The interface circuit 41 and the inverter 44 are supplied by
7 the voltage VCC.

8 The control signal 13 of the power supply circuit 12 of Fig.
9 5 controls a MOSFET field effect transistor 43 directly polarized
10 with a positive voltage, which makes it possible to accelerate
11 the drop of the power supply signal VCC and consequently of the
12 signals CLK, RST and I/O during the powering down, in order to
13 obtain a 5 V to 0.4 V drop time that is shorter than the sliding
14 time of the contacts of the card, so as to comply with the
15 standard ISO 7816-3, which specifies the need to have a voltage
16 lower than 0.4 V at the moment the contacts are disconnected.

17 In operation, the interface circuit 41 ensures a
18 multiplexing/demultiplexing between the signals TX, RX on one
19 hand and I/O on the other hand. It is noted that the "low
20 battery" signal DCD more generally constitutes an alarm signal
21 which can detect other abnormal conditions such as a defective
22 chip card producing a short circuit of the contacts.

23 The utilization of an integrated voltage source makes it
24 possible to obtain the signals to be applied to the chip card in
25 complete safety, without requiring a power supply from the
26 personal computer, which is important in the case of portable
27 computers.

28 Moreover, the coupler according to the invention has a
29 simple design, which makes it possible to obtain a low cost price
30 and a reduced size; thus, it is possible to produce an interface
31 device whose dimensions are on the order of those of a chip card.

32 In the example described above, certain particular control
33 signals RTS, DTR, CTS and DCD from the serial link of the data
34 exchange device were selected to cooperate with the coupler, and
35 each of them was assigned a particular function specific to the

1 operation of a portable data medium. It is clear that the
2 invention is not limited to this particular selection. More
3 generally, any signal from the serial link which, in accordance
4 with the communication protocol of this link, issues from the
5 data exchange device, could play the role of any of the signals
6 RTS, DTR or DCD; likewise, any signal from the serial link which,
7 in accordance with the communication protocol of this link,
8 returns to the data exchange device, could play the role of the
9 signal CTS (for example, for an RS232 link, the signal DSR Data-
10 Set-Ready).

11 Moreover, while the coupler described above is designed to
12 carry out a serial data signal transmission, it is clear that the
13 invention also applies to a parallel data signal transmission, in
14 which case the data exchange device and the portable data medium
15 comprise appropriate data interface means.

16 On the other hand, while the coupler described above was
17 described as a device physically separate from the data exchange
18 device and the portable data medium, it could naturally be
19 integrated into either of these devices. In such as case, the
20 connecting means between the device in question and the coupler,
21 such as a connector or a cable described in relation to Fig. 1,
22 could possibly be eliminated.

23 Moreover, in the second and third types of operation of Fig.
24 4, and according to a less preferred embodiment, no signal CTS is
25 used. In effect, the powering up of the chip card in the second
26 type of operation, and the powering down of the chip card in the
27 third type of operation, do not require the management of this
28 signal in order to comply with the standard ISO7816-3.

CLAIMS

1
2
3 1. A coupler for managing communication between a portable
4 data medium (7) and a data exchange device (1), which
5 communication uses, on the data exchange device end, at least one
6 data transmission signal and two control signals delivered by the
7 data exchange device in one of two first and second predetermined
8 input sequences, and on the data medium end, at least one data
9 medium power supply signal, one data medium reset signal, and one
10 data transmission signal, characterized in that:

11 - it comprises bistable control means (25) input-activated
12 by at least said two control signals delivered by the data
13 exchange device, and designed to output at least said data medium
14 power supply signal and said data medium reset signal, in one of
15 two first and second predetermined output sequences, which is a
16 function of said input sequence,

17 - said first input sequence alone is capable of generating a
18 first output sequence successively comprising said data medium
19 power supply signal and said data medium reset signal, which
20 allows the data exchange device to enter into communication with
21 the portable data medium.

1 2. A coupler according to claim 1, characterized in that
2 it comprises means (31) for detecting the presence of the
3 portable data medium, designed to deliver to the data exchange
4 device a signal of the presence of the medium when the portable
5 data medium is cooperating with the coupler, upon reception of a
6 first of said control signals, the sending of said second input
7 sequence by the data exchange device allowing it to detect the
8 presence of the portable data medium without the latter's being
9 supplied with power.

1 3. A coupler according to claim 1, which comprises means
2 for generating signals (29, 32) designed to:

3 - receive said power supply signal having a predetermined



4 electrical level; and

5 - send to the portable data medium said reset signal and a
6 clock signal from said power supply signal, in such a way that
7 they have an electrical level lower than said predetermined
8 electrical level of the power supply signal.

1 4. A coupler according to claim 3, in which said signal
2 generating means (29, 32, 41) are designed to receive said data
3 transmission signal delivered by the data exchange device and to
4 deliver to the portable data medium said data transmission signal
5 from said power supply signal, in such a way that it has an
6 electrical level lower than said predetermined electrical level
7 of the power supply signal.

1 5. A coupler according to claim 1, characterized in that:
2 - the portable data medium cooperates with the coupler
3 through respective sliding contact means (6); and
4 - said bistable control means (25) comprise attenuation
5 means (43) for the power supply signal designed to attenuate an
6 electrical level of the power supply signal during communication
7 until a predetermined threshold level is reached, before said
8 respective sliding contact means cease to be in mutual
9 cooperation.

1 6. A coupler according to claim 1, in which:
2 - a power source (11, 12, 23, 29) is provided and designed
3 to deliver, upon reception of an activation signal received from
4 the bistable control means (25), said data medium power supply
5 signal and said data medium reset signal; and
6 - the bistable control means are designed to deliver to the
7 power source said activation signal, upon reception of said first
8 input sequence.

1 7. A data exchange device designed to manage communication
2 with a portable data medium (7) and comprising for this purpose



3 data exchange means (1) and coupling means (5), which
4 communication uses, on the data exchange means end, at least one
5 data transmission signal and two control signals delivered by the
6 data exchange means (1) in one of two first and second
7 predetermined input sequences, and on the data medium end, at
8 least one data medium power supply signal, one data medium reset
9 signal, and one data transmission signal, characterized in that
10 the coupling means (5):

11 - comprise bistable control means (25) input-activated by at
12 least one of said two control signals delivered by the data
13 exchange means (1), and designed to output at least said data
14 medium power supply signal and said data medium reset signal in
15 one of two first and second predetermined output sequences, which
16 is a function of said input sequence,

17 - are designed such that said first input sequence alone is
18 capable of generating a first output sequence successively
19 comprising said data medium power supply signal and said data
20 medium reset signal, which allow the data exchange means (1) to
21 enter into communication with the portable data medium;

22 - comprise means (31) for detecting the presence of the
23 portable data medium, designed to deliver to the data exchange
24 means (1) a signal of the presence of the medium when the
25 portable data medium is cooperating with the coupling means (5),
26 upon reception of a first of said control signals, the sending of
27 said second input sequence by the data exchange means (1)
28 allowing it to detect the presence of the portable data medium
29 without the latter's being supplied with power;; and

30 the data exchange means (1) are designed to cyclically send
31 to the coupling means (5), before a communication with the
32 portable data medium, said second input signal until they receive
33 said signal of the presence of the portable data medium.

34 8. A data exchange device according to claim 7, in which
35 the data exchange means (1) are designed to send, once they have
36 detected the presence of the portable data medium, said first
37 input sequence.

