

MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE AND BONDED WAFER

TECHNICAL FIELD

5 [0001] The present disclosure relates to a manufacturing method for a semiconductor device and a bonded wafer.

BACKGROUND ART

[0002] In order to reduce costs of semiconductor devices, technology for effectively using a high-cost monocrystalline wafer has hitherto been proposed. For example,
10 Patent Document 1 proposes a method of slicing a wafer at the time of a thinning process in a device process and reusing a divided wafer on which a device is not formed.

PRIOR ART DOCUMENTS

PATENT DOCUMENT

15 [0003] Patent Document 1: Japanese Patent Application Laid-Open No. 2019-50362

SUMMARY

PROBLEM TO BE SOLVED BY THE INVENTION

[0004] In the method disclosed in Patent Document 1, in order to reduce cracking in
20 the divided wafer to be reused, it is necessary to form a thick epitaxial film as a buffer layer, which is unrelated to device operation, on the divided wafer, and cause the divided wafer to have a thickness equal to that of the original pre-divided wafer. The formation of the thick epitaxial film is disadvantageous in terms of productivity. In contrast, when a thin epitaxial film is formed, there is a problem in higher risks of cracking when the
25 divided wafer is reused.

[0005] The present disclosure is made in order to solve the problem described above, and has an object to enhance productivity and reduce cracking in a wafer in manufacture of a semiconductor device reusing the wafer.

MEANS TO SOLVE THE PROBLEM

5 [0006] A manufacturing method for a semiconductor device of the present disclosure includes the steps of: (a) dividing each of a plurality of first wafers in a thickness direction to thereby obtain at least one first divided wafer not including a device structure from each of the first wafers; (b) bonding a plurality of the first divided wafers obtained from different first wafers to obtain a first bonded wafer being a bonded wafer; and (c)
10 forming the device structure on a front surface of the first bonded wafer.

EFFECTS OF THE INVENTION

[0007] According to the manufacturing method for the semiconductor device of the present disclosure, the device structure is formed on the bonded wafer obtained by bonding the divided wafers. Therefore, the bonded wafer having a sufficient thickness
15 in consideration of cracking can be formed and the wafer can be reused at a lower cost than that when an epitaxial film is formed on each divided wafer. These and other objects, features, aspects and advantages of the present disclosure will become more apparent from the following detailed description of the present disclosure when taken in conjunction with the accompanying drawings.

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BRIEF DESCRIPTION OF DRAWINGS

[0008] [FIG. 1] is a diagram illustrating a basic process of a manufacturing method for a semiconductor device according to a first embodiment.

[FIG. 2] is a flowchart illustrating the manufacturing method for the
25 semiconductor device according to the first embodiment.

[FIG. 3] is a diagram illustrating the manufacturing method for the semiconductor device according to the first embodiment when a thickness of a bonded wafer is 500 μm .

[FIG. 4] is a diagram illustrating the manufacturing method for the
5 semiconductor device according to the first embodiment when the thickness of the bonded wafer is 500 μm .

[FIG. 5] is a diagram illustrating the manufacturing method for the semiconductor device according to the first embodiment when a thickness of a bonded wafer is 350 μm .

10 [FIG. 6] is a diagram illustrating the manufacturing method for the semiconductor device according to the first embodiment when the thickness of the bonded wafer is 350 μm .

[FIG. 7] is a diagram illustrating a depth of a bonded surface in a bonded wafer made up of two divided wafers.

15 [FIG. 8] is a diagram illustrating a depth of a bonded surface in a bonded wafer made up of three divided wafers.

[FIG. 9] is a diagram illustrating patterns of wafer division timings in the manufacturing method for the semiconductor device according to the first embodiment.

[FIG. 10] is a diagram illustrating a basic process when a SiC wafer is divided
20 before formation of an epitaxial film in the manufacturing method for the semiconductor device according to the first embodiment.

[FIG. 11] is a diagram illustrating a basic process of the manufacturing method for the semiconductor device according to a second embodiment.

[FIG. 12] is a diagram illustrating a basic process of the manufacturing method
25 for the semiconductor device according to a modification of the second embodiment.

[FIG. 13] is a diagram illustrating a basic process of the manufacturing method for the semiconductor device according to a third embodiment.

[FIG. 14] is a diagram illustrating a basic process of the manufacturing method for the semiconductor device according to a modification of the third embodiment.

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DESCRIPTION OF EMBODIMENTS

[0009] <A. First Embodiment>

<A-1. Basic Process>

FIG. 1 is a schematic diagram illustrating a basic process of a manufacturing method for a semiconductor device according to the present embodiment. FIG. 2 is a flowchart of the manufacturing method for the semiconductor device according to the present embodiment. With reference to FIG. 1 and FIG. 2, the manufacturing method for the semiconductor device according to the present embodiment will be described below.

15 [0010] First, in Step S101, an epitaxial film 11 is formed on a monocrystalline SiC wafer 10, and a front surface structure (hereinafter a device structure) 12 of the device is formed on the epitaxial film 11. The formation of the device structure 12 includes ion implantation and formation of a front surface electrode. The device structure 12 is a SiC power device structure, for example. When a GaN wafer or a gallium oxide wafer is used instead of the SiC wafer, the device structure 12 is a GaN high-frequency device structure, a GaN power device structure, or a gallium oxide power device structure, for example. The GaN high-frequency device structure, the GaN power device structure, or the gallium oxide power device structure may be formed on the SiC wafer. The SiC wafer 10 on which the epitaxial film 11 and the device structure 12 are formed is referred to as a SiC wafer 13.

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[0011] In Step S101, a SiC wafer 17, which is similar to the SiC wafer 13, is further formed. In other words, an epitaxial film 15 is formed on a monocrystalline SiC wafer 14, and a device structure 16 is formed on the epitaxial film 15. The SiC wafer 14 on which the epitaxial film 15 and the device structure 16 are formed is referred to as the SiC wafer 17. The SiC wafers 13 and 17 are also referred to as first wafers. Here, the SiC wafers 10 and 14 may be a bonded wafer, which is formed by bonding a plurality of SiC wafers. Each of the SiC wafers 10 and 14 has an N-type or P-type conductivity type or semi-insulating property.

[0012] Next, in Step S102, the SiC wafer 13 is divided into a device-included wafer 19 including the device structure 12 and a divided wafer 20 not including the device structure 12. The device-included wafer 19 includes a SiC wafer 18 divided from the SiC wafer 10, the epitaxial film 11 on the SiC wafer 18, and the device structure 12 on the epitaxial film 11.

[0013] In Step S102, the SiC wafer 17 is also divided similarly to the SiC wafer 13. In other words, the SiC wafer 17 is divided into a device-included wafer 22 including the device structure 16 and a divided wafer 23 not including the device structure 16. The device-included wafer 22 includes a SiC wafer 21 divided from the SiC wafer 14, the epitaxial film 15 on the SiC wafer 21, and the device structure 16 on the epitaxial film 15. The device-included wafers 19 and 22 are also referred to as first device-included wafers, and the divided wafers 20 and 23 are also referred to as first divided wafers. Note that laser slicing technology or the like is used for the division of the SiC wafers 13 and 17 in the steps.

[0014] Subsequently, in Step S103, back surfaces being surfaces of the device-included wafers 19 and 22 on the opposite side of the device structures 12 and 16 are treated. First, damaged layers of the device-included wafers 19 and 22 on the back surface side

that are damaged in laser slicing are removed through grinding, polishing, or the like, and the device-included wafers 19 and 22 are adjusted to a desired board thickness. Subsequently, on the back surfaces of the device-included wafers 19 and 22, a regular back surface process, such as formation of a back surface electrode (not illustrated), is performed.

[0015] Next, in Step S104, front surface treatment on the divided wafers 20 and 23 is performed. The divided wafers 20 and 23 also include damaged layers that are damaged in laser slicing, and accordingly the damaged layers are removed through grinding, polishing, or the like, and the divided wafers 20 and 23 are further adjusted to a desired board thickness. In consideration of depth of a bonded surface of the bonded wafer to be described later, the thickness of each of the divided wafers 20 and 23 is desirably 50 μm or more, more desirably 80 μm or more, and most desirably 100 μm or more. When the board thickness of each of the divided wafers 20 and 23 is adjusted, back surface-side treatment, for example, grinding, polishing, or the like, on the divided wafers 20 and 23 may be performed as necessary. Performing the back surface-side treatment enables removal of scratches and the like formed during the device process, in addition to the adjustment of the board thickness. As a result, a high-quality bonded wafer can be obtained in later Step S105. Here, the high-quality bonded wafer refers to a bonded wafer with enhanced damage reduction, deflection reduction, flatness, or the like. It can also be said that the back surface-side treatment on the divided wafers 20 and 23 is a process having certain effects in forming the device-included wafers through division and bonding.

[0016] Subsequently, in Step S105, the divided wafers 20 and 23 are bonded. A wafer obtained by bonding the divided wafers 20 and 23 is referred to as a bonded wafer 24. The bonded wafer 24 is also referred to as a first bonded wafer. In this case, front

surface treatment may be performed on the bonded surface of the divided wafers 20 and 23 through grinding, polishing, CMP, or the like. In order to reduce deflection of the bonded wafer 24, deflection or a front surface state of the divided wafers 20 and 23 may be examined, and depending on its results, a combination of the divided wafers 20 and 23 to be bonded may be determined. In this manner, a high-quality bonded wafer can be obtained. Here, the two divided wafers 20 and 23 may be formed simultaneously or formed separately. In other words, the two divided wafers 20 and 23 may be formed simultaneously or in sequence by using different pieces of treatment equipment, or may be formed in sequence by using one piece of treatment equipment, for example. This enables flexible manufacturing, and enables enhancement of productivity of divided wafers. Note that, although the description here concerns bonding of two divided wafers 20 and 23, the bonded wafer 24 may be formed by bonding any number of, e.g., three or more, divided wafers.

[0017] The divided wafers 20 and 23 are bonded through room temperature bonding, for example. According to room temperature bonding, a clean interface can be obtained, without a bonded interface including a metal layer or the like. In addition, according to room temperature bonding, an amorphous layer is generated in the bonded interface. After bonding of the divided wafers 20 and 23, the bonded wafer 24 may be treated to a desired board thickness through grinding, polishing, CMP, or the like. In the process, the bonded wafer 24 has a thickness similar to that of a commonly-used SiC wafer, and therefore the divided wafers 20 and 23 can be reused at a lower cost without risks of cracking in comparison to when a thick epitaxial film is formed on a thin SiC wafer to maintain overall strength.

[0018] Before bonding, each of the divided wafers 20 and 23 may be subjected to bevel treatment of removing a pointed portion at an intersection between a peripheral surface

and a cross-sectional surface, i.e., a corner portion of each of the divided wafers 20 and 23. In this case, the shape of an end portion of the bonded wafer 24 is a shape similar to "3" in a cross-sectional view, or a zigzag shape having five to seven inflection points. When the shapes of end portions of the divided wafers 20 and 23 are curved, the shape of the end portion of the bonded wafer 24 is a shape similar to "3" through bonding. When the shapes of the end portions of the divided wafers 20 and 23 are triangular shapes, one inflection point overlaps through bonding, and the shape of the end portion of the bonded wafer 24 is a zigzag shape having five inflection points. When the shapes of the end portions of the divided wafers 20 and 23 are trapezoidal shapes, one inflection point overlaps through bonding, and the shape of the end portion of the bonded wafer 24 is a zigzag shape having seven inflection points. In this case, bevel treatment after bonding is unnecessary and the amount of cutting is small, and thus the area of the bonded wafer 24 can be increased.

[0019] Alternatively, the bevel treatment may not be performed on the divided wafers 20 and 23 before bonding, and the bevel treatment may be performed on the bonded wafer 24. In this case, the beveled shape of the bonded wafer is a curved shape similar to ")") in a cross-sectional view or a trapezoidal shape, as with a regular wafer not being the bonded wafer. In this case, in comparison to the shape similar to "3", there are higher effects of chipping prevention in the bonded wafer 24. Further, the bevel treatment may be performed on both of the divided wafers 20 and 23 before bonding and the bonded wafer 24 after bonding. In this case, both of effects of chipping prevention at the time of treatment and chipping prevention in the bonded wafer 24 can be obtained.

[0020] Next, in Step S106, an epitaxial film 25 is formed on the bonded wafer 24, and a device structure 26 is further formed on the epitaxial film 25. A wafer formed in this manner is referred to as a bonded wafer 27.

[0021] Subsequently, in Step S107, the bonded wafer 27 is divided in a thickness direction, and a device-included wafer 29 including the device structure 26 and a divided wafer 30 not including the device structure 26 are obtained. The device-included wafer 29 is also referred to as a second device-included wafer, and the divided wafer 30 is also referred to as a second divided wafer. The device-included wafer 29 has a structure in which the epitaxial film 25 is formed on the SiC wafer 10 and the device structure 26 is formed on the epitaxial film 25. The process is similar to Step S102.

[0022] Note that, although the bonded wafer 27 includes a bonded surface of the two divided wafers 20 and 23, it is desirable that the bonded surface be not included in the device-included wafer 29. In this manner, variation of device characteristics due to the bonded surface can be avoided in the device-included wafer 29. Here, it can also be said that, when the bonded wafer 27 is formed through room temperature bonding, an amorphous layer is generated in the bonded interface, and thus it is desirable that the amorphous layer be not included in a SiC wafer 28 of the device-included wafer 29.

Note that, even if the device-included wafer 29 includes the bonded surface of the two divided wafers 20 and 23, it may not present a problem, considering the type of the device structure, characteristics required for the device, or the like. In this case, it is not necessary to arrange not to include the bonded surface when obtaining the device-included wafer 29, and the degree of freedom in process adjustment or thickness adjustment in the wafer division process can be enhanced.

[0023] The device-included wafer 29 obtained in Step S107 is subjected to the back surface treatment (not illustrated) of Step S103 again. Further, the divided wafer 30 obtained in Step S107 may be subjected to the treatment of Step S104 and the following steps again. Subsequently, the divided wafer 30 is bonded to another divided wafer, and can thereby be used to create another device-included wafer. In other words, the

treatment from Step S105 to Step S107 is repeated at least once, with the divided wafer 30 as the second divided wafer being used as a new first divided wafer.

[0024] In this manner, three device-included wafers 19, 22, and 29 are obtained from two SiC wafers 13 and 17. By repeating the treatment described above, a larger number of device-included wafers than the number of original SiC wafers can be obtained. Further, based on a SiC wafer having a less amount of various inner defects, i.e., a so-called high-quality wafer, a plurality of device-included wafers can be formed, and a large number of high-quality devices can be efficiently produced.

[0025] The bonded wafer obtained by bonding a plurality of divided wafers may have different amounts of various defects, such as crystalline defects, for example, threading dislocation, across the bonded surface, depending on a state of each of the divided wafers. In this case, densities of crystalline defects present in a surface layer may be different or densities of crystalline defects present near a bonded interface may be different between a device structure formation surface side and its opposite surface side of the bonded wafer. Moreover, threading dislocations, which are continuous from the front surface to the back surface in a regular wafer, are discontinuous in the bonded interface in the bonded wafer. However, even when the amounts of various defects are different between a plurality of divided wafers, influence given thereby to the device process or device characteristics can be ignored. Here, by selecting the device structure or the divided wafer as appropriate, the influence given to the device process or the device characteristics by the discontinuity of the defects described above or the like can be further reduced. In addition, by arranging not to include the bonded surface in the device-included wafer, the influence given to the device characteristics by the discontinuity of the defects described above or the like can be eliminated.

[0026] <A-2. Actual Use>

FIG. 3 to FIG. 6 are diagrams illustrating flows when the basic process illustrated in FIG. 1 is put into actual use. FIG. 3 and FIG. 4 illustrate flow examples in the SiC wafer having a thickness of 500 μm , and FIG. 5 and FIG. 6 illustrate flow examples in the SiC wafer having a thickness of 350 μm .

5 [0027] FIG. 3 and FIG. 5 illustrate formation of a bonded wafer E1 from SiC wafers A3 and B3. FIG. 4 and FIG. 6 illustrate formation of a bonded wafer G1 from the bonded wafer E1 and a SiC wafer F3. In FIG. 3 to FIG. 6, a number indicated within a wafer indicates a thickness (μm) of the wafer. Further, a number in parentheses above or below a wafer indicates a thickness (μm) of a removed wafer. Further, a broken line
10 within a wafer indicates a bonded surface, and a number in square brackets beside a bonded surface indicates a depth (μm) of the bonded surface, i.e., a depth (μm) from a front surface to the bonded surface of the bonded wafer. Note that the thickness and the depth of each layer illustrated in these figures are an example, and can be changed as appropriate.

15 [0028] As illustrated in FIG. 3, SiC wafers A3 and B3 are prepared. The thickness of each of the SiC wafers A3 and B3 including an epitaxial film is 510 μm . The SiC wafer A3 is obtained by forming a device structure A2 on the front surface of a SiC wafer A1. Further, the SiC wafer B3 is obtained by forming a device structure B2 on the front surface of a SiC wafer B1. Note that, in description of FIG. 3 to FIG. 6, the device
20 structure includes an epitaxial film. For example, more specifically, the device structure A2 includes an epitaxial film formed on the SiC wafer A1 and a device structure formed on the epitaxial film. The same applies to other device structures in the description of FIG. 3 to FIG. 6.

[0029] The SiC wafer A3 is divided into a device-included wafer A4 including the
25 device structure A2 and a divided wafer A12 not including the device structure A2. The

device-included wafer A4 includes a SiC wafer A11 and the device structure A2 on the SiC wafer A11. The back surface of the SiC wafer A11 is removed by 50 μm , causing the thickness of the SiC wafer A11 to be 100 μm . In the divided wafer A12, the front surface is removed by 50 μm and the back surface is removed by 10 μm , causing the thickness to be 300 μm .

[0030] In the divided wafer A12, the back surface is further removed by 25 μm , causing the thickness to be 275 μm .

[0031] The SiC wafer B3 is divided into a device-included wafer B4 including the device structure B2 and a divided wafer B12 not including the device structure B2. The device-included wafer B4 includes a SiC wafer B11 and the device structure B2 on the SiC wafer B11. In the SiC wafer B11, the back surface is removed by 50 μm , causing the thickness to be 100 μm . In the divided wafer B12, the front surface is removed by 50 μm and the back surface is removed by 10 μm , causing the thickness to be 300 μm .

[0032] In the divided wafer B12, the front surface is further removed by 25 μm , causing the thickness to be 275 μm .

[0033] Next, the divided wafers A12 and B12 are bonded, and a bonded wafer C1 having a thickness of 550 μm is obtained. Here, the depth of the bonded surface of the bonded wafer C1 is 275 μm .

[0034] Subsequently, the thickness of the front surface of the bonded wafer C1 is removed by 50 μm , causing the thickness of the bonded wafer C1 to be 500 μm . Here, the depth of the bonded surface of the bonded wafer C1 is 225 μm .

[0035] Next, a device structure C2 is formed on the bonded wafer C1. A wafer made up of the bonded wafer C1 and the device structure C2 is referred to as a bonded wafer C3. The thickness of the bonded wafer C3 is 510 μm , and the depth of the bonded surface in the bonded wafer C3 is 235 μm .

[0036] Subsequently, the bonded wafer C3 is divided into a device-included wafer C4 including the device structure C2 and a divided wafer C5 not including the device structure C2. The device-included wafer C4 includes a SiC wafer A121 being a part of the divided wafer A12 and the device structure C2 on the SiC wafer A121. The bonded
 5 surface in the bonded wafer C3 is not included in the device-included wafer C4. The back surface of the SiC wafer A121 is removed by 50 μm , causing the thickness of the device-included wafer C4 to be 100 μm . The divided wafer C5 includes a SiC wafer A122 being a part of the divided wafer A12 and the divided wafer B12. In the divided wafer C5, the front surface is removed by 50 μm and the back surface is removed by 10
 10 μm , causing the thickness to be 300 μm . Here, the depth of the bonded surface in the divided wafer C5 is 35 μm .

[0037] In the divided wafer C5, the back surface is further removed by 25 μm , causing the thickness to be 275 μm .

[0038] A SiC wafer D3 is prepared. The SiC wafer D3 is obtained by forming a
 15 device structure D2 on the front surface of a SiC wafer D1.

[0039] The SiC wafer D3 is divided into a device-included wafer D4 including the device structure D2 and a divided wafer D12 not including the device structure D2. The device-included wafer D4 includes a SiC wafer D11 and the device structure D2 on the SiC wafer D11. The back surface of the SiC wafer D11 is removed by 50 μm , causing
 20 the thickness of the SiC wafer D11 to be 100 μm . In the divided wafer D12, the front surface is removed by 50 μm and the back surface is removed by 10 μm , causing the thickness to be 300 μm .

[0040] In the divided wafer D12, the front surface is further removed by 25 μm , causing the thickness to be 275 μm .

25 [0041] Next, the divided wafers C5 and D12 are bonded, and a bonded wafer E1

having a thickness of 550 μm is obtained. In this case, the bonded wafer E1 includes a first bonded surface being a bonded surface between the SiC wafer A122 and the divided wafer B12 and a second bonded surface being a bonded surface between the divided wafer B12 and the divided wafer D12. The depth of the first bonded surface is 35 μm ,
 5 and the depth of the second bonded surface is 275 μm .

[0042] Subsequently, as illustrated in FIG. 4, the front surface of the bonded wafer E1 is removed by 50 μm . This removes the SiC wafer A122 from the bonded wafer E1, causing the thickness of the bonded wafer E1 to be 500 μm . Here, the depth of the bonded surface in the bonded wafer E1 is 225 μm .

10 [0043] Next, a device structure E2 is formed on the front surface of the bonded wafer E1. A SiC wafer made up of the bonded wafer E1 and the device structure E2 on the bonded wafer E1 is referred to as a bonded wafer E3. The thickness of the bonded wafer E3 is 510 μm , and the depth of the bonded surface in the bonded wafer E3 is 235 μm .

[0044] Subsequently, the bonded wafer E3 is divided into a device-included wafer E4
 15 including the device structure E2 and a divided wafer E5 not including the device structure E2. The device-included wafer E4 includes a SiC wafer B121 being a part of the divided wafer B12 and the device structure E2 on the SiC wafer B121. The divided wafer E5 includes the divided wafer D12 and a SiC wafer B122 being a part of the divided wafer B12. In the divided wafer E5, the front surface is removed by 50 μm and
 20 the back surface is removed by 10 μm , causing the thickness to be 300 μm .

[0045] In the divided wafer D12, the back surface is further removed by 25 μm , causing the thickness to be 275 μm .

[0046] A SiC wafer F3 is prepared. The SiC wafer F3 is obtained by forming a device structure F2 on the front surface of a SiC wafer F1.

25 [0047] The SiC wafer F3 is divided into a device-included wafer F4 including the

device structure F2 and a divided wafer F12 not including the device structure F2. The device-included wafer F4 includes a SiC wafer F11 and the device structure F2 on the SiC wafer F11. The back surface of the SiC wafer F11 is removed by 50 μm , causing the thickness of the SiC wafer F11 to be 100 μm . In the divided wafer F12, the front surface is removed by 50 μm and the back surface is removed by 10 μm , causing the thickness to be 300 μm .

[0048] In the divided wafer F12, the front surface is further removed by 25 μm , causing the thickness to be 275 μm .

[0049] Next, the divided wafers E5 and F12 are bonded, and a bonded wafer G1 having a thickness of 550 μm is obtained. In this case, the bonded wafer G1 includes a first bonded surface being a bonded surface between the SiC wafer B122 and the divided wafer D12 and a second bonded surface being a bonded surface between the divided wafer D12 and the divided wafer F12. The depth of the first bonded surface is 35 μm , and the depth of the second bonded surface is 275 μm .

[0050] Subsequently, the front surface of the bonded wafer G1 is removed by 50 μm . This removes the SiC wafer B122 from the bonded wafer G1, causing the thickness of the bonded wafer G1 to be 500 μm . The depth of the bonded surface in the bonded wafer G1 is 225 μm .

[0051] Although FIG. 3 and FIG. 4 describe up to formation of the bonded wafer G1, a device structure may be formed on the bonded wafer G1 and then divided wafers may be further taken out from the bonded wafer G1. As described above, by repeating formation of a bonded wafer through bonding of divided wafers and a device structure on the bonded wafer and division of the bonded wafer, creation of device-included wafers using the divided wafers can be repeated.

[0052] Three device-included wafers A4, B4, and C4 are obtained from two SiC

wafers A3 and B3. Further, five device-included wafers A4, B4, C4, D4, and E4 are obtained from three SiC wafers A3, B3, and D3. In other words, $(2n-1)$ device-included wafers are obtained from n SiC wafers 10. In this manner, the device-included wafers can be formed with a reduced number of SiC wafers to be used, and effects of reducing costs can be obtained.

[0053] In the description of the examples of FIG. 3 and FIG. 4, each of the SiC wafers A3, B3, D3, and F3 is obtained by forming an epitaxial film having a thickness of 10 μm on a SiC wafer having a thickness of 500 μm . However, the thickness of each layer constituting each of the SiC wafers A3, B3, D3, and F3 is not limited to this, and may be changed as appropriate depending on desired device characteristics or wafer thickness. For example, a case in which the wafer thickness is 350 μm and the epitaxial film thickness is 10 μm is illustrated in FIG. 5 and FIG. 6.

[0054] In the examples of FIG. 3 and FIG. 4, the thickness of each of the device-included wafers A4, C4, and E4 is 100 μm , but is not limited to this and is selected as appropriate depending on device characteristics. Further, the back surface of each of the SiC wafers A11, A121, and B121 is removed by 50 μm , but this is not restrictive. In order to remove damaged layers at the time of division and cause each of the device-included wafers A4, C4, and E4 to have a desired thickness, a removal amount of the back surface of each of the SiC wafers A11, A121, and B121 may be selected as appropriate from 10 μm to 100 μm , for example.

[0055] In the examples of FIG. 3 and FIG. 4, the thickness of each of the divided wafers A12, C5, and E5 is 275 μm , but this is not restrictive. The thickness of each of the divided wafers A12, C5, and E5 may be 50 μm or more, desirably 80 μm or more, and most desirably 100 μm or more. This enables prevention of cracking in divided wafers, and enables such usage that a bonded surface is not included in each of the

device-included wafers C4 and E4. When a bonded surface is not included the device-included wafer, influence given to device characteristics by the bonded surface can be eliminated, and characteristics equivalent to those of a device using a regular wafer not using a bonding means can be obtained.

5 [0056] The front surface of each of the divided wafers A12, C5, and E5 is removed by 50 μm , but this is not restrictive. In order to remove damaged layers at the time of division or cause each of the divided wafers A12, C5, and E5 to have a desired thickness, a removal amount of the front surface of each of the divided wafers A12, C5, and E5 may be selected as appropriate from 10 μm to 100 μm , for example.

10 [0057] In the examples of FIG. 3 and FIG. 4, treatment on the back surface of each of the divided wafers A12, C5, and E5 is performed two separate times, but this is not restrictive, and the treatment may be performed at a time or may be performed separately in a plurality of, e.g., two or more, processes. When the treatment is performed at a time, effects of reducing the number of processes can be obtained. When the treatment is
15 separated into a plurality of processes, enhancement in quality after removal can be expected.

[0058] In the examples of FIG. 3 and FIG. 4, the back surface of each of the divided wafers A12, C5, and E5 is removed by a total of 35 μm in two processes. However, the removal amount of the back surface of each of the divided wafers A12, C5, and E5 is not
20 limited to this, and can be selected as appropriate so that each of the divided wafers A12, C5, and E5 has a desired thickness. Further, when each of the divided wafers A12, C5, and E5 can be caused to have a desired thickness through treatment on the front surface, the treatment on the back surface need not be performed. When the back surface of each of the divided wafers A12, C5, and E5 is removed, laser printing performed on a regular
25 wafer can be removed, and thus influence of laser printing at the time of bonding, i.e.,

damage or unevenness on the bonded surface, can be eliminated, and quality of the bonded wafer can be enhanced. The effects are observed when a total removal amount of the back surface of each divided wafer is 1 μm or more, and are remarkably obtained when the total removal amount is 30 μm or more in particular.

5 [0059] In the examples of FIG. 3 and FIG. 4, total removal amounts of the front surface of each of the divided wafers A12, C5, and E5 and each of the divided wafers B12, D12, and F12 are different, but may be the same. When the total removal amounts are the same, treatment processes for these divided wafers can be integrated, and therefore this is superior in terms of productivity. Further, in the examples of FIG. 3 and FIG. 4,
10 total removal amounts of the back surface of each of the divided wafers A12, C5, and E5 and B12, D12, and F12 are different, but may be the same. When the total removal amounts are the same, treatment processes for these divided wafers can be integrated, and therefore this is superior in terms of productivity.

[0060] In the examples of FIG. 3 and FIG. 4, two divided wafers each having a
15 thickness of 275 μm are bonded to form each of the bonded wafers C1, E1, and G1 having a thickness of 550 μm . However, the thickness of each divided wafer is not limited to this, and can be changed as appropriate. Further, divided wafers having different thicknesses may be bonded, and for example, the thicknesses of the divided wafer A12 and the divided wafer B12 may be different.

20 [0061] In the examples of FIG. 3 and FIG. 4, the front surface of each of the bonded wafers C1, E1, and G1 is removed by 50 μm . However, a removal amount of the front surface of each of the bonded wafers C1, E1, and G1 is not limited to this, and can be changed as appropriate so that each of the bonded wafers C1, E1, and G1 has a desired thickness. Further, when the thickness is a desired thickness at the time of bonding, here,
25 removal is unnecessary. Note that the film thickness of the bonded wafer need not be

the same as the film thickness of the original wafer, and may be different. When the wafer after bonding is thicker, cracking and deflection can be further reduced in a device manufacturing process. When the thicknesses are the same, a process similar to that for a regular wafer can be performed. Even when the bonded wafer is thin, the thickness of
5 the bonded wafer being 100 μm or more, more desirably 250 μm , and most desirably 300 μm or more can facilitate the flow of the device process.

[0062] Note that, after the process of removing each of the film thicknesses, finishing treatment may be performed through grinding, polishing, CMP, or the like. For finishing of the bonded surface of the divided wafers, in particular, precise treatment may
10 be required in order to reduce front surface roughness, and mirror-finishing treatment using polishing or CMP is desirable. In this manner, a high-quality bonded wafer can be obtained.

[0063] Note that the device structures A2, B2, C2, D2, E2, and F2 illustrated in FIG. 3 and FIG. 4 may be the same structures, or may be different. In other words, the device
15 structure on a regular wafer and the device structure on a bonded wafer may be different. For example, the device structure A2 and the device structure C2 may be different. When the thickness of the bonded wafer is thin and thus there is more sensitivity to deflection or cracking than a regular wafer, the deflection or the cracking can be avoided by manufacturing a device having a small process load on the bonded wafer.
20 Alternatively, influence of the deflection or the cracking on the bonded wafer can also be reduced by manufacturing a device that requires a thick epitaxial film. The device structure mentioned here may be a device structure in which a semiconductor element such as a diode, a transistor, or a thyristor or a combination of these is formed.

[0064] Further, the device structure on the bonded wafer may be determined depending
25 on a manufacture yield of a device formed by using a regular wafer. In other words,

when the quality of the regular wafer is low and the manufacture yield of the device formed by using the regular wafer is low, a device structure insensitive to the quality of the wafer may be formed on the bonded wafer obtained by dividing and bonding the wafer. Further, when the quality of the regular wafer is high and the manufacture yield of the device formed by using the regular wafer is high, a device structure sensitive to the quality of the wafer may be formed on the bonded wafer obtained by dividing and bonding the wafer. Here, the quality of the wafer may be determined by the amount or the type of defects that influence device characteristics. Thus, after measuring at least one of the amount and the type of the defects as well as the manufacture yield of the device in advance before formation of the device structure and obtaining information for determining that desired characteristics can be obtained, the device structure on the bonded wafer may be determined. As described above, by changing the device structures to be formed between a high-quality wafer having a high yield and a low-quality wafer having a low yield, the manufacture yield in the entire factory can be enhanced.

[0065] Note that, also when the process illustrated in FIG. 3 and FIG. 4 is changed as appropriate, $(2n-1)$ device-included wafers are obtained from n SiC wafers. As described above, the amount of the SiC wafers to be used can be reduced, and effects of reducing costs can be obtained. In other words, the effects of the technology of the present disclosure can be fully obtained.

[0066] In FIG. 5 and FIG. 6, only the thicknesses of the wafers are different from those of FIG. 3 and FIG. 4, and thus description of these figures will be omitted. As with FIG. 3 and FIG. 4, numerical values illustrated in FIG. 5 and FIG. 6 can also be changed as appropriate.

[0067] <A-3. Thicknesses of Wafers and Depths of Bonded Surfaces>

In the description using the example of FIG. 1, when a bonded surface is included in the device-included wafer 29, the bonded surface may influence device characteristics. When there is a bonding failure in the bonded surface, in particular, this adversely influences the device characteristics. In order to avoid such risks, it is desirable that the device-included wafer 29 be formed avoiding the bonded surface of the bonded wafer. Thus, it is desirable that the depth of the bonded surface in the bonded wafer 24 be larger than the thickness of the device-included wafer 29. In consideration of this, the depth of the bonded surface in the bonded wafer 24 is desirably 50 μm or more, more desirably 80 μm or more, and most desirably 100 μm or more. In this manner, even when the device structure is formed by using the bonded wafer, the device characteristics are not influenced by the bonded surface, and characteristics equivalent to those of when a regular wafer without bonding is used can be obtained.

[0068] Note that, in each of the bonded wafers C1, E1, and G1 before device structure formation illustrated in FIG. 3 and FIG. 4, the depth of the bonded surface is 225 μm . Further, in each of the bonded wafers C1, E1, and G1 before device structure formation illustrated in FIG. 5 and FIG. 6, the depth of the bonded surface is 160 μm .

[0069] As illustrated in FIG. 7, when the bonded wafer is formed by bonding two divided wafers, it is desirable that the depth of the bonded surface be 50 μm or more from the front surface of the bonded wafer. Further, as illustrated in FIG. 8, when the bonded wafer is formed by bonding three divided wafers, it is desirable that the depth of the shallowest bonded surface be 50 μm or more from the front surface of the bonded wafer.

[0070] In FIG. 3 and FIG. 4, the thickness of each of the bonded wafers C1, E1, and G1 is 500 μm , and in FIG. 5 and FIG. 6, the thickness of each of the bonded wafers C1, E1, and G1 is 350 μm . The thicknesses of these bonded wafers are determined, considering that there will be no deflection when the device structure is formed on the

bonded wafer. In other words, the thickness of the bonded wafer is desirably 100 μm or more, more desirably 250 μm , and most desirably 300 μm or more.

[0071] <A-4. Wafer Division Timings>

In FIG. 1 to FIG. 6, divided wafers are divided from the SiC wafer including
5 the device structure. In other words, division is performed after the device structure is formed on the SiC wafer. However, the timing at which the divided wafers constituting the bonded wafer are divided from the original SiC wafer is not limited to the timing after formation of the device structure on the original SiC wafer. In FIG. 9, "+" indicates various wafer division timings. Both of the divided wafer to be the front surface side of
10 the bonded wafer and the divided wafer to be the back surface side in later bonding may be divided before an epitaxial film is formed on the original SiC wafer (before epitaxy), may be divided after an epitaxial film is formed on the original SiC wafer and before the device structure is formed (after epitaxy), or may be divided after the device structure is formed on the original SiC wafer. Further, between the divided wafer to be the front
15 surface side of the bonded wafer and the divided wafer to be the back surface side in later bonding, the division timings from the original SiC wafer may be different. In other words, the division process may be performed before epitaxial film formation, before device formation, or after device formation.

[0072] FIG. 10 illustrates a basic process when the SiC wafer is divided before
20 formation of an epitaxial film. With reference to FIG. 10, the basic process will be described below.

[0073] First, a high-quality SiC wafer 40 and a low-quality SiC wafer 43 are prepared. The difference of quality in both of the SiC wafers 40 and 43 is exhibited in the number of defects, flatness, or the like, for example. The high-quality SiC wafer 40 has smaller
25 front surface defects or dislocation density in crystals, in comparison to the low-quality

SiC wafer 43. To assess the quality of the SiC wafer, for example, optical microscope observation, photoluminescence imaging observation, X-ray diffraction analysis, or the like is used.

[0074] The SiC wafer 40 is divided into two high-quality divided wafers 41 and 42, and similarly, the SiC wafer 43 is divided into two low-quality divided wafers 44 and 45. Subsequently, damaged layers formed in the cross-sectional surfaces of the divided wafers 41, 42, 44, and 45 are removed through grinding, polishing, or the like.

[0075] Next, the high-quality divided wafer 41 and the low-quality divided wafer 44 are bonded, and a bonded wafer 46 is formed. Further, the high-quality divided wafer 42 and the low-quality divided wafer 45 are bonded, and a bonded wafer 47 is formed.

[0076] Subsequently, an epitaxial film 48 and a device structure 49 are formed on the bonded wafer 46. A wafer made up of the bonded wafer 46, the epitaxial film 48, and the device structure 49 is referred to as a bonded wafer 50. Similarly, an epitaxial film 51 and a device structure 52 are formed on the bonded wafer 47. A wafer made up of the bonded wafer 47, the epitaxial film 51, and the device structure 52 is referred to as a bonded wafer 53.

[0077] Next, the bonded wafer 50 is divided into a device-included wafer 54 including the device structure 49 and the divided wafer 44. The device-included wafer 54 includes the high-quality divided wafer 41, the epitaxial film 48, and the device structure 49. Similarly, the bonded wafer 53 is divided into a device-included wafer 55 including the device structure 52 and the divided wafer 45. The device-included wafer 55 includes the high-quality divided wafer 42, the epitaxial film 51, and the device structure 52.

[0078] According to the method, by using the low-quality SiC wafer as a wafer in the bonded wafer on the back surface side, i.e., a support substrate, a plurality of device-included wafers can be created from the high-quality SiC wafer. Further, by

dividing a plurality of wafers from the initial SiC wafer before formation of an epitaxial film, all of the divided wafers, which have been divided, can be reused. Note that the high-quality divided wafer being used as the front surface side in the bonded wafer and the low-quality wafer being used as the back surface side in the bonded wafer can also be applied to a case in which the wafer is divided after device formation described in FIG. 1 to FIG. 6. As in the method, by assessing the quality of the wafer and utilizing the high-quality divided wafer as the front surface of the bonded wafer, the high-quality wafer can be more efficiently utilized, an overall device yield as a manufacturing factory can be enhanced, and productivity can be further enhanced.

10 [0079] <A-5. Modification>

In the description above, the original pre-divided wafer is a monocrystalline SiC wafer. In this case, because SiC is easily treated, there are advantages in that divided wafers are easily bonded. However, the original pre-divided wafer, for example, the first wafer, the first divided wafer, the first bonded wafer, or the like, need not be limited to SiC, and may be made of another monocrystalline material, such as diamond, gallium nitride (GaN), gallium oxide (Ga₂O₃), or aluminum nitride (AlN). Even in such a case, the divided wafers do not have a difference in thermal expansion coefficients, and thus bonding can be stably performed.

[0080] In the examples of FIG. 3 to FIG. 6, the thicknesses of the divided wafers constituting the bonded wafer are the same. For example, each of the thicknesses of the divided wafers A12 and B12 constituting the bonded wafer C1 in FIG. 3 is 275 μm . Further, each of the thicknesses of the divided wafers A12 and B12 constituting the bonded wafer C1 in FIG. 5 is 190 μm . However, the thicknesses of the divided wafers constituting the bonded wafer need not be the same.

25 [0081] In the examples of FIG. 3 to FIG. 6, one bonded wafer is divided into one

device-included wafer and one divided wafer not including the device structure. However, one bonded wafer may be divided into one device-included wafer and a plurality of divided wafers not including the device structure.

[0082] Further, in the example of FIG. 10, one SiC wafer 40 is divided into two
5 divided wafers 41 and 42. However, one SiC wafer 40 may be divided into a plurality of divided wafers. The same applies to the SiC wafer 43 in the example of FIG. 10.

[0083] <A-6. Effects>

In reference to the example of FIG. 1, the manufacturing method for the semiconductor device according to the first embodiment includes the steps of: (a)
10 dividing each of the plurality of SiC wafers 13 and 17 in a thickness direction to thereby obtain at least one divided wafer 20 or 23 not including the device structure from each of the SiC wafers 13 and 17; (b) bonding a plurality of divided wafers 20 and 23 obtained from different SiC wafers 13 and 17 to obtain the bonded wafer 24; and (c) forming the device structure 26 on the front surface of the bonded wafer 24. As described above, by
15 reusing the divided wafer 20 remaining after obtaining the device-included wafer 19 from the SiC wafer 13 together with another divided wafer 23, a further device-included wafer 29 can be obtained.

[0084] As a method of reusing the wafer, the method described in Patent Document 1, in which a thick epitaxial layer is formed on a divided wafer, has a problem in that
20 economic efficiency is poor and the wafer is liable to be deflected and cracked. In contrast, in the method of the present embodiment, the divided wafers are bonded, and therefore the wafer can be reused at a low cost with reduced deflection.

[0085] Further, in reference to the example of FIG. 1, the bonded wafer 24 is a bonded wafer obtained by bonding the plurality of divided wafers 20 and 23 that are divided from
25 different SiC wafers 13 and 17 and do not include the device structure. In addition, the

bonded surface of the plurality of divided wafers 20 and 23 is present at a depth of 50 μm or more from the front surface of the bonded wafer 24. In this manner, the device-included wafer 29 not including the bonded surface can be manufactured by using the bonded wafer 24. Therefore, influence given to device characteristics by the bonded surface can be avoided.

[0086] <B. Second Embodiment>

In the first embodiment, the bonded wafer is formed by bonding a plurality of divided wafers. In contrast, in the second embodiment, the bonded wafer is formed by bonding one divided wafer to a monocrystalline wafer not being a divided wafer.

[0087] <B-1. Basic Process>

FIG. 11 is a schematic diagram illustrating a basic process in the manufacturing method for the semiconductor device according to the second embodiment. With reference to FIG. 11, the manufacturing method for the semiconductor device according to the second embodiment will be described below.

[0088] First, a SiC wafer 63 and a monocrystalline SiC wafer 67 are prepared. The SiC wafer 63 is obtained by forming an epitaxial film 61 on a SiC wafer 60 and further forming a device structure 62 on the epitaxial film 61.

[0089] Next, the SiC wafer 63 is divided into a device-included wafer 65 including the device structure 62 and a divided wafer 66 not including the device structure 62. The device-included wafer 65 includes a SiC wafer 64 divided from the SiC wafer 60, the epitaxial film 61 on the SiC wafer 64, and the device structure 62 on the epitaxial film 61.

[0090] In the back surface of the device-included wafer 65 and the front surface of the divided wafer 66, damaged layers due to division are generated. These damaged layers are removed through grinding, polishing, or the like.

[0091] Next, the divided wafer 66 is bonded to the monocrystalline SiC wafer 67, and

a bonded wafer 68 is thereby formed. The divided wafer 66 corresponds to the front surface side of the bonded wafer 68, and the monocrystalline SiC wafer 67 corresponds of the back surface side of the bonded wafer 68. As described above, the monocrystalline SiC wafer 67 is used as a support substrate of the divided wafer 66.

5 [0092] Subsequently, an epitaxial film 69 is formed on the bonded wafer 68, and a device structure 70 is further formed on the epitaxial film 69. A wafer made up of the bonded wafer 68, the epitaxial film 69, and the device structure 70 is referred to as a bonded wafer 71.

[0093] Next, the bonded wafer 71 is divided into a device-included wafer 72 including
10 the device structure 70 and the monocrystalline SiC wafer 67. Here, it is desirable that the device-included wafer 72 not include the bonded surface between the divided wafer 66 and the monocrystalline SiC wafer 67. Thus, in consideration of the thickness of the device structure 70, the bonded surface between the divided wafer 66 and the monocrystalline SiC wafer 67 in the bonded wafer 68 is desirably located at a depth of 50
15 μm or more from the front surface of the bonded wafer 68, more desirably located at a position 80 μm deep therefrom, and most desirably located at a depth of 100 μm or more therefrom. In other words, the thickness of the divided wafer 66 is desirably 50 μm or more, more desirably 80 μm or more, and most desirably 100 μm or more. In this manner, the bonded surface is not included in the device-included wafer 72, and influence
20 given to the device by the bonded surface can be removed.

[0094] As described above, the monocrystalline SiC wafer 67 is used as a support substrate when the device structure 70 is formed on the divided wafer 66. After being divided from the bonded wafer 71, the monocrystalline SiC wafer 67 can be reused as a support substrate of another divided wafer. Here, the support substrate may not have a
25 structure suitable for bonding to the SiC wafer, such as deflection, front surface roughness,

or front surface unevenness. In view of this, before the SiC wafer and the support substrate are bonded, the structure suitable for bonding to the support substrate, such as deflection, front surface roughness, or front surface unevenness, may be formed on the SiC wafer, the support substrate, or both of these by treating a surface of the SiC wafer to be bonded to the support substrate through grinding, polishing, CMP, or the like or treating the SiC wafer through pressurization, heating, or the like. This allows for satisfactory bonding between the SiC wafer and the support substrate.

[0095] Note that the board thickness of the monocrystalline SiC wafer 67 divided from the bonded wafer 71 may be changed from the original board thickness of the monocrystalline SiC wafer 67. In other words, when the monocrystalline SiC wafer 67 is divided from the bonded wafer 71, the monocrystalline SiC wafer 67 need not be divided at the bonded surface between the divided wafer 66 and the monocrystalline SiC wafer 67. Further, the bonded surface may be removed by removing a damaged layer of the divided monocrystalline SiC wafer 67. Further, the bonded surface may remain in the divided monocrystalline SiC wafer 67.

[0096] In the example of FIG. 11, one SiC wafer 63 is divided into one device-included wafer 65 and one divided wafer 66 not including the device structure. However, one SiC wafer 63 may be divided into one device-included wafer 65 and a plurality of divided wafers not including the device structure.

[0097] Instead of the monocrystalline SiC wafer 67, a monocrystalline GaN wafer or a monocrystalline gallium oxide wafer may be used. Such alternative wafers may be used from the perspective of thermal management in the device manufacturing process, such as heat dissipation from the wafer or heat storage in the wafer.

[0098] Instead of the SiC wafer 63, a wafer made of another material mentioned in the first embodiment may be used. In that case, when a wafer to be used as a support

substrate and a divided wafer are made of the same material, bonding strength is easily secured.

[0099] The bonded wafer obtained by bonding the divided wafer and the support substrate may have different amounts of various defects, such as crystalline defects, for example, threading dislocation, across the bonded surface, depending on a state of each of the wafers. In this case, densities of crystalline defects present in a surface layer may be different or densities of crystalline defects present near a bonded interface may be different between a device structure formation surface side and its opposite surface side of the bonded wafer. Moreover, threading dislocations, which are continuous from the front surface to the back surface in a regular wafer, are discontinuous in the bonded interface in the bonded wafer. However, even when the amounts of various defects are different between a plurality of wafers, influence given thereby to the device process or device characteristics can be ignored. Here, by selecting the device structure, the divided wafer, or the support substrate as appropriate, the influence given to the device process or the device characteristics by the discontinuity of the defects described above or the like can be further reduced. In addition, by arranging not to include the bonded surface in the device-included wafer, the influence given to the device characteristics by the discontinuity of the defects described above or the like can be eliminated.

[0100] <B-2. Modification>

FIG. 12 is a schematic diagram illustrating a basic process in the manufacturing method for the semiconductor device according to a modification of the second embodiment. In the present modification, the SiC wafer is divided before an epitaxial film is formed. With reference to FIG. 12, the manufacturing method for the semiconductor device according to the modification of the second embodiment will be described below.

[0101] First, a SiC wafer 80 and two monocrystalline SiC wafers 83 and 84 are prepared.

[0102] Next, the SiC wafer 80 is divided into two divided wafers 81 and 82.

[0103] In the back surface of the divided wafer 81 and the front surface of the divided
5 wafer 82, damaged layers due to division are generated. These damaged layers are removed through grinding, polishing, or the like.

[0104] Subsequently, the divided wafer 81 and the monocrystalline SiC wafer 83 are bonded to form a bonded wafer 85, and the divided wafer 82 and the monocrystalline SiC wafer 84 are bonded to form a bonded wafer 86. As described above, the
10 monocrystalline SiC wafers 83 and 84 are used as support substrates of the divided wafers 81 and 82.

[0105] Next, an epitaxial film 87 is formed on the bonded wafer 85, and a device structure 88 is formed on the epitaxial film 87. A wafer made up of the bonded wafer 85, the epitaxial film 87, and the device structure 88 is referred to as a bonded wafer 89.
15 Similarly, an epitaxial film 90 is formed on the bonded wafer 86, and a device structure 91 is formed on the epitaxial film 90. A wafer made up of the bonded wafer 86, the epitaxial film 90, and the device structure 91 is referred to as a bonded wafer 92.

[0106] Subsequently, the bonded wafer 89 is divided into a device-included wafer 93 including the device structure 88 and the monocrystalline SiC wafer 83. The
20 device-included wafer 93 includes the divided wafer 81, the epitaxial film 87, and the device structure 88. Similarly, the bonded wafer 92 is divided into a device-included wafer 94 including the device structure 91 and the monocrystalline SiC wafer 84. The device-included wafer 94 includes the divided wafer 82, the epitaxial film 90, and the device structure 91.

25 [0107] Here, it is desirable that the device-included wafers 93 and 94 not include the

bonded surfaces between the divided wafers 81 and 82 and the monocrystalline SiC wafers 83 and 84. Thus, in consideration of the thickness of each of the device structures 88 and 91, each of the bonded surfaces between the divided wafers 81 and 82 and the monocrystalline SiC wafers 83 and 84 in the bonded wafers 85 and 86 is desirably located at a depth of 50 μm or more from the front surface of each of the bonded wafers 85 and 86, desirably located at a position 80 μm deep therefrom, and most desirably located at a depth of 100 μm or more therefrom. In other words, the thickness of each of the divided wafers 81 and 82 is desirably 50 μm or more, more desirably 80 μm or more, and most desirably 100 μm or more. In this manner, the bonded surface is not included in each of the device-included wafers 93 and 94, and influence given to the device by the bonded surface can be removed.

[0108] According to the method described above, by using the monocrystalline SiC wafers 83 and 84 as support substrates, the device structures 88 and 91 can be formed on the plurality of divided wafers 81 and 82 divided from the SiC wafer. Further, the monocrystalline SiC wafers 83 and 84 divided from the bonded wafers 89 and 92 can be reused as support substrates for other divided wafers.

[0109] Note that the board thickness of each of the monocrystalline SiC wafers 83 and 84 divided from the bonded wafers 89 and 92 may be changed from the original board thickness of each of the monocrystalline SiC wafers 83 and 84. In other words, when each of the monocrystalline SiC wafers 83 and 84 is divided from the bonded wafers 89 and 92, each of the monocrystalline SiC wafers 83 and 84 need not be divided at each of the bonded surfaces between the divided wafers 81 and 82 and the monocrystalline SiC wafers 83 and 84. Further, each of the bonded surfaces may be removed by removing a damaged layer of each of the divided monocrystalline SiC wafers 83 and 84. Further, each of the bonded surfaces may remain in each of the divided monocrystalline SiC

wafers 83 and 84.

[0110] In the example of FIG. 12, one SiC wafer 80 is divided into two divided wafers 81 and 82. However, one SiC wafer 80 may be divided into three or more divided wafers.

5 [0111] Instead of the SiC wafer 80, a wafer made of another material also mentioned in the first embodiment may be used. In that case, it is desirable that a wafer to be used as a support substrate and a divided wafer be made of the same material in order to secure bonding strength.

[0112] <B-3. Effects>

10 The manufacturing method for the semiconductor device according to the second embodiment includes the steps of: (a) dividing the wafer in a thickness direction to thereby obtain the divided wafer; (b) bonding the divided wafer to the monocrystalline support substrate to obtain the bonded wafer; and (c) forming the device structure on the bonded wafer. In this manner, the semiconductor device can be manufactured by
15 reusing the wafer with high productivity with reduced cracking in the wafer.

[0113] Further, the bonded wafer according to the second embodiment is a bonded wafer obtained by bonding the divided wafer that is divided from the wafer and does not include the device structure to the support substrate, and it is desirable that the bonded surface between the divided wafer and the support substrate be present at a depth of 50
20 μm or more from the front surface. In this case, when the device structure is formed on the bonded wafer and then a device structure-included wafer including the device structure is divided from the bonded wafer, the bonded surface is not included in the device structure-included wafer, and therefore influence given to the device by the bonded surface can be removed.

25 [0114] When the divided wafer illustrated in the first embodiment is used as a support

substrate (for example, the process illustrated in FIG. 10), the wafer to be the support substrate is divided from a regular wafer to be manufactured, and thus there may be a restriction on the thickness of the support substrate, or waste may be caused in removing the support substrate or the divided wafer to obtain the bonded wafer having a desired film thickness. In the present embodiment, the support substrate is directly divided from an ingot to be manufactured. Therefore, there is no restriction on the board thickness, and waste can be reduced because a monocrystalline wafer having a board thickness necessary as the support substrate can be directly manufactured. In this manner, high effects of reducing costs can be obtained. Further, by using low-quality crystals having many crystalline defects unsuitable for device manufacture as the support substrate, material loss throughout the overall manufacturing process can also be reduced.

[0115] <C. Third Embodiment>

In the second embodiment, the bonded wafer is formed by bonding one divided wafer to a monocrystalline wafer not being a divided wafer. In contrast, in the third embodiment, the bonded wafer is formed by bonding one divided wafer to a polycrystalline wafer not being a divided wafer.

[0116] <C-1. Basic Process>

FIG. 13 is a schematic diagram illustrating a basic process in the manufacturing method for the semiconductor device according to the third embodiment. With reference to FIG. 13, the manufacturing method for the semiconductor device according to the third embodiment will be described below.

[0117] First, a SiC wafer 103 and a polycrystalline SiC wafer 107 are prepared. The SiC wafer 103 is obtained by forming an epitaxial film 101 on a SiC wafer 100 and further forming a device structure 102 on the epitaxial film 101.

[0118] Next, the SiC wafer 103 is divided into a device-included wafer 105 including

the device structure 102 and a divided wafer 106 not including the device structure 102. The device-included wafer 105 includes a SiC wafer 104 divided from the SiC wafer 100, the epitaxial film 101 on the SiC wafer 104, and the device structure 102 on the epitaxial film 101.

5 [0119] In the back surface of the device-included wafer 105 and the front surface of the divided wafer 106, damaged layers due to division are generated. These damaged layers are removed through grinding, polishing, or the like.

[0120] Next, the divided wafer 106 is bonded to the polycrystalline SiC wafer 107, and a bonded wafer 108 is thereby formed. The divided wafer 106 corresponds to the front
10 surface side of the bonded wafer 108, and the polycrystalline SiC wafer 107 corresponds of the back surface side of the bonded wafer 108. As described above, the polycrystalline SiC wafer 107 is used as a support substrate of the divided wafer 106.

[0121] Subsequently, an epitaxial film 109 is formed on the bonded wafer 108, and a device structure 110 is further formed on the epitaxial film 109. A wafer made up of the
15 bonded wafer 108, the epitaxial film 109, and the device structure 110 is referred to as a bonded wafer 111.

[0122] Next, the bonded wafer 111 is divided into a device-included wafer 112 including the device structure 110 and the polycrystalline SiC wafer 107. As described above, the polycrystalline SiC wafer 107 is used as a support substrate when the device
20 structure 110 is formed on the divided wafer 106. After being divided from the bonded wafer 111, the polycrystalline SiC wafer 107 can be reused as a support substrate of another divided wafer. Here, the support substrate may not have a structure suitable for bonding to the SiC wafer, such as deflection, front surface roughness, or front surface unevenness. In view of this, before the SiC wafer and the support substrate are bonded,
25 the structure suitable for bonding to the support substrate, such as deflection, front surface

roughness, or front surface unevenness, may be formed on the SiC wafer, the support substrate, or both of these by treating a surface of the SiC wafer to be bonded to the support substrate through grinding, polishing, CMP, or the like or treating the SiC wafer through pressurization, heating, or the like. This allows for satisfactory bonding
5 between the SiC wafer and the support substrate.

[0123] Note that the board thickness of the polycrystalline SiC wafer 107 divided from the bonded wafer 111 may be changed from the original board thickness of the polycrystalline SiC wafer 107. In other words, when the polycrystalline SiC wafer 107 is divided from the bonded wafer 111, the polycrystalline SiC wafer 107 may be, but not
10 necessarily, divided at the bonded surface between the divided wafer 106 and the polycrystalline SiC wafer 107. Further, the bonded surface may be removed by removing a damaged layer of the divided polycrystalline SiC wafer 107. Further, the bonded surface may remain in the divided polycrystalline SiC wafer 107.

[0124] The bonded wafer 108 includes the bonded surface between the divided wafer
15 106 and the polycrystalline SiC wafer 107. It is desirable that the device-included wafer 112 not include the bonded surface. Thus, the depth of the bonded surface between the divided wafer 106 and the polycrystalline SiC wafer 107 in the bonded wafer 108 is desirably 50 μm or more, more desirably 80 μm or more, and most desirably 100 μm or more. In other words, the thickness of the divided wafer 106 divided from the SiC wafer
20 103 is desirably 50 μm or more, more desirably 80 μm or more, and most desirably 100 μm or more. In this manner, the bonded surface is not included in the device-included wafer 112, and influence given to the device by the bonded surface can be removed.

[0125] In the example of FIG. 13, one SiC wafer 103 is divided into one device-included wafer 105 and one divided wafer not including the device structure.
25 However, one SiC wafer 103 may be divided into one device-included wafer 105 and a

plurality of divided wafers not including the device structure.

[0126] Instead of the SiC wafer 63, a wafer made of another material also mentioned in the first embodiment may be used. In that case, it is desirable that a wafer to be used as a support substrate and a divided wafer be made of the same material in order to secure bonding strength.

[0127] The bonded wafer obtained by bonding the divided wafer and the support substrate may have different amounts of various defects, such as crystalline defects, for example, threading dislocation, across the bonded surface, depending on a state of each of the wafers. In this case, densities of crystalline defects present in a surface layer may be different or densities of crystalline defects present near a bonded interface may be different between a device structure formation surface side and its opposite surface side of the bonded wafer. Moreover, threading dislocations, which are continuous from the front surface to the back surface in a regular wafer, are discontinuous in the bonded interface in the bonded wafer. However, even when the amounts of various defects are different between a plurality of wafers, influence given thereby to the device process or device characteristics can be ignored. Here, by selecting the device structure, the divided wafer, or the support substrate as appropriate, the influence given to the device process or the device characteristics by the discontinuity of the defects described above or the like can be further reduced. In addition, by arranging not to include the bonded surface in the device-included wafer, the influence given to the device characteristics by the discontinuity of the defects described above or the like can be eliminated.

[0128] <C-2. Modification>

FIG. 14 is a schematic diagram illustrating a basic process in the manufacturing method for the semiconductor device according to a modification of the third embodiment.

In the present modification, the SiC wafer is divided before an epitaxial film is formed.

In addition, the SiC wafer may be divided after an epitaxial film is formed and before a device structure is formed. With reference to FIG. 14, the manufacturing method for the semiconductor device according to the modification of the third embodiment will be described below.

5 [0129] First, a SiC wafer 120 and two polycrystalline SiC wafers 123 and 124 are prepared.

[0130] Next, the SiC wafer 120 is divided into two divided wafers 121 and 122.

[0131] In the back surface of the divided wafer 121 and the front surface of the divided wafer 122, damaged layers due to division are generated. These damaged layers are
10 removed through grinding, polishing, or the like.

[0132] Subsequently, the divided wafer 121 and the polycrystalline SiC wafer 123 are bonded to form a bonded wafer 125, and the divided wafer 122 and the polycrystalline SiC wafer 124 are bonded to form a bonded wafer 126. As described above, the polycrystalline SiC wafer 123 is used as a support substrate of the divided wafer 121, and
15 the polycrystalline SiC wafer 124 is used as a support substrate of the divided wafer 122.

[0133] Next, an epitaxial film 127 is formed on the bonded wafer 125, and a device structure 128 is formed on the epitaxial film 127. A wafer made up of the bonded wafer 125, the epitaxial film 127, and the device structure 128 is referred to as a bonded wafer 129. Similarly, an epitaxial film 130 is formed on the bonded wafer 126, and a device
20 structure 131 is formed on the epitaxial film 130. A wafer made up of the bonded wafer 126, the epitaxial film 130, and the device structure 131 is referred to as a bonded wafer 132.

[0134] The bonded wafers 125 and 126 include the bonded surfaces between the divided wafers 121 and 122 and the polycrystalline SiC wafers 123 and 124. It is
25 desirable that the device-included wafers 133 and 134 not include the bonded surfaces.

Thus, the depth of each of the bonded surfaces between the divided wafers 121 and 122 and the polycrystalline SiC wafers 123 and 124 in the bonded wafers 125 and 126 is desirably 50 μm or more, more desirably 80 μm or more, and most desirably 100 μm or more. In other words, the thickness of each of the divided wafers 121 and 122 divided
5 from the SiC wafer 120 is desirably 50 μm or more, more desirably 80 μm or more, and most desirably 100 μm or more. In this manner, the bonded surface is not included in each of the device-included wafers 133 and 134, and influence given to the device by the bonded surface can be removed.

[0135] Subsequently, the bonded wafer 129 is divided into the device-included wafer
10 133 including the device structure 128 and the polycrystalline SiC wafer 123. The device-included wafer 133 includes the divided wafer 121, the epitaxial film 127, and the device structure 128. Similarly, the bonded wafer 132 is divided into the device-included wafer 134 including the device structure 131 and the polycrystalline SiC wafer 124. The device-included wafer 134 includes the divided wafer 122, the epitaxial
15 film 130, and the device structure 131.

[0136] According to the method described above, by using the polycrystalline SiC wafers 123 and 124 as support substrates, the device structures 128 and 131 can be formed on the plurality of divided wafers 121 and 122 divided from the SiC wafer. Further, the polycrystalline SiC wafers 123 and 124 divided from the bonded wafers 129
20 and 132 can be reused as support substrates for other divided wafers.

[0137] Note that the board thickness of each of the polycrystalline SiC wafers 123 and 124 divided from the bonded wafers 129 and 132 may be changed from the original board thickness of each of the polycrystalline SiC wafers 123 and 124. In other words, when each of the polycrystalline SiC wafers 123 and 124 is divided from the bonded wafers 129
25 and 132, each of the polycrystalline SiC wafers 123 and 124 need not be divided at each

of the bonded surfaces between the divided wafers 121 and 122 and the polycrystalline SiC wafers 123 and 124. Further, each of the bonded surfaces may be removed by removing a damaged layer of each of the divided polycrystalline SiC wafers 123 and 124. Further, each of the bonded surfaces may remain in each of the divided polycrystalline SiC wafers 123 and 124.

[0138] In the example of FIG. 14, one SiC wafer 120 is divided into two divided wafers. However, one SiC wafer 120 may be divided into three or more divided wafers.

[0139] <C-3. Effects>

In reference to the example of FIG. 14, the manufacturing method for the semiconductor device according to the third embodiment includes the steps of: (a) dividing the SiC wafer 120 in a thickness direction to thereby obtain the divided wafers 121 and 122 each having a thickness of 50 μm or more; (b) bonding the divided wafers 121 and 122 to the polycrystalline SiC wafers 123 and 124 being support substrates to obtain the bonded wafers 125 and 126; and (c) forming the device structures 128 and 131 on the bonded wafers 125 and 126. In this manner, the semiconductor device can be manufactured by reusing the wafer with high productivity with reduced cracking in the wafer.

[0140] Further, in reference to the example of FIG. 14, the bonded wafer according to the third embodiment is a bonded wafer obtained by bonding the divided wafers 121 and 122 that are divided from the SiC wafer 120 and do not include the device structure to the polycrystalline SiC wafers 123 and 124 being support substrates, and each of the bonded surfaces between the divided wafers 121 and 122 and the polycrystalline SiC wafers 123 and 124 is present at a depth of 50 μm or more from the front surface. In this manner, the semiconductor device can be manufactured by reusing the wafer with high productivity with reduced cracking in the wafer.

[0141] When the divided wafer illustrated in the first embodiment is used as a support substrate (for example, the process illustrated in FIG. 10), the wafer to be the support substrate is divided from a regular wafer to be manufactured, and thus there may be a restriction on the thickness of the support substrate, or waste may be caused in removing
5 the support substrate or the divided wafer to obtain the bonded wafer having a desired film thickness. In the present embodiment, the support substrate is directly divided from an ingot to be manufactured. Therefore, there is no restriction on the board thickness, and waste can be reduced because a monocrystalline wafer having a board thickness necessary as the support substrate can be directly manufactured. In this manner, high
10 effects of reducing costs can be obtained. Further, by using low-quality crystals having many crystalline defects unsuitable for device manufacture as the support substrate, material loss throughout the overall manufacturing process can also be reduced.

[0142] Further, in comparison to when a monocrystalline wafer is used as the support substrate illustrated in the second embodiment, a polycrystalline substrate can be
15 manufactured at a low price, and effects of reducing costs can be obtained.

[0143] Note that each embodiment can be freely combined, or each embodiment can be modified or omitted as appropriate. The above description is in all aspects illustrative. It is therefore understood that numerous unillustrated modifications can be devised. For example, features of the processes of division, bonding, and treatment on the front and
20 back of wafers related to these or the divided wafers, the bonded wafers, and the device-included wafers illustrated in the first embodiment can be combined or modified or omitted as appropriate in embodiments using the support substrates illustrated in the second and third embodiments.

EXPLANATION OF REFERENCE SIGNS

25 [0144] 10, 13 SiC wafer, 11, 15, 25 Epitaxial film, 12, 16, 26 Device structure, 19, 22,

29 Device-included wafer, 20, 23, 30, 66, 106 Divided wafer, 67 Monocrystalline SiC substrate, 107 Polycrystalline SiC substrate.

CLAIMS

[Claim 1] A manufacturing method for a semiconductor device, the manufacturing method comprising the steps of:

(a) dividing each of a plurality of first wafers in a thickness direction to thereby
5 obtain at least one first divided wafer not including a device structure from each of the first wafers;

(b) bonding a plurality of the first divided wafers obtained from different first wafers to obtain a first bonded wafer being a bonded wafer; and

(c) forming the device structure on a front surface of the first bonded wafer.
10

[Claim 2] The manufacturing method for the semiconductor device according to claim 1, wherein

the step (a) is a step of dividing each of the first wafers on which the device structure is formed on the front surface into a first device-included wafer being a
15 device-included wafer including the device structure and the at least one first divided wafer.

[Claim 3] The manufacturing method for the semiconductor device according to claim 1 or 2, further comprising the step of

20 (d) dividing the first bonded wafer on which the device structure is formed into a second device-included wafer being a device-included wafer including the device structure and at least one second divided wafer not including the device structure.

[Claim 4] The manufacturing method for the semiconductor device according to claim 3,
25 further comprising the step of

(e) after the step (d), repeating the step (b) to the step (d) at least once, with the second divided wafer being used as a new first divided wafer.

[Claim 5] The manufacturing method for the semiconductor device according to any one
5 of claims 1 to 4, wherein

at least one of the first wafers is a bonded wafer formed by bonding a plurality of wafers.

[Claim 6] The manufacturing method for the semiconductor device according to claim 3,
10 wherein

when an original pre-divided wafer of the device-included wafer is the bonded wafer formed by bonding a plurality of wafers, the device-included wafer does not include a bonded surface included in an original pre-divided bonded wafer.

15 [Claim 7] The manufacturing method for the semiconductor device according to any one of claims 1 to 6, wherein

a material of each of the first wafers is SiC.

[Claim 8] The manufacturing method for the semiconductor device according to claim 7,
20 wherein

a material of each of the first wafers is monocrystalline SiC.

[Claim 9] The manufacturing method for the semiconductor device according to any one of claims 1 to 8, wherein

25 a thickness of the first divided wafer is 50 μm or more.

[Claim 10] The manufacturing method for the semiconductor device according to any one of claims 1 to 9, wherein

the device structure is a SiC power device structure.

5

[Claim 11] A bonded wafer obtained by bonding a plurality of divided wafers that are divided from different wafers and do not include a device structure, wherein

a bonded surface of the plurality of divided wafers is present at a depth of 50 μm or more from a front surface.

10

[Claim 12] The bonded wafer according to claim 11, wherein

a material of each of the wafers is SiC.

[Claim 13] The bonded wafer according to claim 12, wherein

15 a material of each of the wafers is monocrystalline SiC.

[Claim 14] The bonded wafer according to any one of claims 11 to 13, wherein

each of the wafers has an N-type or P-type conductivity type or semi-insulating property.

20

[Claim 15] The bonded wafer according to any one of claims 11 to 14, wherein

an amorphous layer is present in the bonded surface of the plurality of divided wafers.

25 [Claim 16] A manufacturing method for a semiconductor device, the

manufacturing method comprising the steps of:

- (a) dividing a wafer in a thickness direction to thereby obtain a divided wafer;
- (b) bonding the divided wafer to a support substrate to obtain a bonded wafer;

and

- 5 (c) forming a device structure on the bonded wafer.

[Claim 17] The manufacturing method for the semiconductor device according to claim 16, wherein

 a bonded surface between the divided wafer and the support substrate in the
10 bonded wafer is located at a depth of 50 μm or more from a front surface of the bonded wafer.

[Claim 18] The manufacturing method for the semiconductor device according to claim 16 or 17, wherein

15 the support substrate is monocrystalline SiC or monocrystalline GaN.

[Claim 19] The manufacturing method for the semiconductor device according to claim 16 or 17, wherein

 the support substrate is a polycrystalline substrate.

20

[Claim 20] A bonded wafer obtained by bonding a divided wafer that is divided from a wafer and does not include the device structure to a support substrate, wherein

 a bonded surface between the divided wafer and the support substrate is present at a depth of 50 μm or more from a front surface.

25

[Claim 21] The bonded wafer according to claim 20, wherein
a material of each of the wafer and the support substrate is monocrystalline SiC
or monocrystalline GaN.

5 [Claim 22] The bonded wafer according to claim 20, wherein
a material of the wafer is polycrystalline SiC.

[Claim 23] The bonded wafer according to any one of claims 20 to 22, wherein
the wafer has an N-type or P-type conductivity type or semi-insulating property.

10

[Claim 24] The bonded wafer according to any one of claims 20 to 23, wherein
an amorphous layer is present in the bonded surface between the divided wafer
and the support substrate.