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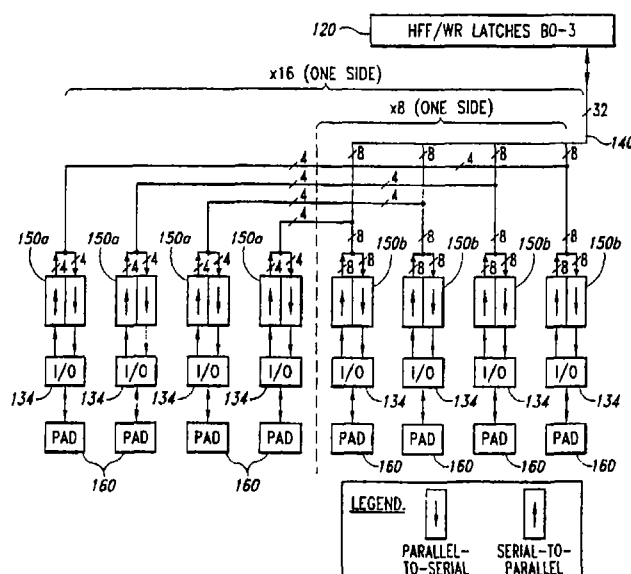
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) Title: MEMORY DEVICE AND METHOD HAVING DATA PATH WITH MULTIPLE PREFETCH I/O CONFIGURATIONS



(57) **Abstract:** A memory device is operable in either a high mode or a low speed mode. In either mode, 32 bits of data from each of two memory arrays are prefetched into respective sets of 32 flip-flops (120). In the high speed mode, the prefetched data bits are transferred in parallel to 4 parallel-to-serial converters (150a), which transfrom the parallel data bits to a burst of 8 serial data bits and apply the burst to a respective one of 4 data bus terminals (160). In the low speed mode, two sets of prefetched data bits are transferred in parallel to 8 parallel-to-serial converters (150a), which transfrom the parallel data bits to a burst of 8 serial data bits and apply the burst to a respective on of 8 data bus terminals (160)