TIMING RECOVERY SYSTEM FOR A DIGITAL SIGNAL PROCESSOR

ABSTRACT OF THE DISCLOSURE

A timing recovery system for a digital signal receiver receives a signal, representing successive symbols, from a transmitter. The symbols are subject to exhibiting multiple symbol rates. The system derives a sample enable signal from the received input signal and employs a single, fixed frequency oscillator. A source (10) of samples representing the received signal are sampled at a fixed frequency. An interpolator (12) is coupled to the sample source and is responsive to a control signal. The interpolator produces samples taken at times synchronized to the successive symbols from the transmitter. A phase error detector (16) is coupled to the interpolator, detects a phase error between the sample times of the transmitter synchronized samples produced by the interpolator and times of the successive transmitter symbols, and supplies a phase error signal. The phase error signal is coupled to one input terminal of a summer (32) and a source (31) of a nominal delay signal is coupled to the other. A numerically controlled delay (34-46) produces the control signal for the interpolator in response to the signal from the summer. An output signal from the interpolator is filtered by a fixed, non-adaptive pulse-shaping filter (14).

Figure 2