ABSTRACT

An integrated circuit (IC) device includes a fin-type active region, a channel region on the fin-type active region, a gate line surrounding the channel region on the fin-type active region, a source/drain region that is adjacent to the gate line on the fin-type active region and has a sidewall facing the channel region, wherein the source/drain region includes a first buffer layer, a second buffer layer, and a main body layer, which are sequentially stacked in a direction away from the fin-type active region, each include a $Si_{1-x}Ge_x$ layer ($x \neq 0$) doped with a p-type dopant, and have different Ge concentrations, and the second buffer layer conformally covers a surface of the first buffer layer that faces the main body layer. A thickness ratio of the side buffer portion to the bottom buffer portion is in a range of about 0.9 to about 1.1.

FIG. 2A