A NEW METHOD TO FORM N- AND P-CHANNEL TRANSISTORS WITH SHALLOW JUNCTIONS

ABSTRACT

A method for forming N- and P-channel transistors having shallow junctions in an integrated circuit device is described. A semiconductor substrate is provided having active regions separated from one another by isolation regions wherein there is a N-channel active region and a P-channel active region and wherein gate electrodes and associated lightly doped source and drain regions have been formed in each of the active regions. A layer of borosilicate glass is deposited overlying the semiconductor substrate. A photoresist mask is formed over the P-channel active region. The borosilicate glass layer is etched away where it is not covered by the photoresist mask thereby leaving the borosilicate glass layer only overlying the P-channel region. The photoresist mask is removed. A layer of phosphosilicate glass is deposited overlying the semiconductor substrate. The semiconductor substrate is heated whereby boron ions within the borosilicate glass layer are driven into the semiconductor substrate in the P-channel region to form heavily doped P-channel source and drain regions and whereby phosphorus ions within the phosphosilicate glass layer are driven into the semiconductor substrate in the N-channel region to form heavily doped N-channel source and drain regions. The phosphosilicate layer is planarized to complete the formation of N- and P-channel transistors in the fabrication of an integrated circuit device.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)