Computer System

Field of Technology

The invention relates to computer technology, particularly it concerns computer systems.

The invention has application in both engineering and technical calculations for space and aviation technologies, geodesy, hydrometeorology and other fields which require high performance computations.

Prior Technology

There is a known computer system which contains central input-output processors, a switch, a main memory unit, a control panel, peripheral memory devices with control blocks and data transmission processors (SU, A, 692400).

In this system Von Neumann's principle of data processing is used. Every central processor contains a conforming (conjugating) unit, a block for performing procedures, an indexing block, a block for value retrieving, a block for processing strings, an arithmetic-logical unit, a block of the basic registers, a unit for instructions forming, a control unit, a unit for the distribution of stack addresses, a buffering stack of operands, an associative memory unit, a unit for transformation of the mathematical addresses into the physical ones, a block of memory for buffering instructions, a block for analysis of interrupts.

The arithmetic-logical unit includes: blocks for multiplication, addition, division, code transformation and logical operation performing. These blocks work in parallel and independently from one another, providing parallel data processing within each processor and using the natural parallelism of the programs under execution.

However, implementation of this unit has shown that, in practice, the use of Von Neumann's principle of computation organization requires high unproductive expenditures of hardware and

computing capacity to provide parallel work of several executive devices. These expenditures, first of all, are related to the fact that to form independent sequences of instructions from the program in execution it is necessary to do a preliminary survey of program segments (of the average length up to 30 instructions) and a dynamic planning of executing units loading with the help of special hardware means, which was described in detail (Babayan B.A. "Main results and perspective of development of the "Elbrus" architecture", Applied Computer Science works collection, vol. 15, Moscow, Finance and Statistics, 1989, pp. 100-131).

Due to this fact the hardware becomes considerably more complicated, having simultaneously a low real increase of performance. Parallelism of program processing on several executive devices is restricted and does not spread on the whole program (the segments of parallel processing do not exceed 10-20 instructions). Moreover, the process of extraction of instructions from the program for parallel execution itself requires a large amount of additional hardware and working time of the processor. This is another factor of the decrease in performance.

There is a known device which contains units of common memory, units of central input-output processors, using Von Neumann's principle of computation processing and parallel work of several executive devices, being parts of central processors. This device achieves program processing parallelism by means of forming an extensive instruction which includes operations for the simultaneous start of several arithmetic units (SU, A, 1777148).

Formation of such an instruction is conducted by static operation planning during the program translation stage. Here, the number of operations of the instruction being executed in parallel is limited (it does not exceed 7).

However, this device does not achieve high performance based on the internal parallelism of the programs in execution because of limited parallelism of operations in execution in the device and a cessation of execution when all the operands necessary for a computation are not available. This problem arises from the restrictions set by the translator and also in the case when the variable position in memory depends on computation conditions. Also, this device has a complicated translator structure and a large amount of the hardware to conduct local parallelism of computation.

There is a known computer system which contains a switch and N processor units. In such a system the first control outputs and address outputs of the i-th processor unit (i = 1,..,N) are connected correspondingly with the i-th input of the first control input group and with the i-th input of the group of the address switch inputs. The first and second informational outputs of the i-th processor unit are connected with the corresponding i-th input of the group of informational switch inputs. The first informational, address, control and the second informational, address, control inputs of the i-th processor unit are connected with the first and second informational system inputs. The first control input of this system is connected with the control switch input and with the third control input of the i-th processor unit. The switch control output is connected with the fourth control input of the i-th processor unit. The third informational output of this unit is connected with the first informational output of the system. The computer system can have a second informational output and a third informational input (US. 4814978).

For computation organization this system uses the data flow principle, which provides effective loading for each processor unit and high total performance. This is achieved by means of parallel instruction execution in all sections of the program and is supported by a programmable computation organization. The program is mapped as a graph, each node of which

is an instruction and arcs show the direction of data transmission. Each of the processor units, mutually connected through the switch, executes a local section of the program. The processor units work in parallel and the necessary synchronization between sections of the program is carried out by means of the data transmit through the switch. Parallelism is achieved by the partition of the program during translation into separate linked sections, which leads to a waste of time and adecrease in device performance. Thus, device performance depends greatly on the programming system capability to segregate sections (sub-programs), which are weakly linked to one another. in the original program and is quite time-consuming on the user (programmer) side.

These disadvantages do not allow the full internal parallelism of the programs in execution to be realized in this device and as a result do not achieve high performance based on this parallelism and the data flow principle.

The invention explanation.

The invention is based on the problem of creating a computer system which would achieve increased performance by means of simultaneous access of each processor unit to the entire program in execution and through automation of the process of computational means distribution.

The problem is solved this way. The computer system contains a switch, N processor units, a second informational output and a third informational input. The first control output and address output of the i-th processor unit (i=1...N) are connected correspondingly with the i-th input of the first group of switch control inputs and with the i-th input of the group of switch address inputs. The first and second informational outputs of the i-th processor unit are connected with the corresponding input of the group of switch informational inputs. The first informational, address, and control inputs and the second informational, address, and control inputs of the i-th processor

unit are connected with the first and second informational inputs of the system. The first control input of the system is connected with the control input of the switch and with third control input of the i-th processor unit. The control output of the switch 2 is connected with the fourth control input of the i-th processor unit. The third informational output of the i-th processor unit is connected with the first informational output of the system.

According to the invention,

1. The computer system contains an auxiliary switch, N modules of associative memory and a buffering block. The first control, first informational, second control and second informational outputs of the i-th group of exchange outputs of the auxiliary switch are connected correspondingly with the fifth control, third informational, sixth control and fourth informational inputs of the i-th processor unit. The first group of control outputs of the auxiliary switch is connected with the first group of control inputs of the buffering block. The second group of control outputs of the auxiliary switch is connected with the second group of control inputs of the buffering block. The control inputs of the auxiliary switch and of the buffering block and the first control input of each module of associative memory are connected with the control input of the system. The i-th inputs of the first and second groups of control inputs of the auxiliary switch are connected correspondingly with the second and third control outputs of the i-th processor unit. The seventh and eighth control inputs of the i-th processor unit are connected correspondingly with the i-th outputs of the first and second groups control outputs of the buffering block. The third group of control outputs and the first group of the informational outputs of the buffering block are connected correspondingly with the third group of control inputs and the first group of informational inputs of the auxiliary switch. The second group of informational outputs of the buffering block is connected with the second informational output of the system. The fourth

group of control inputs of the auxiliary switch is connected with the fourth group of control outputs of the buffering block. The i-th input of the first group of informational inputs of the buffering block is connected with the fourth and fifth informational outputs of the i-th processor unit. The fourth control output of i-th processor unit is connected with the i-th input of the third group of control inputs of the buffering block. The third group of informational outputs of the buffering block is connected with the second group of informational inputs of the auxiliary switch. The first control output of the i-th module of associative memory is connected with the i-th input of the second group of control inputs of the switch. The i-th output of the group of informational outputs of the switch is connected with the informational input of the i-th module of associative memory. The informational and the second control outputs of the i-th module of associative memory are connected with the i-th inputs of the second group of informational inputs and the fourth group of control inputs of the buffering block. The third group of informational inputs of the buffering block is connected with the third informational input of the system. And, the i-th output of the group of control outputs of the switch is connected with the second control input of the i-th module of associative memory.

2. Each processor unit, according to the invention, may contain the first and second switches, the first and second control units, an executive device for instruction processing and an executive device for operand processing. The first and second control inputs of the first switch are connected with the first and second control outputs of the first control unit of control. The third control output of the first control unit is connected with the first control input of the executive device for instruction processing. The first and the second control outputs of the second control unit are connected with the first and second control inputs of the second switch. The first informational input of the second switch is connected with the address output of the executive

device for instruction processing, the first informational output of the executive device for instruction processing is connected with the second informational input of the second switch and the first informational input of the first switch. The second informational output of the executive device for instruction processing is connected with the second informational input of the first switch and the third informational input of the second switch. The first control output of the executive device for instruction processing is connected with the first control input of the first control unit. The fourth control output of the first control unit is connected with the first control input of the executive device for operand processing. The first control output of the executive device for operand processing is connected with the second control input of the first control unit. The first control input of the second control unit is connected with the second control output of the executive device for operand processing. The second control output of the executive device for instruction processing is connected with the second control input of the second control unit. The second control input of the executive device for instruction processing is connected with the third control output of the second control unit. The fourth control output of the second control unit is connected with the second control input of the executive device for operand processing. The fourth informational input of the second switch is connected with the address output of the executive device for operand processing. The first informational output of the executive device for operand processing is connected with the fifth informational input of the second switch and the third informational input of the first switch. The second informational output of the executive device for operand processing is connected with the fourth informational input of the first switch and with the sixth informational input of the second switch. The first, second and third informational outputs of the second switch are the address output, the first informational output and second informational output of the processor unit respectively. The third informational

outputs of the executive device for instruction processing and of the executive device for operand processing are connected with the third informational output of the processor unit. The fourth and fifth informational outputs of the processor unit are respectively the first and second informational outputs of the first switch. The fifth control output of the second control unit is connected with the first control output of the processor unit. The second and third control outputs of the processor unit are the third control outputs of the executive device for instruction processing and of the executive device for operand processing respectively. The fourth control output of the processor unit is connected with the fifth control output of the first control unit. The first informational, address and control inputs of the processor unit are the first informational, address and the third control inputs of the executive device for instruction processing respectively. The second informational, address and control inputs of the processor unit are connected correspondingly with the first informational, address and the third control inputs of the executive device for operand processing. The fourth control input of the executive device for operand processing and the fourth control input of the executive device for instruction processing are connected with the third control input of the processor unit. The fourth control input of the processor unit is connected with the third control input of the second control unit. The third informational input of the processor unit is the second informational input of the executive device for instruction processing. The fifth control input of the executive device for instruction processing is the fifth control input of the processor unit. The fourth informational and the sixth control inputs of the processor unit are connected with the second informational and the fifth control inputs of the executive device for operand processing respectively. And, the seventh and eighth control inputs of the processor unit are connected with the third and fourth control inputs of the first control unit respectively.

3. The auxiliary switch, according to the invention, may contain the first and second control units and the first and second switching units. The first groups of the control outputs of the first and second control units are connected with the first and second groups of the control outputs of the auxiliary switch respectively. The first and second control outputs of the i-th group of exchange outputs of the auxiliary switch are connected with the i-th outputs of the second group of the control outputs of the first and second control units respectively. The control inputs of the first and second control units are connected with the control input of the auxiliary switch. The first and second groups of the informational inputs of the auxiliary switch are connected with the groups of the informational inputs of the first and second switching units respectively. The i-th outputs of the group of the informational outputs of the first and second switching units are connected correspondingly with the first and second informational outputs of the i-th group of the exchange outputs of the auxiliary switch. The first and second groups of the control inputs of the auxiliary switch are connected with the first groups of the control inputs of the first and second control units respectively. The groups of the control outputs of the first and second switching units are connected correspondingly with the second groups of the control inputs of the first and the second control units. The third groups of the control inputs of the first and the second control units are connected correspondingly with the third and fourth groups of the control inputs of the auxiliary switch. And, the third groups of the control outputs of the first and second control units are connected with the first groups of the control inputs of the first and second switching units respectively. The second group of the control inputs of each of these units is connected correspondingly with the fourth group of the control outputs of the first and second control units.

4. The buffering block, according to the invention, may contain the group of buffering units. The first, second and third control outputs of the i-th buffering unit are connected with the i-th outputs of the first, second and third groups of the control outputs of the buffering block respectively. The i-th inputs of the first and second groups of the control inputs of the buffering block are connected with the first and second control inputs of the i-th buffering unit respectively. The fourth control output of the buffering unit is connected with the i-th output of the fourth group of the control outputs of the buffering block. The control input of the buffering block is connected with the third control input of each of the buffering units. The i-th inputs of the third and fourth groups of the control inputs of the buffering block are connected with the fourth and fifth control inputs of the i-th buffering unit respectively. The first, second and third informational outputs of the buffering units are connected correspondingly with the i-th outputs of the first, second and third groups of the informational outputs of the buffering block. The i-th inputs of the first, second and third groups of the informational inputs of the buffering block are connected with the first, second and third informational inputs of the i-th buffering unit respectively.

The brief description of drafts (figures)

Further on the invention is illustrated by an example of its application and attached drafts, where :

Fig.1 represents the functional diagram of the computer system;

Fig.2 represents the functional diagram of the computer system processor unit;

Fig.3 represents the functional diagram of the control unit of the first switch of the processor unit;

Fig.4 represents the functional diagram of the control unit of the second switch of the processor unit;

Fig.5 represents the functional diagram of the executive device for instruction processing;

Fig.6 represents the functional diagram of the control unit of the executive device for instruction processing of the processor unit;

Fig.7 represents the functional diagram of the switching block of the executive device for instruction processing;

Fig.8 represents the functional diagram of the control unit of the switching block of the executive device for instruction processing;

Fig.9 represents the functional diagram of the input register unit of the executive device for instruction processing;

Fig.10 represents the functional diagram of the instruction register unit of the executive device for instruction processing;

Fig.11 represents the functional diagram of the executive device for operand processing of the processor unit;

Fig.12 represents the functional diagram of the control unit of the executive device for operand processing;

Fig.13 represents the functional diagram of the input register unit of the executive device for operand processing;

Fig.14 represents the functional diagram of the output register unit of the executive device for operand processing;

Fig.15 represents the functional diagram of the computer system auxiliary switch;

Fig.16 represents the functional diagram of the auxiliary switch control unit;

Fig.17 represents the functional diagram of the auxiliary switch switching unit;

Fig.18 represents the functional diagram of the auxiliary switch query forming control unit;

Fig.19 represents the functional diagram of the switching control block of the auxiliary switch control unit;

Fig.20 represents the functional diagram of the switching priority control unit of the switching control block of the auxiliary switch control unit;

Fig.21 represents the functional diagram of the input query unit of the switching control block of the auxiliary switch control unit;

Fig.22 represents the functional diagram of the transforming-receiving unit of the auxiliary switch switching unit

Fig.23 represents the functional diagram of the transforming-transmitting unit of the auxiliary switch switching unit;

Fig.24 represents the functional diagram of the computer system buffering block;

Fig.25 represents the functional diagram of the buffering unit of the buffering block;

Fig.26 represents the functional diagram of the buffering unit buffer;

Fig.27 represents the functional diagram of the buffering control unit of the buffer unit;

Fig.28 represents the functional diagram of the computer system associative memory module;

Fig.29 represents the functional diagram of the computer system switch;

Fig.30 represents the functional diagram of the computer system switch control unit;

Fig.31 represents the functional diagram of the transmitting control unit of the computer system switch control unit;

Fig.32 represents the functional diagram of the receiving control unit of the computer system switch control unit;

Fig.33 represents the functional diagram of the switching control unit of the computer system switch control unit;

Fig.34 represents the general appearance of computation graph;

Fig.35 represents the informational package structure.

The best way to implement the invention.

The computer system (Fig.1) contains a group of processor units **1-1...1-N**, a switch **2**, an auxiliary switch **3**, a group of associative memory modules **4-1...4-N** and a buffering block **5**.

The computer system also contains the first, second and third informational inputs **6**, **7** and **8**, control input **9**, the first and second informational outputs **10-11** and memory zeroizing input **12**.

Each processor unit **1-i** contains the first, second, third and fourth informational inputs **13**, **14**, **15** and **16**, the first and second address inputs **17-1** and **17-2**, the first to the eighth control inputs **18-1...18-8** respectively, the first to the fourth control outputs **19-1...19-4**, an address output **20** and the first to the fifth informational outputs **21-1...21-5**.

Auxiliary switch **3** contains control input **22**, the first to the fourth groups of control inputs **23-1...23-N**, **24-1...24-N**, **25-1...25-N**, **26-1...26-N**, the first and second groups of informational inputs **27-1-1...27-1-N** and **27-2-1...27-2-N**, the first and the second groups of control outputs **28-1...28-N** and **29-1...29-N**; N groups of exchange outputs, each of which includes the first control, first informational, the second control and the second informational outputs **30-1-i**, **30-2-i**, **30-3-i**, and **30-4-i** respectively.

Buffering block 5 contains control input 31, the first and the second groups of control inputs 32-1...32-N and 33-1...33-N, the first group of informational inputs 34-1...34-N, the third group of control inputs 35-1..35-N, the second group of informational inputs 36-1...36-N, the fourth group of control inputs 37-1...37-N, and the third group of informational inputs 38-1...38-N. Buffering block 5 also contains the first to the third groups of control outputs 39-1...39-N, 40-1...40-N, 41-1...41-N, the first and the second groups of informational outputs 42-1...42-N and 43-1...43-N, the fourth group of control outputs 44-1...44-N and the third group of informational outputs 45-1...45-N.

Each associative memory module 4-i contains first control input 46, zeroizing input 47, informational input 48, second informational input 49, first control output 50, informational output 51 and second control output 52.

Switch 2 contains control input 53, the first group of control inputs 54-1...54-N and the group of address inputs 55-1...55-N. Switch 2 also contains the second group of control inputs 56-1...56-N, the group of informational inputs 57-1...57-N, control output 58, the group of informational outputs 59-1...59-N and the group of control outputs 60-1...60-N. The synchronization and energy supply chains are not shown.

Each processor unit 1-i (Fig.2) includes the first and the second switches 61 and 62, the first and the second switch control units 63 and 64 for the first and the second switches respectively, executive device for instruction processing 65 and executive device for operand processing 66.

Switch 61 contains the first and the second control inputs 67-1 and 67-2, the first to the fourth informational inputs 68-1, 68-2, 69-1, 69-2, and the first and the second informational outputs, connected with the outputs 21-4 and 21-5 of the processor unit.

Switch 62 contains the first and the second control inputs 70-1 and 70-2, the first to the sixth informational inputs 71-1, 71-2, 71-3, 72-1, 72-2, 72-3, and the first to the third informational outputs, connected with the outputs 20, 21-1, 21-2 of the processor unit respectively.

First switch control unit 63 contains the first and the second control inputs 73, 74, the first to the fourth control outputs 75-1, 75-2, 76-1, 76-2, the third and the fourth control inputs which are connected with inputs 18-7 and 18-8 of the processor unit, and the fifth control output which is connected with output 19-4 of the processor unit.

Second switch control unit 64 contains the first and the second control inputs 77 and 78, the first to the fourth control outputs 79-1, 79-2 and 80-1, 80-2, the third control input which is connected with input 18-4 of the processor unit, and the fifth control output which is connected with output 19-1 of the processor unit.

Executive device for instruction processing 65 includes the first and the second control inputs 81 and 82, the first and the second control outputs 83 and 84, the third control output 85, address output 86, the first and the second informational outputs 87 and 88, the third informational output which is connected with the output 21-3 of the processor unit, the first and the second informational inputs which are connected with inputs 13 and 15 of the processor unit respectively, the third to the fifth control inputs which are connected with inputs 18-1, 18-3, and 18-5 of the processor unit respectively, and an address input connected with input 17-1 of the processor unit.

Executive device for operand processing 66 contains the first and the second control inputs 89 and 90, the first to the third control outputs 91, 92, 93, address output 94, the first and the second informational outputs 95 and 96, the third informational output which is connected with the output 21-3 of the processor unit, the first and the second informational inputs which are

connected with inputs 14 and 16 of the processor unit respectively, the third to the fifth control inputs which are connected with inputs 18-2, 18-3, and 18-6 of the processor unit respectively, and an address input connected to input 17-2 of the processor unit.

Each switch control unit 63 (Fig.3) and 64 (Fig.4) contains "AND" elements 97 and 98, "OR" element 99 and priority coder 100.

Executive device for instruction processing 65 (Fig.5) contains control unit 101, output switch 102, switching block 103, instruction register unit 104, instruction memory 105, arithmetic-logical unit (ALU) 106, loading switch 107 and input register unit 108.

Control unit 101 contains input 109-1 for zeroizing, the first and the second inputs 109-2 and 109-3 for control of result transmission, starting control input 109-4, input 109-5 for instruction type bits, input 109-6 for memory readiness signal, input 109-7 for the ALU result significance signal, input 109-8 for the ALU readiness signal, input 109-9 for the instruction code, the first and the second outputs 110-1 and 110-2 for the data readiness signal, output 110-3 for the control of field switching, output 111-4 for the control of data reception, ALU starting control output 111-5 and output 111-6 for the control of instruction retrieval.

Output switch 102 contains the first and the second control inputs 112-1 and 112-2, the first and the second informational inputs 112-3 and 112-4 and an informational output connected with the outputs 86 and 88 of the executive device 65.

Switching block 103 contains control inputs 113-1...113-12, informational inputs 114-1...114-10 and 115-1...115-4, and informational outputs connected with the output 87 of executive device 65 and with inputs 112-3 and 112-4 of switch 102.

Instruction register unit 104 contains informational input 116-1, control input 116-2, and informational outputs connected with the inputs 115-1...115-4 of block 103.

The instruction memory **105** contains load control input **117-1**, informational input **117-2**, address input **117-3**, reading control input **117-4**, and informational and control outputs connected with the corresponding inputs **116-1** and **116-2** of the instruction register unit and with the corresponding inputs **109-5** and **109-6** of the control unit **101**.

Arithmetic-logical unit (ALU) **106** (made analogously to the device SU 1367012) contains instruction control input **118-1**, first and second operand inputs **118-2** and **118-3**, starting control input **118-4**, first and second informational outputs **119-1** and **119-2**, and control output **119-3**.

Loading switch **107** contains first and second informational inputs **120-1** and **120-2**, first and second control inputs **120-3** and **120-4**, and an informational output connected with address input **117-3** of instruction memory **105**.

Input register unit **108** contains control input **121-1**, informational outputs **122-1...122-11**.

Control unit **101** (Fig.6) contains "AND" elements **123** and **124**, priority coder **125**, "AND" elements **126...133**, "OR" elements **134...136**, decoder **137**, "AND" elements **138...140**, "OR" elements **141** and **142**, "AND" elements **143...145**, control triggers **146...151**, "AND" elements **152...157**, "OR" element **158**, and "AND" elements **159** and **160**.

Switching block **103** (Fig.7) contains registers **161...171**, control unit **172**, and switches **173...178**.

Control unit **172** (Fig.8) contains "OR" elements **179...190**, control inputs **191...202**, and control outputs **203...222**.

Input register unit **108** (Fig.9) contains status word register **223**, first data word register **224** and second data word register **225**.

Instruction register unit **104** (Fig.10) contains first and second operation code registers **226** and **227**, and first and second instruction number registers **228** and **229**.

Executive device 66 (Fig.11) contains control unit 230, output switch 231, output register unit 232, instruction memory 233, ALU 234, loading switch 235 and input register unit 236.

Control unit 230 contains zeroizing input 237-1, first and second inputs for result transmission 237-2 and 237-3, starting control input 237-4, input for instruction type bits 237-5, input for the memory readiness signal 237-6, input 237-7 for the data significance signal, input 237-8 for the ALU readiness signal, first and second outputs for the control of output switching 238-1 and 238-2, output for transmission control 238-3, output for reception control 238-4, output for starting control 238-5, and the first to the third control outputs connected with the outputs 91...93 of the executive device 66.

Output register unit 232 contains control inputs 239-1, 239-2 and 239-3, informational inputs 239-4, 239-5 and 239-6, and informational outputs 240-1, 240-2 and 240-3.

Switch 231 contains an informational output connected with outputs 94 and 96 of executive device 66, first and second control inputs connected with outputs 238-1 and 238-2 of unit 230, and first and second informational inputs connected with outputs 240-2 and 240-3 of output register unit 232.

Instruction memory 233, ALU 234 and loading switch 235 are analogous to the corresponding devices 105, 106 and 107 in executive device 65.

Input register unit 236 contains control and informational inputs 241-1 and 241-2, and informational outputs 242-1...242-5.

Control unit 230 (Fig.12) contains "OR" elements 243-1 and 243-2, "AND" elements 244-1...244-4, "AND" elements 245-1 and 245-2, "OR" element 246, "AND" elements 247-1 and 247-2, "OR" element 248, priority coder 249, "AND" elements 250-1 and 250-2, "AND"

element 251, triggers 252-1...252-3 and 253-1...253-3, "AND" elements 254-1...254-6, "OR" element 255, and "AND" element 256.

Input register unit 236 (Fig.13) contains registers 257, 258-1 and 258-2 for the status word bits of the first and the second operands.

Output register unit 232 (Fig.14) contains result register 259, first and second registers of instruction number and operation code 260-1 and 260-2, and status attribute register 261.

Auxiliary switch 3 (Fig.15) contains first and second control units 262-1 and 262-2, and first and second switching units 263-1 and 263-2.

Each control unit 262-1 and 262-2 contains control input 264; the first to the third groups of control inputs 265-1...265-N, 266-1...266-N, 267-1...267-N respectively; and the first to the fourth groups of control outputs 268-1...268-N, 269-1...269-N, 270-1-1...270-N-N and 271-1...271-N.

Each switching unit 263-1 and 263-2 contains the first and the second groups of control inputs 272-1-1...272-N-N and 273-1...273-N, a group of informational inputs 274-1...274-N, a group of informational outputs 275-1...275-N, and a group of control outputs 276-1...276-N.

Each control unit 262-1 and 262-2 (Fig. 16) contains a group of readiness signal formation triggers 277-1...277-N, readiness set control unit 278 and switching control block 279.

Readiness set control unit 278 contains N pairs of first and second control outputs 280-1-1 and 280-2-1 to 280-1-N and 280-2-N, zeroizing input 281, the first to the third groups of control inputs 282-1...282-N, 283-1...283-N, and 284-1...284-N, N groups of outputs 285-1-1...285-1-N to 285-N-1...285-N-N of bits for channel number switching, and N groups of inputs 286-1-1...286-1-N to 286-N-1...286-N-N of bits for channel number switching.

Switching control block 279 contains N groups of outputs 287-1-1...287-1-N to 287-N-1...287-N-N of the switching channel number set, the first and the second groups of control outputs 288-1...288-N and 289-1...289-N, zeroizing input 290, N pairs of first and second control inputs 291-1-1 and 291-2-1 to 291-1-N and 291-2-N, a group of control inputs 292-1...292-N, N groups of control outputs 293-1-1...293-1-N to 293-N-1...293-N-N of the switching elements, N groups of inputs 294-1-1...294-1-N to 294-N-1...294-N-N of the switching channel set, and the third group of control outputs 295-1...295-N.

Each switching unit 263-1 (263-2) (Fig. 17) contains high frequency impulse generator 296, a group of output registers 297-1...297-N, a group of transforming-transmitting units 298-1...298-N, a group of "OR" elements 299-1...299-N, a group of photo-receivers 300-1...300-N, the first group of the optical lens rasters 301-1...301-N, controlled optical transparency 302, the second group of optical lens rasters 303-1...303-N, a group of deflectors 304-1...304-N, a group of laser oscillators 305-1...305-N, a group of transforming-transmitting units 306-1...306-N, and a group of input registers 307-1...307-N.

Each transforming-transmitting unit 298-i contains control output 308, informational outputs 308-1...308-N of parallel code, first and second control inputs 309-1 and 309-2, and informational input of serial code 309-3.

Each transforming-transmitting unit 306-i (Fig. 23) contains informational output of serial code 310, control input 311, a group of inputs of transforming control 311-1...311-N and a group of informational inputs of parallel code 312-1...312-N.

Readiness set control unit 278 (Fig. 18) contains first group of "OR" elements 313-1...313-N, group of "AND" elements 314-1..314-N, second group of "OR" elements 315-1...315-N, a group of registers 316-1...316-N, and third group of "OR" element 317-1...317-N.

Switching control block 279 (Fig. 19) contains N groups of double-input "AND" elements 318-1-1...318-1-N to 318-N-1...318-N-N, N groups of N-input "AND" elements 319-1-1...319-1-N to 319-N-1...319-N-N, N groups of triggers 320-1-1...320-1-N to 320-N-1...320-N-N, priority control unit 321 and input query receiving unit 322.

Priority control unit 321 contains zeroizing input unit 323, the first to the fourth groups of control outputs 323-1-1...323-1-N, 323-2-1...323-2-N, 323-3-1...323-3-N and 323-4-1...323-4-N, N groups of inputs 324-1-1...324-1-N to 324-N-1...324-N-N of output channel sampling control, and the first to the third groups of control inputs 325-1-1...325-1-N, 325-2-1...325-2-N, 325-3-1...325-3-N.

Priority control unit 321 (Fig. 20) contains the first and the second priority coders 326 and 327, "OR" element 328, the first and the second groups of status triggers 329-1...329-N and 330-1...330-N, the first group of "OR" elements 331-1...331-N, a group of query triggers 332-1...332-N, the first group of "AND" elements 333-1...333-N, the second and the third groups of "OR" elements 334-1...334-N and 335-1...335-N, and the second group of "AND" elements 336-1...336-N.

Input query receiving unit 322 (Fig. 21) contains a group of control inputs connected with inputs 291-2-1...291-2-N of the switching control block 279, N groups of inputs of output channel number bits connected with inputs 294-1-1...294-N-N of the switching control block 279, and a group of control outputs connected with inputs 325-1-1...325-1-N of priority control unit 321.

The unit 322 (Fig. 21) contains a group of switches 337-1...337-N and a group of decoders 338-1...338-N.

Each of the transforming-transmitting units **298-i** (Fig. 22) contains decoder **339**, counter **340**, "OR" element **341** and amplifier-former **344**, coder **345**, counter **346** and "AND" element **347**.

Each buffering block **5** (Fig. 24) contains group of buffering units **348-1...348-N**.

Each buffering unit **348-i** (Fig. 25) contains the first to the fourth control outputs **349-1...349-4**, the first to the third informational outputs **349-5...349-7**, the first and second control inputs connected with the corresponding inputs of the first and second groups of control inputs **32-1...32-N** and **33-1...33-N**, the third control input connected with control input **31**, the fourth and fifth control inputs connected with the corresponding inputs of the third and the fourth groups of control inputs **35-1...35-N** and **37-1...37-N**, and the first to the third informational inputs connected with the corresponding inputs of the first, the second and the third groups of informational inputs **34-1...34-N**, **36-1...36-N** and **38-1...38-N**.

Each buffering unit **338-i** contains the first and the second buffers **350-1** and **350-2**. The buffer **350-1** is used for temporary storage and transmission of the instruction words, and the buffer **350-2** is used for temporary storage and transmission of operand packets. Both buffers have the same structure and configuration, being different only in internal logic of means of identification of input packet type.

Each buffer **350-1** and **350-2** (Fig. 26) contains the first and the second control inputs **351-1** and **351-2**, the first and the second informational inputs **351-3** and **351-4**, the third and the fourth control inputs **351-5** and **351-6**, input of external exchange **351-7**, the first and the second outputs of transmission control **352-1** and **352-2**, informational output **352-3**, and output of external exchange **352-4**.

Each buffer 350-1 and 350-2 contains output switch 353, group of "OR" element 353-1...353-5, group of "AND" elements 354-1...354-4, the register memorizing unit (RMU) 355 and the corresponding control unit 356-1 (356-2), input switch 357, the first and the second input registers 358-1 and 358-2.

Each control unit 356-1 and 356-2 contains control outputs 359-1...359-12, zeroizing input 360-1, the first input of packet code 360-2, the first control input of receiving 360-3, the second input of packet code 360-4, the second and the third control inputs of receiving 360-5 and 360-6, and the first to the fifth control inputs 361-1...361-5.

Each of the control units 356-1 and 356-2 (Fig.27) contains priority coder 362, counters 362-1 and 362-2, logical "AND" elements 363-1...363-4, triggers 364-1...364-3 and the corresponding group of decoders 365-1-1...365-1-3 (or 365-2-1...365-2-3). The mentioned groups of decoders carry out the function of identification of input packet type and they are different only in the functioning of the inner logic: the group of decoders 365-1-1...365-1-3 is used for identification of the instruction words packets, and the group of decoders 365-2-1...365-2-3 is used for identification of the operand packets.

Each associative memory module 4-i (Fig.28) contains buffer register 366 and associative memorizing unit (AMU) 367, built in analogy with the device (RU, 2035069).

AMU 367 contains the first and the second informational outputs 368-1 and 368-2, the first and the second control outputs 369 and 370, the first to the third control inputs 371-1...371-3, and the first and the second informational inputs 372-1 and 372-2.

The switch 2 (Fig.29) contains control unit 373 and switching unit 374, built in analogy with the switching unit 263-1 (263-2) included into the auxiliary switch 3.

The control unit 373 contains the exchange control output 375, a group of control outputs 375-1...375-N, the first to the N-th groups of outputs 376-1-1...376-1-N to 376-N-1...376-N-N of the channel switching control, the receiving control output 377, zeroizing input 378, and the first to the N-th groups of inputs. Each of the first to the N-th groups of inputs contains control input 378-1-i, address input 378-2-i, and the first and the second groups of control inputs 379-1...379-N and 380-1...380-N.

The switching unit 374 contains a group of informational outputs 381-1...381-N, a group of informational inputs 382-1...382-N, the first to the N-th groups of inputs 383-1-1...383-1-N to 383-N-1...383-N-N of switching control, a group of control outputs 384-1...384-N and a group of inputs 385-1...385-N of receiving control.

The control unit 373 (Fig.30) contains a group of input query forming triggers 386-1...386-N, transmission control unit 387, receiving control unit 388, switching control unit 389, a group of query receiving triggers 390-1...390-N, a group of decoders 391-1...391-N, a group of input registers 392-1...392-N and a group of "AND" elements 393-1...393-N.

The transmission control unit 387 contains the first to the N-th groups of control outputs, each of which contains the first and the second query set outputs 394-1-i and 394-2-i, zeroizing input 395, the first to the N-th groups of query control inputs 396-1-1...396-1-N to 396-N-1...396-N-N, the first and the second groups of control inputs 397-1...397-N and 398-1...398-N.

The receiving control unit 388 contains the first control output 399, a group of receiving control outputs 399-1...399-N, the second control output 400, and the first to the N-th groups of inputs. Each of the first to the N-th groups of inputs contains the first and the second inputs of status transmission 401-1-i and 401-2-i, a group of control inputs 402-1...402-N, zeroizing input

403, and the first to the N-th groups of resetting control inputs 404-1-1...404-1-N to 404-N-1...404-N-N.

The switching control unit 389 contains the first to the N-th groups of control outputs 405-1-1...405-1-N to 405-N-1...405-N-N, the first to the N-th groups of priority control inputs 406-1-1...406-1-N to 406-N-1...406-N-N, and a group of control inputs 407-1...407-N.

The transmission control unit 387 (Fig.31) contains the first group of "OR" elements 408-1...408-N, a group of "AND" elements 409-1...409-N, and the second group of "OR" elements 410-1...410-N.

The receiving control unit 388 (Fig.32) contains trigger 411, a group of "OR" elements 411-1...411-N, the first and the second "OR" elements 412-1 and 412-2, the first to the N-th groups of "AND" elements 413-1-1...413-1-N to 413-N-1...413-N-N, and "AND" elements 414, 415-1 and 415-2.

The switching control unit 389 (Fig.33) contains a group of priority coders 416-1...416-N and the first to the N-th groups of "OR" elements 417-1-1...417-1-N to 417-N-1...417-N-N.

The principles of computational organization under data flow control assume that the algorithm of the problem solution is represented as a graph of the computation process, consisting of operations (instructions) on data (operands) and links (directions) by which the data (results) are transmitted from one to another instruction (Fig.34).

Data processing according to the graph is carried out as the data prepared for processing appear at the instruction inputs. The completion of pairs of data related to a particular instruction is performed in the memory, which seeks for them by a key. A key, generally, is a code, consisting of instruction number bits, an index, an iteration and so on. The best operational realization of such memory, considering volume and speed, would be based on the utilization of

optical elements, and considering an increase in performance, it would be optimal to break its whole volume into separate modules.

Each instruction has a number K-i which can be used to place it in the command memory, a code of operation (COP-i), and a "destination address" K-j to which the result of processing is related.

Furthermore, an instruction has attributes, determining the conditions of its processing or its type. An instruction can be double-input or single-input, depending on how many operands (one or two) it processes, which is determined by the operation code. An instruction can be double-address or single-address, depending on the number of destinations (to the input of how many instructions) to which its result is transmitted. For example, the instruction K-1 (Fig.34) is a single-input, double-address instruction; the instruction K-4 is double-input, single-address instruction; and the instructions K2 and K-3 are single-address, single-input instruction.

The operation, determined by the COP of a given instruction, can be carried out with numeric data (operands) and with supplementary data (instruction words). The first functional group of instructions is performed by arithmetic operations (operand processing operations), and the second group by the instruction word processing operations.

In order to organize the graph processing, instructions and data are represented as informational objects consisting of multi-bit words, where the corresponding groups of bits form the fields with the necessary functional assignment (Fig. 35).

Information processing is carried out by executive devices of two different types, which receive the information in the form of operand packets and instruction words packets. Generally a packet includes a status word and two data words, which either are operands or contain

supplementary data. A packet of a single-input instruction contains a status word and only one data word.

A status word contains the following basic groups of the functional bits (fields):

COP - code of operation;

K - number of instruction;

G - number of generation;

T- number of iteration;

I - index.

The functional fields of a status word can de used in different ways. In particular, the key group of bits for data seeking in the associative memory modules is determined by the fields K, G, T, I. The field COP also may contain bits indicating the instruction type (single- or double-address, single- or double-input) and the packet type (packet of instruction words or packet of operands).

If an instruction has two outputs, then its processing result will be accompanied by two status words, which means two destinations of its transmission.

Bit groups of attributes, determining the type of destination instruction, are stored in command memory and are retrieved with its number and code of operation.

The computer system (Fig. 1) runs the program, which is loaded through the first and the second informational inputs 6 and 7, and returns the result of processing through the second informational output 11. The system realizes its own parallelism of the computational process, represented by the graph, processing simultaneously all the prepared instructions. In the command memory 105 and 233 for the executive devices 65 and 66 of each of the processor units 1-i, all the instructions of the program being executed are stored. The memory 105 contains

all the instructions for the instruction word processing, and the memory 233 contains all the instructions for the operand processing.

Instruction loading (Fig. 5 and 11) is carried out through the first and the second informational inputs 13 and 14 and the loading switches 107 and 235 respectively, for the executive devices 65 and 66.

The system is started by the transmitting to the third input 8 starting packets of instruction words and operands from an external (not shown on Fig. 1) system.

The starting packets with the corresponding control signals are transmitted to the inputs of the third group of informational inputs 38-1...38-N of the buffering block 5. The total number of inputs used will be determined by the starting conditions of a particular program.

The buffering block 5 is used to smooth peaks of the input queries on the inputs of the auxiliary switch 3. The use of the buffering block 5 in the starting process is its additional function.

Starting packet bits are transmitted to the informational input of the buffering unit 348-i, which, in this case, conducts the starting functions, and further on to the external exchange input 351-7 of the buffers 350-1 and 350-2 (Fig. 25). From the buffers 350-1 and 350-2, they are transmitted to the fourth informational input of the output switch 353 (Fig. 26). The switching in the output switch 353 is controlled through its fourth control input, to which the corresponding signal is transmitted from the control output 359-12 of the control unit 356-1 (356-2) through the "AND" element 354-4. This control signal is formed (Fig. 27) at the output of the decoder 365-1-3 (365-2-3), to the input of which the coded bit group determining the type of the starting packet is transmitted. Depending on the type of the starting packet, the switch 353 control signal will be

formed either in the buffer **350-1** (for instruction word receiving) or in the buffer **350-2** (for operand receiving).

If the starting packet contains operands, then the bits of the packet from the output **352-3** of the buffer **350-2** are transmitted (through the second informational output of the unit **348-i** and the i-th output of the third group of the informational outputs **45-1...45-N** of the buffering block **5**) to the i-th input of the second group of the informational inputs **27-2-1...27-2-N** of the auxiliary switch **3**.

The information on the i-th output of the third group of the informational outputs **45-1...45-N** of the buffering block **5** is accompanied by strobe of the transmission (signal of "significance"), which is a control signal of an exchange query, and is transmitted from the i-th output of the fourth group of the control outputs **44-1...44-N** of the buffering block **5** to the i-th input of the fourth group of the control inputs **26-1...26-N** of the auxiliary switch **3**.

The main function of the auxiliary switch is to distribute all received packets over its free outputs.

Transmission strobe and the bits of the operand packets, transmitted respectively to the i-th inputs of the fourth group of control inputs **26-1...26-N** and to the i-th inputs of the second group of the informational inputs **27-2-1...27-2-N** of the auxiliary switch, are transmitted to the query inputs **265-i** and the informational input **274-i** respectively, the executive device **262-2** and the switching unit **263-2** (Fig. 15, 16, 17).

The operand packet bits, transmitted to the input **274-i** of the switching unit **263-2**, are received by the input register **307-i**. The signal of receiving control is formed at the output **271-i** of the control unit **262-2**.

The switching, including the transmission of packet bits from the input **264-i** of the switching unit **263-2** to its informational output **275-j**, corresponding to the first free output register from the group **297-1...297-N** is carried out with the help of the dimensional optical system.

From the output of the register **307-i** the parallel code of the packet bits is transmitted to the inputs **312-1...321-N** of the transforming-transmitting unit **306-i**. The serial code formed on its output **310** is transmitted to the laser oscillator **305-i**. The laser signal corresponding to the serial code (through the optical system, which includes the controlled deflector **304-i**, a group of optical lens rasters **303-1...303-N**, controlled optical transparency **302** and a group of optical lens rasters **301-1...303-N**) is transmitted to the input of photo-receiver **300-j**, from the output of which the serial code of the input packet is transmitted to the informational input **309-3** of the transforming-transmitting unit **298-j**. On the outputs of the register **297-j** a parallel code is formed which corresponds to the bit groups of the packet on the input **274-i** of the switching unit **263-2**, and on the output **308** of the unit **298-j** a signal is formed which determines the end of the output parallel code forming.

The switching unit **263-2** (Fig. 17) provides the information transmission from any input **274-1...274-N** to any output **275-1...275-N**, determined by a free register from the register group **297-1...297-N**, which means "free address" switching regime. The signals controlling the corresponding information transformation and switching of dimensional optical net are transmitted to the inputs **272-1-1...272-N-N** of the switching unit **263-2** from the outputs **270-1-1...270-N-N** of the control unit **262-2** (Fig. 15).

The forming of the signals mentioned (Fig. 16, 19, 20) is carried out in the switching control block **279** when the strobe of transmission is transmitted on its input **292-i** from the input **265-i** of the control unit **262-2**. To the output **269-j** of the control unit **262-2** (Fig. 16) the strobe of the

packet transmission is transmitted which is formed at the trigger **277-j** of the group of the readiness signal forming triggers.

The instruction words packet transmission is carried out in the same way with the use of identical functional structures of the buffering block **5** and the auxiliary switch 3.

The strobe of transmission and the bits of the operand packet respectively through outputs **30-3-j** and **30-4-j** of the auxiliary switch **3** are transmitted to the inputs **18-6** and **16** of the processor unit **1-j** (Fig. 1) and to the corresponding inputs of the executive device **66** (Fig. 2) .

The strobe of transmission through the corresponding input of the executive device **66** is transmitted to the input **237-4** of the control unit **230** (Fig. 11) and the bits of the operand packet are transmitted to the informational input **241-2** of the input register unit **236.**

The reception of functional fields of the operand packet (Fig. 13) by the status word register **257** and the operand registers **258-1** and **258-2** occurs after the reception of the signal of receiving control on the input **241-1** of the input register unit **236.** The bits of the instruction number are transmitted from output **242-1** of the input register unit **236** through the first informational input of the loading switch **235** to the address input of the command memory **233.** The starting control signal is transmitted from output **238-5** of control unit **230** to the retrieval control input of the command memory **233.**

The operation code bits and the operand bits, accompanied by the starting control signal, are transmitted from the outputs **242-2, 242-3** and **242-4** of the input register unit **236** to the corresponding inputs of the ALU **234.** The bits of the functional fields of G, T, I are transmitted to the input **239-6** of the output register unit **232.** The bits of functional fields containing the operation code and the instruction number, for which the result of computations is destined, are

transmitted from the informational output of command memory 233,. to the input 239-5 of the output register unit 232. This result is transmitted to the input 239-4 of the unit 232.

The inputs 239-1, 239-2 and 239-3 of the output register unit 232 receive the corresponding signals which control the reception of the ALU result to the register 259, the bit fields K and COP of the subsequent instruction to the registers 260-1 and 260-2, and the bit fields G, T, I - to the register 261. On the outputs 240-1, 240-2 and 240-3 of the output register unit 232 the functional fields of the result of the current instruction processing (sub-packet) are formed. These fields reflect the principles of computation represented by the computation graph and are transmitted respectively to the first informational input 95 of the executive device 66 and to the informational inputs of the output switch 231. Control signals are transmitted from the outputs 238-1 and 238-2 of the control unit 230 to the control inputs of the output switch 231. The output of the switch 231 is connected with the address output 234 and the second informational output 96 of the executive device 66. The output 94 receives an informational field, corresponding to a group of lower bits of the instruction number, which is placed on the register 260-1 (260-2). This group of bits identifies the number of the associative memory module from the group of modules 4-1...4-N, which allows the sub-packets to be distributed evenly over the associative memory modules. The functions of the output switch 231 are determined by the presence of double-address instructions, i.e. the instructions, the processing result of which is the input operand for two following instructions (having different numbers and operation codes). This condition is realized through having two output registers 260-1 and 260-2 of instructions, the content of which is sequentially transmitted through the switch 231 to the outputs 94 and 96 accompanying the result, which is transmitted to the output 95.

The output switch 231 control signals are formed after the functional fields of the type of instruction and of the strobe of the transmission are transmitted from the informational and control outputs of the command memory 233 to the inputs 237-5 and 237-6 of the control unit 230 respectively. The signal of significance of the result is transmitted from the informational output of the ALU to the input 237-7.

The functional fields of the instruction type include the following attributes: 1A (single-address instruction), 2A (double-address instruction), 1B (single-input instruction), 2B (double-input instruction), which are transmitted (Fig. 12) to the triggers 254-2...254-5. The status of the triggers influences the formation of the control signals on the outputs 238-1 and 238-2 of the control unit 230. The transmission strobes, corresponding to the regimes of the single- or double-input instructions, are formed on the first and the second control outputs 91 and 92 of the executive device 66. And, corresponding to these regimes, bits of the functional fields of the sub-packet are formed on the first and the second informational outputs 95 and 96.

In the single- and double-input instruction regimes, the bits of the sub-packet are transmitted from the outputs 95 and 96 to the outputs 21-4, 21-5 and 21-1 and 21-2 of the j-th processor unit respectively through the switches 61 and 62, which are controlled through the outputs 75-1 and 75-2 of the unit 63 and through the outputs 79-1 and 79-2 of the unit 64. The control signals are formed after the input 74 of the unit 63 and input 77 of the unit 64 receive the strobes of transmission respectively from the outputs 91 and 92 of the executive device 66. Information regarding the number of the associative memory module is transmitted from output 94 of the executive device 66 to the address output 20 of the processor unit only in the double-input instruction regime, since running a single-input instruction does not require seeking for a second operand.

When the result (operand) output from the corresponding executive device is one for a double-input instruction, the search for the pair operand is conducted in an associative memory module. The number of the particular module (further on referred to as "address") is determined by the bit group on the output 20 of the processor unit. Access to the group of associative memory modules 4-1...4-N is realized by means of the switch 2 (Fig. 29).

Here, the j-th inputs of the first group of control inputs, a group of address inputs and the second group of control inputs 54-1...54-N, 55-1...55-N, 57-1...57-N of the switch 2 receive control signals, the number of the memory module and the functional fields of the sub-packet from the outputs 19-1, 20 and 21-1, 21-2 of the j-th processor unit respectively.

The switch 2, which includes control unit 373 and switching unit 374, provides data transmission, unlike the switch 3, to a "fixed" address on the output as determined by the given number k of the associative memory module.

The switching conditions are realized in the control unit 373 (Fig. 30). The inputs 378-1-j and 378-2-j of the control unit 373 receive the corresponding control information from the inputs 54-j and 55-j of the switch 2. Then, the following operations are carried out: the receiving of the address in the register 392-j, the setting of query trigger 390-j, at the k-th output of the decoder 391-j a position code corresponding to the k-th associative memory module is formed and these signals are transmitted to the inputs 407-1...407-N and 406-1-1...406-N-N of the switching control unit 389. The switching control signals are formed at the outputs 405-1-1...405-N-N of the switching control unit 389 and are transmitted to the outputs 376-1-1...376-N-N of the control unit 373.

The mentioned signals are formed at the outputs of priority coders 416-1...416-N (Fig. 33), which play the part of priority schemes, realizing the queuing of queries to each of the associative memory modules.

The control signals from the outputs 376-1-1...376-N-N of the control unit 373 are transmitted to a group of switching control inputs 383-1-1...383-N-N of the switching unit 374 The structure and functioning of switching unit 374 are fully similar to those of the switching units 263-1 and 263-2 of the switch 3. Here, the input 383-j-k of the switching unit 374 receives a signal controlling the k-th input of the j-th deflector from the group 304-1...304-N (Fig.17), and the output 59-k of the switch 2 receives bit fields corresponding to those received at informational input 57-j of the switch 2. The corresponding transmission strobe is formed at the trigger 386-k (Fig. 30) and is transmitted through the output 375-k of the control unit 373 to the output 60-k of the switch 2.

Bits of the functional fields of the sub-packet and the transmission strobe are transmitted from the outputs 59-k and 60-k of the switch 2 to the inputs 48 and 49 of the associative memory module 4-k. The bit field of the status word (as a key for associative seeking),and the bit fields of the operand and the transmission strobe are transmitted respectively to the inputs 372-1, 372-2 and 371-3 of the associative memorizing unit (AMU) 367. The bit field of the status word is also transmitted to the informational input of the buffering register 366. The control input of the buffering register 366 receives the transmission strobe from the second control input 49 of the associative memory module.

A sub-packet which does not have a pair "stays" in memory.

When the AMU contains the corresponding pair operand, the bit fields of the first and the second operands are formed at the outputs 368-1 and 368-2. The bit fields of the first and the

second operands, together with the bit field of the status word (at the output of register 366), are transmitted to the informational input of the associative memory module 4-k. The second informational output 92 of the associative memory module 4-k receives the transmission strobe, formed at the first control output 369 of the AMU 367.

Having been formed at the informational output 51 of the associative memory module k, the ensuing packet is transmitted to the input 36-k of the buffering block 5 and then to the corresponding input of the buffering unit 348-k. The input 37-k of the buffering unit 348-k receives the transmission strobe from the second control input 52 of the associative memory module 4-k through the corresponding input of the buffering block 5.

If the received packet is an operand packet, its functional fields bits are received by the register 358-2 of the buffer 350-2, and the corresponding receiving control signal is formed at the output 359-9 of the control unit 356-2.

From the output of the register 358-2 the bit fields of the packet are transmitted to the second informational input of the switch 353. The corresponding control input of the switch 353 receives the signal of switching control from the output of "AND" element 354-1. The signal of switching control is transmitted together with the bit fields of the packet to the first input of the switch 353, which plays the part of transmission strobe, which is completed at the output of the "OR" element 353-1.

If the corresponding input register 307-k is free in the switching unit 263-2 of the switch 3, then the input 27-2-k of the switch 3 receives a packet of operands from the first output of the switch 353 through the output 352-3 of the buffer 350-2, through the output 349-6 of the buffering unit 348-k and through the output 45-k of the block 5. Respectively, the transmission

strobe is transmitted to the input 26-k of the switch 3 from the output 44-k of the buffering block 5 and the ensuing processing cycle is run.

When the receiving to the switch 3 is closed, in the case when the register 307-k is busy, a signal blocking transmission is transmitted from the switching unit to the input 33-k of the buffering block 5. The signal blocking transmission is transmitted through the corresponding input of the unit 348-k to the input 351-1 of the buffer 350-2 and from the buffer to the input 362-1 of the control unit 356-2 and the "OR" element input 353-5. At the output of the "OR" element the control signal is formed. The control signal is transmitted to the fifth control input of the switch 353. Information from the switch 353 is transmitted to through its second output to an input of the RMU 355, accompanied by the loading signal from the output 359-11 of the control unit 356-2. Information loading to the RMU 355 will be carried out until the blocking signal is cleared on the input 33-k of the buffering block 5. When the signal is cleared and if there is no information at the registers 358-1 and 358-2 and at the fourth informational input of the switch 353, the bits of the packet are transmitted from the RMU 355 through the third informational input of the switch 353 to the output 352-3 of the buffer 350-2 and to the corresponding input 45-k of the buffering block 5, and through the corresponding inputs and outputs of the switch 3 - to the fourth informational input 16 of the k-th processor unit.

If the result, obtained in the executive device 66, does not require a search for the corresponding pair, which is determined by the single-inputness of the instruction, then the result of the processing and the corresponding strobe of transmission are formed on the outputs 21-4, 21-5 and 19-4 of the k-th processor unit respectively, to which they are transmitted from the corresponding outputs of the switch 61 and the control unit 63 (Fig. 2). The bit fields of the result and the corresponding control signals are formed similarly to the result of the double-input

instruction. The sub-packet bits and the strobe of transmission are transmitted to the inputs 34-k and 35-k of the buffering block 5.

If the transmitted sub-packet is an instruction word, it is received by the register 358-1 of the buffer 350-1. The corresponding control signal is formed at the output 369-8 of the control unit 356-1. The bits of the sub-packet are transmitted from the output of the register 358-1 to the informational input of the switch 357. From the first informational output of the switch 357 the bits of the sub-packet are transmitted to the first informational input of the switch 353. The corresponding signal of the switching control, received by its first control input, is formed at the output of the "AND" element 354-2, A control signal is transmitted from the output 359-4 of the control unit 356-1 to an input of the "AND" element 354-2(Fig. 26, 27).

The second informational output of the switch 357 is used for transmission of the computing result to the external controlling system. The corresponding control signal is formed at the first output of the decoder 365-1. The input of decoder 365-1 receives the bits of the code determining the type of the sub-packet. The information from the second informational output of the switch 357 together with the strobe of transmission from the output 359-7 of the control unit 356-1 is transmitted to the output 352-4 of the buffer 350-1 and through the output 349-7 of the unit 348-k and the output 43-k of the block 5 is transmitted to the second informational output 11 of the system.

The bit fields processing in the executive device 65, including the determination by the instruction system operations of the functional fields of the status word, are realized in the switching block 103 (Fig. 5,7). The corresponding control signals, which are formed at an output of decoder 137 are transmitted through the output 111-3 of the control block 101 to the inputs 113-1...113-12 of the switching block 103. In the block 103, the signals of the switching group

173...178 control are formed at the outputs 203...222 of the control unit 122 (Fig. 7). The informational inputs of control unit 122 receive the bits of the functional fields of the status word, transmitted from the outputs 122-2...122-11 of the input register unit 108. The modified fields of the status and data words, formed this way, on the registers 161...171 are transmitted through the informational outputs of the unit 103 to the inputs 112-3 and 112-4 of the output switch 102, and from its output - to the address and the second informational outputs 86 and 88 of the executive device 65.

In addition to the operations of modification of functional fields, the executive device 65 also carries out the operations of relations determination (e.g., between the data values of two inputs of an instruction or between the values of separate functional bit groups). Such operations are run in ALU 106.

As for the rest, the working of the functional units of the executive device 65 is similar to the working of the corresponding units of the executive device 66. The corresponding control and informational outputs 19-4, 21-4 and 21-5, 19-1, 21-1 and 21-2 of the k-th processor unit are the place for forming the transmission strobes and the bits of the result packet functional fields, which realize the beginning of the ensuing computing cycle. Each processor unit processes the instructions without mutual synchronization with any of the other (N-1) processor units.

Thus, the described computer system provides a high performance by means of increasing the load of the processor units and obtaining in this way a decrease of the working programs running time. Then, a high parallelism of the processor units' working is obtained automatically and there is no need to distribute the group parallel processes between separate computational structures (executive devices) inside every running program, or between programs, which is usually carried

out by a person, who may become unable to cope with this problem when the number of parallel computing structures increases.

Industrial applications

The invention can be applied for both engineering and technical calculations in the space and aviation technologies, geodesy, hydrometeorology and other fields.



Formula of the invention

1. Computer system contains the switch (2) and N processor units (1-1...1-N) the second informational output (11) and the third informational input (8). The first control outputs (19-1) and address outputs (20) of the i-th processor unit (1-i) (i=1...N) are connected correspondingly with the i-th input (54-i) of the first group of control inputs and with the i-th input (55-i) of the group of the switch address inputs. The first (21-1) and the second (21-2) informational outputs of the i-th processor unit (1-i) are connected with the corresponding i-th input (57-i) of the group of the switch informational inputs. The first informational (13), address (17-1), control (18-1) and the second informational (14), address (17-2), control (18-2) inputs of the i-th processor unit (1-i) are connected with the first (6) and second (7) informational inputs of the system. The first control input (9) of the system is connected with the control input (53) of the switch (2) and with the third control input (18-3) of the i-th processor unit (1-i). The control output (58) of the switch (2) is connected with the fourth control input (18-4) of the i-th processor unit (1-i). The third informational output (21-3) of the i-th processor unit (1-i) is connected with the first informational output (10) of the system. The computer system is characterized by the fact that there are introduced the auxiliary switch (3), N modules (4-1...4-N) of associative memory and the buffering block (5). The first control (30-1-i), first informational (30-2-i), second control (30-3-i) and second informational (30-4-i) outputs of the i-th group of exchange outputs of the auxiliary switch (3) are connected correspondingly with the fifth control (18-5), third informational (15), sixth control (18-6) and fourth informational (16) inputs of the i-th processor unit(1-i). The first group of control outputs (28-1...28-N) of the auxiliary switch (3) is connected with the first group of control inputs (32-1...32-N) of the buffering block (5). The second group

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of control outputs (29-1...29-N) of the auxiliary switch (3) is connected with the second group of control inputs (33-1...33-N) of the buffering block (5).

The control input (22) of the auxiliary switch (3) and the control input (31) of the buffering block (5) and the first control input 46 of each module (4-1...4-N) of associative memory are connected with the control input (9) of the system. The i-th inputs of the first (23-1...23-N) and second (24-1...24-N) groups of control inputs of the auxiliary switch (3) are connected correspondingly with the second (19-2) and third (19-3) control outputs of the i-th processor unit (1-i). The seventh (18-7) and eighth (18-8) control inputs of the i-th processor unit are connected correspondingly with the i-th outputs of the first (39-1...39-N) and second (40-1...40-N) groups control outputs of the buffering block (5). The third group of control outputs (41-1...41-N) and the first group of the informational outputs (42-1...42-N) of the buffering block are connected correspondingly with the third group of control inputs (25-1...25-N) and the first group of informational inputs (27-1-1...27-1-N) of the auxiliary switch (3). The second group of informational outputs (43-1...43-N) of the buffering block is connected with the second informational output (11) of the system. The fourth group of control inputs (26-1...26-N) of the auxiliary switch (3) is connected with the fourth group of control outputs (44-1...44-N) of the buffering block (5). The i-th input of the first group of the informational inputs (34-1...34-N) of the buffering block is connected with the fourth (21-4) and fifth (21-5) informational outputs of the i-th processor unit (1-i). The fourth control output (19-4) of i-th processor unit is connected with the i-th input of the third group of control inputs (35-1...35-N) of the buffering block (5). The third group of informational outputs (45-1...45-N) of the buffering block is connected with the second group of informational inputs (27-2-1...27-2-N) of the auxiliary switch(3). The first

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control output (50) of the i-th module (4-i) of associative memory is connected with the i-th input of the second group of control inputs (56-1...56-N) of the switch (2). The i-th output of the group of informational outputs (59-1...59-N) of the switch is connected with the informational input (48) of the i-th module (4-i) of the associative memory. The informational (51) and the second control (52) outputs of the i-th module of the associative memory are connected with the i-th inputs of the second group of informational inputs (36-1...36-N) and the fourth group of control inputs (37-1...37-N) of the buffering block (5). The third group of informational inputs (38-1...38-N) of the buffering block is connected with the third informational input (8) of the system. And, the i-th output of the group of control outputs (60-1...60-N) of the switch (2) is connected with the second control input (49) of the i-th module (4-i) of the associative memory.

2. The computer system, according to invention, is characterized by the fact that each processor unit (1-i) contains the first (61) and the second (62) switches, the first (63) and the second (64) units of control, the executive device for instruction processing (65) and the executive device for the operand processing (66). The first (67-1) and second (67-2) control inputs of the first switch (61) are connected with the first (75-1) and second (75-2) control outputs of the first unit of control (63). The third control output (76-1) of the first unit of control is connected with the first control input (81) of the executive device for instruction processing (65). The first (79-2) and the second (79-2) control outputs of the second unit of control (64) are connected with the first (70-1) and second (70-2) control inputs of the second switch (62). The first informational input (71-1) of the second switch is connected with the address output (86) of the executive device for the instruction processing (65), the first informational output (87) of the executive device for instruction processing is connected with the second informational input (71-

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2) of the second switch (62) and the first informational input (68-1) of the first switch (61). The second informational output (88) of the executive device for instruction processing is connected with the second informational input (68-2) of the first switch (61) and the third informational input (71-3) of the second switch (62). The first control output (83) of the executive device for instruction processing is connected with the first control input (73) of the first unit of control (63). The fourth control output (76-2) of the first unit of control (63) is connected with the first control input (89) of the executive device for operand processing (66). The first control output (91) of the executive device for operand processing (66) is connected with the second control input (74) of the first unit of control (63). The first control input (77) of the second unit of control (64) is connected with the second control output (92) of the executive device for the operand processing (66). The second control output (84) of the executive device for the instruction processing (65) is connected with the second control input (78) of the second unit of control (64). The second control input (82) of the executive device for the instruction processing (65) is connected with the third control output (80-1) of the second unit of control (64). The fourth control output (80-2) of the second unit of control is connected with the second control input (90) of the executive device for the operand processing (66). The fourth informational input (72-1) of the second switch (62) is connected with the address output (94) of the executive device for the operand processing (66), the first informational output (95) of the executive device for operand processing is connected with the fifth informational input (72-2) of the second switch and the third informational input (69-1) of the first switch. The second informational output (96) of the executive device for operand processing is connected with the fourth informational input (69-2) of the first switch and with the sixth informational input (72-3) of the second switch. The

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first, second and third informational outputs of the second switch are the address output (20), the first informational output (21-1) and second informational output (21-2) of the processor unit respectively. The third informational outputs of the executive device for the instruction processing (65) and of the executive device for the operand processing (66) are connected with the third informational output (21-3) of the processor unit. The fourth (21-4) and fifth (21-5) informational outputs of the processor unit are respectively the first and second informational outputs of the first switch (61). The fifth control output of the second unit of control (64) is connected with the first control output (19-1) of the processor unit. The second (19-2) and third (19-3) control outputs of the processor unit are the third control outputs (85) and (93) of the executive device for the instruction processing and of the executive device for the operand processing respectively. The fourth control output (19-4) of the processor unit is connected with the fifth control output of the first unit of control (63). The first informational 13, address 17-1 and control 18-1 inputs of the processor unit are the first informational, address and the third control inputs of the executive device for the instruction processing (65) respectively. The second informational (14), address (17-2) and control (18-2) inputs of the processor unit are connected correspondingly with the first informational, address and the third control inputs of the executive device for the operand processing (66). The fourth control input of the executive device for the operand processing and the fourth control input of the executive device for the instruction processing are connected with the third control input 18-3 of the processor unit. The fourth control input (18-4) of the processor unit is connected with the third control input of the second unit of control (64). The third informational input (15) of the processor unit is the second informational input of the executive device for the instruction processing (65). The fifth control

input of the executive device for the instruction processing is the fifth control input (18-5) of the processor unit. The fourth informational (16) and the sixth control (18-6) inputs of the processor unit are connected with the second informational and the fifth control inputs of the executive device for the operand processing (66) respectively. And, the seventh (18-7) and eighth (18-8) control inputs of the processor unit are connected with the third and fourth control inputs of the first unit of control (63) respectively.

3. The computer system, according to invention, is characterized by the fact that the auxiliary switch (3), according to the invention, contains the first (262-1) and the second (262-2) units of control and the first (263-1) and the second (263-2) units of switching. The first groups (268-1...268-N) of the control outputs of the first (262-1) and second (262-2) units of control are connected with the first (28-1...28-N) and second (29-1...29-N) groups of the control outputs of the auxiliary switch (3) respectively. The first (30-1-i) and second (30-3-i) control outputs of the i-th group of exchange outputs of the auxiliary switch are connected with the i-th outputs 269-i of the second group of the control outputs (269-1...269-N) of the first (262-1) and second (262-2) units of control respectively. The control inputs (264) of the first and second units of control are connected with the control input (22) of the auxiliary switch (3). The first (27-1-1...27-1-N) and second (27-2-1...27-2-N) groups of the informational inputs of the auxiliary switch are connected with the groups of the informational inputs (274-1...274-N) of the first (263-1) and second (263-2) units of switching respectively. The i-th outputs of the group of the informational outputs (275-1...275-N) of the first and second units of switching are connected correspondingly with the first (30-2-i) and second (30-4-i) informational outputs of the i-th group of the exchange outputs of the auxiliary switch (3). The first (23-1...23-N) and second (24-1...24-N) groups of the control

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inputs of the auxiliary switch are connected with the first groups of the control inputs (265-1...265-N) of the first (262-1) and second (262-2) units of control respectively. The groups of the control outputs (276-1...276-N) of the first (263-1) and second (263-2) units of switching are connected correspondingly with the second groups (266-1...266-N) of the control inputs of the first (262-1) and the second (262-2) units of control. The third groups (267-1...267-N) of the control inputs of the first and the second units of control are connected correspondingly with the third (25-1...25-N) and fourth (26-1...26-N) groups of the control inputs of the auxiliary switch (3). And, the third groups of the control outputs (270-1-1...270-N-N) of the first (262-1) and second (262-2) units of control are connected with the first groups 272-i-j of the control inputs (272-1-1...272-N-N) of the first (263-1) and second (263-2) units of switching respectively. The second group of the control inputs (273-1...273-N) of each of these units is connected correspondingly with the fourth group of the control outputs (271-1...271-N) of the first (262-1) and second (262-2) units of control.

4. The device according to invention, is characterized by the fact that the buffering block (5), contains the group of the buffering units (348-1...348-N). The first (349-1), second (349-2) and third (349-3) control outputs of the i-th buffering unit (348-i) are connected with the i-th outputs of the first (39-1...39-N), second (40-1...40-N) and third (41-1...41-N) groups of the control outputs of the buffering block (5) respectively. The i-th inputs of the first (32-1...32-N) and second (33-1...33-N)groups of the control inputs of the buffering block are connected with the first and second control inputs of the i-th (348-i) buffering unit respectively. The fourth control output (349-4) of the buffering unit is connected with the i-th output (44-i) of the fourth group of the control outputs (44-1...44-N) of the buffering block. The control input (31) of the buffering

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block is connected with the third control input of each of the buffering units (348-1...348-N). The i-th inputs of the third (35-1...35-N) and fourth (37-1...37-N) groups of the control inputs of the buffering block (5) are connected with the fourth and fifth control inputs of the i-th buffering unit (348-i) respectively. The first (349-5), second (349-6) and third (349-7) informational outputs of the buffering units are connected correspondingly with the i-th outputs of the first (42-1...42-N), second (43-1...43-N), and third (45-1...45-N) groups of the informational outputs of the buffering block (5). The i-th inputs of the first (34-1...34-N), second (36-1...36-N) and third (38-1...38-N) groups of the informational inputs of the buffering block are connected with the first, second and third informational inputs of the i-th buffering unit (348-i) respectively.

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