

ABSTRACT

A semiconductor memory device a memory cell array and a repair control circuit. The memory cell array including a normal cell region and a redundancy cell region, the normal cell region including a plurality of normal region groups, and redundancy cell region configured to replace failed memory cells of the normal cell region. The repair control circuit configured to, determine a target normal region group from among the plurality of normal region groups based on an input address, extract target fail addresses from among a plurality of fail addresses based on the target normal region group, and control a repair operation based on the target fail addresses and the input address.

FIG. 1