# Claims

1. A method for producing a semiconductor integrated circuit device comprising a memory circuit region and a peripheral circuit region, the memory circuit region including a memory cell in which a memory gate structure is disposed between a first select gate structure and a second select gate structure through a sidewall spacer, the first select gate structure including a first select gate electrode, the second select gate structure including a second select gate electrode, the peripheral circuit region including a logic gate structure of a peripheral circuit, the method comprising:

a sidewall spacer formation step of forming the memory gate structure in the memory circuit region and then forming the sidewall spacer covering the memory gate structure, the memory gate structure including a lower gate insulating film, a charge storage layer, an upper gate insulating film, and a memory gate electrode stacked in this order;

a conductive layer formation step of stacking a gate insulating film and a conductive layer in this order in the memory circuit region formed with the memory gate structure and in the peripheral circuit region;

a conductive layer patterning step of etching back the conductive layer in the memory circuit region while leaving intact the conductive layer in the peripheral

circuit region, so as to form a sidewall-shaped surrounding conductive layer around the memory gate electrode and along the sidewall spacer; and

a gate electrode formation step of patterning the conductive layer in the peripheral circuit region by using a resist patterned by using a photomask, so as to form a logic gate electrode of the logic gate structure on the gate insulating film, and removing at least a part of the surrounding conductive layer in the memory circuit region by using the resist, so as to divide the surrounding conductive layer into the first select gate electrode and the second select gate electrode, the second select gate electrode being electrically separated from the first select gate electrode.

2. The method for producing a semiconductor integrated circuit device according to claim 1, further comprising, before the sidewall spacer formation step, a first photomask processing step of implanting impurities by using a resist into a portion of the memory circuit region where the memory gate structure is to be formed, so as to form a channel formation layer, the resist being patterned by using a first photomask dedicated to fabrication of the memory circuit region,

wherein the sidewall spacer formation step includes a second photomask processing step of forming a memory gate electrode conductive layer on the upper gate

insulating film and then patterning the memory gate electrode conductive layer by using a resist, so as to form the memory gate electrode, the resist being patterned by using a second photomask dedicated to fabrication of the memory circuit region,

the conductive layer patterning step includes a contact formation photomask processing step of forming the surrounding conductive layer and a contact formation conductive layer in the memory circuit region by using a resist patterned by using another photomask dedicated to fabrication of the memory circuit region, and

a dedicated photomask process using at least one photomask dedicated to formation of the memory cell in the memory circuit region includes a total of three steps, the three steps being the first photomask processing step, the second photomask processing step, and the contact formation photomask processing step.

3. The method for producing a semiconductor integrated circuit device according to claim 2, wherein

the conductive layer patterning step includes, before the contact formation photomask processing step, a third photomask processing step of implanting impurities by using a resist into portions of the memory circuit region where the first select gate electrode and the second select gate electrode are to be formed, so as to form a channel formation layer on a substrate surface

that is to be facing the first select gate electrode and the second select gate electrode, the resist being patterned by using a third photomask dedicated to fabrication of the memory circuit region, and

the dedicated photomask process includes a total of four steps, the four steps being the first photomask processing step, the second photomask processing step, the third photomask processing step, and the contact formation photomask processing step.

4. The method for producing a semiconductor integrated circuit device according to any one of claims 1 to 3, wherein

the first select gate electrode formed in the gate electrode formation step is connected to a first select gate line,

the second select gate electrode formed in the gate electrode formation step is connected to a second select gate line different from the first select gate line, and

the memory gate electrode is connected to a memory gate line.

5. A semiconductor integrated circuit device comprising:

a memory circuit region including a memory cell in which a memory gate structure is disposed between a first select gate structure and a second select gate structure

through a sidewall spacer, the first select gate structure including a first select gate electrode, the second select gate structure including a second select gate electrode; and

a peripheral circuit region including a logic gate structure of a peripheral circuit,

wherein the logic gate structure has a configuration in which a logic gate electrode made of a conductive layer same as a conductive layer of the first select gate electrode and the second select gate electrode is disposed on a gate insulating film,

the memory gate structure has a configuration in which a lower gate insulating film, a charge storage layer, an upper gate insulating film, and a memory gate electrode are stacked in this order, and

the first select gate electrode and the second select gate electrode are sidewall-shaped along the sidewall spacer on a sidewall of the memory gate electrode, and disposed along one line surrounding the memory gate electrode, and electrically separated from each other by a plurality of select gate electrode cutout portions at which the first select gate electrode and the second select gate electrode are absent.