Description

BACKGROUND OF THE INVENTION

Field of the Inveniton

The present invention relates to a photoelectric conversion device.

Related Background Art

It is well known that photo-sensors are used as photoelectric conversion devices in various picture information handling apparatus such as facsimiles, digital copiers and character readers. In modern apparatus, photo-sensors are arranged linearly to form Zong sensor. The sensor is capable of reading picture image with a high level of accuracy. Recently, as a photosensor which provides an inexpensive high-speed picture reading apparatus, a sensor has been proposed in which a thin film transistor (referred to as TFT hereinafter) of amorphous silicon is connected to a photoelectric converting section which is constituted by an array of photo-sensor elements which also are made of amorphous silicon. The photo-sensor of this type is inexpensive and is capable of reading picture information at a high speed. In this sensor, parallel signal output from the array of photo-sensor elements are changed into a serial signal by means of the switching TFT. This arrangement enables the number of the driving ICs to be decreased, thereby to reduce the cost of the driving circuit.

In the photosensor employing a TFT, however, there is the disadvantage that the number of manufacturing steps is increased because the photoelectric conversion section and the TFT have to be produced independently, with the result that the production cost is increased and the yield is lowered.

Japanese Journal of Applied Physics, Volume 20, Supplement 20/1, 1981 at pages 311 to 314 discloses an amorphous-silicon sensor which consists of an amorphous-silicon field-effect-transistor, an armorphous-silicon photo-conductor and an MOS capacitor. US Patent 4461956 discloses a solid state photoelectric converter comprising an array of photoelectric converting elements and a signal processing circuit for the accumulation of signals produced as outputs from the photoelectric converting elements and an arrangement for transferring the accumulated signals, the transfer arrangement being driven by an array of transistors wired in a two-dimensional matrix, the converting elements, the transfer arrangement and the transistors constituting the signal processing circuit being in the form of thin semi-conductor films.

SUMMARY OF THE INVENTION

The objects of the present invention are achieved by a device as claimed in claim 1 and a process as claimed in claim 8.

According to the present invention a photoelectric conversion device having, on a substrate a photoelectric conversion section comprising a thin film semiconductor layer for photoelectrically converting an image information, a charge accumulation section for accumulating an electric signal photoelectrically produced by said photoelectric conversion section, a switch section comprising a thin film semiconductor layer for outputting the charge accumulated in said charge accumulation section, is characterised in that the photoelectric conversion section comprises at least a pair of electrodes spaced from each other and formed on the thin film semiconductor layer, said charge accumulation section comprises a thin film semiconductor layer and an insulating layer both of which are sandwiched between at least a pair of electrodes, said switching section comprises a gate electrode, source and drain electrodes spaced from each other and an insulating layer sandwiched between the gate electrode and the thin film semiconductor layer, and said thin film semiconductor layers are made of the same semiconductor material.

According to the present invention a method, for producing a photoelectric conversion device, which includes forming a photoelectric conversion section, a charge accumulating section for accumulating an output of said photoelectric conversion section, and a switch section each section being provided with an insulating layer and a semiconductor layer is characterised in that the semiconductor layer of the three said sections is formed from the same material during a single manufacturing step.

How the invention may be carried out will now be described by way of example only and with reference to the accompanying drawings in which:

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a plan view of a photoelectric conversion device of the type to which the present invention can be applied;

Fig. 1B is a sectional view taken along the line X-Y of Fig. 1A;

Figs. 2A to 2D are sectional views illustrating different steps of a process for producing the device shown in Figs. 1A and 1B;

Fig. 3 is a plan view of a portion of another photoelectric conversion device of the kind to which the present invention can be applied;

Fig. 4 is is a sectional view taken along the line A-B of Fig. 3;

Figs. 5A to 5F are sectional views of different steps of a process for producing a photoelectric conversion device of the kind to which the present invention can be applied;

Fig. 6A is a plan view of still another photoelectric

conversion device of the kind to which the present invention can be applied;
Fig. 6B is a vertical sectional view taken along the line A-A' of Fig. 6A;
Fig. 7 is a diagram of an equivalent circuit of the photoelectric conversion device shown in Figs. 6A and 6B;
Fig. 8 is an illustration of a line sensor incorporating the arrangement shown in Figs. 6A and 6B;
Fig. 9A is a plan view of a further photoelectric conversion device of the kind to which the present invention can be applied;
Fig. 9B is a sectional view taken along the line A-A' of Fig. 9A;
Fig. 10 is a diagram of an equivalent circuit of the photoelectric conversion device;
Fig. 11 is an illustration of a first embodiment of the photoelectric conversion device in accordance with the present invention;
Fig. 12 is a sectional view taken along the line A-A' of Fig. 11;
Fig. 13 is a sectional view taken along the line B-B' of Fig. 11;
Fig. 14 is a schematic illustration of a second embodiment of the photoelectric conversion device in accordance with the present invention;
Fig. 15 is a sectional view taken along the line A-A' of Fig. 14;
Fig. 16 is a sectional view taken along the line B-B' of Fig. 14;
Fig. 17 is an illustra on of the charge accumulating section 20;
Fig. 18 is a chart showing charge accumulating capacity characteristic of the charge accumulating section 20;
Fig. 19 is a sectional view of a line sensor of a third embodiment of the photoelectric conversion device in accordance with the present invention;
Fig. 20 is a diagram showing an equivalent circuit of a line Sensor having a matrix array;
Fig. 21 is a timing chart illustrating the operation of the line sensor;
Fig. 22 is a perspective view of the line sensor;
Fig. 23 is a fragmentary sectional view of the line sensor shown in Fig. 22;
Fig. 24A to 24C are fragmentary sectional views of the line sensor shown in Fig. 23;
Fig. 25 is a plan view of a portion of a line sensor of a fourth embodiment of the present invention;
Figs. 26A and 26B are fragmentary sectional views of the line sensor shown in Fig. 2;
Fig. 27 is a plan view of a portion of the line sensor shown in Fig. 22, showing particularly lead lines 218;
Figs. 28A to 28E are fragmentary sectional views of the line sensor in different steps of the production process;
Fig. 29 is a fragmentary sectional view of the line sensor shown in Fig. 25;
Figs 30A to 30E are fragmentary sectional views of the line sensor in different steps of the production process;
Fig. 31 is a fragmentary sectional view of another line sensor;
Figs. 32A to 32E are fragmentary sectional views of the line sensor in different steps of the production process; and
Fig. 33 is a fragmentary sectional view of still another line sensor.

DESCRIPTION OF THE PRFFERRED EMBODIMENT

Figs. 1A and 1D show a photoelectric conversion device of the kind to which the present invention can be applied.

More particularly, Fig. 1A is a fragmentary sectional view showing a photo-sensor array incorporated in the device, while Fig. 1B is a sectional view taken along the line X-Y of Fig. 1A.

Referring to these Figures, the photo-sensor arrays have a glass substrate 1, an underlying electrode 2 of a capacitor, a gate electrode 3, an insulating layer 4, an ohmic contact layer 6 consisting of an n^+ layer, a photoconductive layer 7 of a photoelectric conversion section, and a semiconductor layer 8 of a TFT. The photoconductive layer 7 and the semiconductor layer 8 are made of the same amorphous silicon layer. The photo-sensor array further has a common electrode 10 and signal deriving line 11. An incident light impinges upon the photoconductive layer 7 so as to be converted by the latter into parallel electric signals which in turn are further converted into serial electric signals.

An example of the process for producing the photo-sensor array shown in Figs. 1A and 1B will be explained hereinunder with reference to Figs. 2A to 2D.

A glass substrate 1 (Corning No. 7059) polished at both surfaces is cleaned with an ordinary neutral detergent or an organic alkali detergent. Then, Cr is deposited to a thickness of 0.15 μ by electron beam evaporation deposition method. Then, a photo-resist pattern of a desired shape is formed by using a positype photo-resist (AZ-1370 made by Sibure). Subsequently, the unnecessary Cr is removed by an aqueous solution of a mixture of ammonium secondary cerium nitrate and perchloric acid, so as to form the underlying electrode 2 of capacitor and the gate electrode 3, as shown in Fig. 2A.

Subsequently, the glass substrate 1 is placed in a glow discharge decomposition apparatus of capacitance coupling type so as to be held in a vacuum atmosphere of a pressure of 1×10^{-6} Torr at 230 °C. Subsequently, SiH_4 diluted to 10 % by H_2 and NH_3 are simultaneously supplied into the apparatus at flow rates of 5 SCCM and 20 SCCM, respectively. Then,

a glow discharge is effected for 2 hours at RF discharge power of 15 W, using a high-frequency power supply of 13.56 MHz, so as to form an insulating layer 4 of silicon nitride to a thickness of 0.3 μ (μ ≡ μm). Then, SiH_4 gas is supplied at a flow rate of 10 SCCM, and glow discharge is effected for 2.5 hours with discharge power of 8 W and gas pressure of 0.07 Torr (1 Torr = 133.3 Pa) so as to form an amorphous silicon intrinsic layer to a thickness of 0.50 μ. Then, an n^+ layer 6 constituting an ohmic contact layer is deposited to a thickness of 0.12 μ as shown in Fig. 2B, using as the material a gas composed of SiH_4 diluted by H_2 to 10 % and PH_3 diluted by H_2 to 100 ppm mixed at a ratio of SiH_4 : PH_3 = 1 : 10, with a discharge power of 30 W.

Subsequently, a desired pattern is formed by using a posi-type photo-resist (OFPR-1300 made by Tokyo Ouka Kogyo), and a dry etching by plasma etching method is conducted with CF_4 gas of a pressure of 0.30 Torr and an RF discharging power of 100 W, so as to remove the unnecessary portions of the n^+ layer and the intrinsic layer of amorphous silicon, thereby forming amorphous silicon photoconductive layer 7 and a semiconductor layer 8, as shown in Fig. 2C.

Then, Aℓ is deposited by electron beam deposition method to a thickness of 0.5 μ so as to form a conductive layer, as shown in Fig. 2D.

Then, after forming a photo-resist pattern into a desired form, exposed portions of the conductive layer 9 are removed by a mixture constituted by phosphoric acid (85 vol% aqueous solution), nitric acid (60 vol% aqueous solution), glacial acetic acid and water which are mixed at a volumetric ratio of 16 : 1 : 2 : 1, thereby forming a common electrode 10 and a signal deriving line 11. Subsequently, dry etching is conducted by plasma etching method using a CF_4 gas, so as to remove unnecessary portion of the n^+ layer, thereby forming an n^+ layer of the desired pattern. Subsequently, the photo-resist is separated so that the photo-sensor array shown in Fig. 1B is formed.

The photo-sensor of this arrangement remarkably reduces the number of steps of the production process as compared with a photo-sensor array which is produced by a process in which the photoconductive layer and the semiconductor layer are formed independently. It is to be noted that the described embodiment eliminates the necessity for the masking which is indispensable in the conventional process for the purpose of preventing each amorphous silicon layer from being formed in the areas where the layer should not be formed. Furthermore, the degree of integration of the photo-sensor elements in the array can be increased so as to reduce the area of the substrate, because the photoelectric conversion section and the TFT section are farmed in close proximity to each other.

Fig. 3 is a plan view of a portion of the photo-sensor array in another arrangement of the kind to which the present invention can be applied, while Fig. 4 is a sectional view taken along the line A-B of Fig. 3. This arrangement has a light shielding film 12 and a light incident film 13. Other portions are materially the same as those in the first arrangement and are denoted by the same reference numerals as those used in Figs. 1A and 1B.

Layers of Aℓ and Cr are formed on the glass substrate 1 in the same way as that in the first arrangement. Then, the underlying layer 2 of capacitor, gate electrode 3 and the light shielding film 12 are formed by photo-lithographic method. Then, the same steps as the first arrangement are followed so that the photo-sensor array shown in Figs. 3 and 4 are formed.

The photo-sensor array of this embodiment is an original-contact type sensor which does not make use of any refraction distribution type rod lens array. As shown in Fig. 4, the incident light comes from the underside of the glass substrate and impinges upon the photoconductive layer 7 after being reflected from the surface of an original (not shown) placed on the photo-sensor. The light shielding film 12 is intended for preventing incident light from coming into the photoconductive layer from the underside thereof. This arrangement offers, besides the advantages derived from the first arrangement an advantage in that the sensitivity of the photo-sensor is increased by virtue of the fact that the light which has impinged upon and passed through the photoconductive layer is reflected by the Aℓ layer.

With the arrangements described so far there is a decrease in the number of production steps by virtue of the fact that the photoconductive layer of the photoelectric conversion layer and the semiconductor layer of the TFT are formed by the same amorphous silicon layer. In addition, since the photoelectric conversion section and TFT portion are formed in the close proximity of each other, the degree of integration of sensor elements is increased so as to realize a reduction in the size of the sensor array and a remarkably decrease in the substrate area.

Figs. 5A to 5F are sectional views illustrating steps of a process for producing a photo-sensor array shown in Fig. 2 as still another arrangement to which the present invention can be applied. Figs. 5A to 5F are sectional views taken along the line X-Y of Fig. 2.

In this process, glass substrate 1 (Corning No. 7059) polished at both surfaces is cleaned with an ordinary neutral detergent or an organic alkali detergent. Then, Cr is deposited to a thickness of 0.15 μ by electron beam evaporation deposition method. Then, a photo-resist pattern of a desired shape is formed by using a posi-type photo-resist (AZ-1370 made by Sibure). Subsequently, the unnecessary Cr is removed by an aqueous solution of a mixture of ammonium secondary cerium nitrate and perchloric acid, so as to form the underlying electrode 2 of capacitor and the

gate electrode 3, as shown in Fig. 5A.

Subsequently, the glass substrate 1 is placed in a glow discharge decomposition apparatus of capacitance coupling type so as to be held in a vacuum atmosphere of a pressure of 1 x 10^{-6} Torr at 230 °C. Subsequently, SiH_4 diluted to 10 % by H_2 and NH_3 are simultaneously supplied into the apparatus at flow rates of 5 SCCM and 20 SCCM, respectively. Then, a glow discharge is effected for 2 hours at RF (radio frequency) discharge power of 15 W, using a high-frequency power supply of 13.56 MHz, so as to form an insulating layer 4 of silicon nitride to a thickness of 0.3 μ. Then, SiH_4 gas is supplied at a flow rate of 10 SCCM, and glow discharge is effected for 2.5 hours with discharge power of 8 W and gas pressure of 0.07 Torr so as to form an amorphous silicon intrinsic layer to a thickness of 0.50 μ. Then, an n^+ layer 6 constituting an ohmic contact layer is deposited to a thickness of 0.12 μ as shown in Fig. 5B, using as the material a gas composed of SiH_4 diluted by H_2 to 10 % and PH_3 diluted by H_2 to 100 ppm mixed at a ratio of SiH_4: PH_3 = 1 : 10, with a discharge power of 30 W.

Subsequently, a desired pattern is formed by using a posi-type photo-resist (OFPR-1300 made by Tokyo Ouka Kogyo), and a dry etching by plasma etching method is conducted with CF_4 gas of a pressure of 0.30 Torr. and an RF discharging power of 100 W, so as to remove the unnecessary portions of the n^+ layer and the intrinsic layer of amorphous silicon, thereby forming amorphous silicon photoconductive layer 7 and a semiconductor layer 8, as shown in Fig. 5C.

Then, Aℓ is deposited by electron beam deposition method to a thickness of 0.5 μ so as to form a conductive layer, as shown in Fig. 5D.

Then, after forming a photo-resist pattern into a desired form, exposed portions of the conductive layer 9 are removed by a mixture constituted by phosphoric acid (85 vol% aqueous solution), nitric acid (60 vol% aqueous solution), glacial acetic acid and water which are mixed at a volumetric ratio of 16 : 1 : 2 : 1, thereby forming a common electrode 10 and signal deriving lines 11. Subsequently, dry etching is conducted by plasma etching method using a CF_4 gas, so as to remove unnecessary portion of the n^+ layer, thereby forming an n^+ layer of the desired pattern. Subsequently, the photo-resist is separated as shown in Fig. 5E. Finally, a photo-resist is formed in a desired pattern so as to form a photo-resist of a desired pattern, and the amorphous silicon semiconductor layer 8 of the TFT section is plasma-etched so that the semiconductor layer 8 has a reduced thickness of 0.2 μ, as shown in Fig. 5F.

Fig. 2, shows a portion of the photo-sensor array formed by the process explained above.

The photo-sensor of this arrangement remarkably reduces the number of steps of the production process as compared with conventional photo-sensor array because the photoconductive layer and the semiconductor layer of the TFT are formed of the same amorphous silicon layer. It is to be noted that the described arrangement ensures a high performance of the photosensor, through improvement in the sensitivity of the photoelectric conversion section and through increase in the OFF resistance of the TFT section, by virtue of the fact that the thicknesses of the amorphous silicon photoconductive layer 7 and the semiconductor layer 8 can be optimized. Furthermore, the degree of integration of the photo-sensor elements in the array can be increased so as to reduce the area of the substrate, because the photoelectric conversion section and the TFT section are formed in close proximity to each other.

Figs. 6A and 6B show still another photoelectric conversion device of the kind to which the present invention can be applied. More specifically, Fig. 6A is a plan view, while Fig. 6B is a sectional view taken along the line A-A' of Fig. 6A.

Referring to these Figures, a gate electrode 19, and an insulating film 11 of silicon nitride (SiNx:H) or silicon oxide (SiO_2) are formed on a glass substrate 10. In addition, a semiconductor layer 12 such as of amorphous silicon (a-Si) and an n^+ layer 13 constituting an ohmic contact layer are formed in sequence on the insulating layer 11. On the n^+ layer 13, further formed are electrodes 14, 15 of the photoelectric conversion section 20, source and drain electrodes 17, 18 of a TFT section 21, and a grounding electrode 16 of a series resistance section 22. The electrode 15 of the photoelectric conversion section 20 is connected to the gate electrode 19 of the TFT section 21, and the gate electrode 19 is connected to the series resistance section 22. In this embodiment, the insulating film 11 of the TFT section 21, semiconductor layer 12 and the n^+ layer 13 are formed simultaneously, so that the number of the steps in the production process can be reduced.

Fig. 7 is a diagram showing an equivalent circuit of the photoelectric conversion section. The photoelectric conversion device 28 is shown in the area surrounded by broken lines. The photoelectric conversion element 23 corresponds to the photoelectric conversion section 20, while the TFT 24 corresponds to the TFT section 21. Similarly, the serial resistance 25 corresponds to the serial resistance section 22. The photoelectric conversion element 23 is connected at its one end to the gate electrode of the TFT transistor 24 and also to one end of the series resistance 25. The series electrode 25 is grounded at its other end. Voltages V_G and V_D are applied to the other end of the photoelectric conversion element 23 and the source electrode of the TFT 24. A capacitor 26 for accumulating charges and an amplifier 27 are connected to the drain electrode of the TFT 24.

The operation of the photoelectric conversion device of this arrangement will be explained with refer-

ence to the equivalent circuit shown in Fig. 7.

Representing the conductances of the photoelectric conversion element 23 and the series resistor 25 by G_1 and G_2, respectively, the potential V_g of the gate electrode is expressed as follows.

$$V_g = \frac{G_1}{G_1 + G_2} V_G \ (V_G > 0)$$

When light impinges upon the photoelectric conversion element 23, the conductance G_1 is increased as compared with that before the light is received, so that the voltage Vg of the gate electrode of the TFT 24 also is increased. That is, the optical signal applied to the photoelectric conversion element 23 is converted into electric signals and is amplified by the TFT 24. The thus amplified electric signal is accumulated in the capacitor 26 and is further amplified by the amplifier 27.

Fig. 8 shows a line sensor as an application of the photoelectric conversion device described above. In this Figure, the same reference numerals are used to denote the same parts as those in the equivalent circuit shown in Fig. 7, and description of such parts is omitted for the purpose of simplification of explanation,

Referring to Fig. 8, a charge transfer section 31 is constituted by capacitors 26_1 to 26_n connected to the drain electrodes of TFTs 24_1 to 24_n of the photoelectric conversion devices 28_1 to 28_n, transistors 29_1 to 29_n for transferring the charges accumulated in the capacitors 26_1 to 26_n, shift registers 30_1 to 30_n for sequentially operating the transistors 20_1 to 29_n, and an amplifier 27. Usually, the charge transfer section 31 is constructed integrally as a driving IC.

A description will be made hereinafter as to an example of the method for producing the photoelectric conversion device of this arrangement.

A glass substrate 10 (Corning No. 7059) polished at both surfaces is subjected to ordinary washing by a neutral detergent. Then, Cr is deposited to a thickness of 0.05 μm by sputtering, and a photo-resist pattern of a desired form is formed by using a posi-type photo-resist (OFPR-800 produced by Tokyo Ouka Kogyo). Subsequently, the gate electrode 19 of the TFT is formed by using an aqueous solution of a mixture of ammonium secondary cerium nitrate and perchloric acid. After removal of the photo-resist, the glass substrate 10 is placed in a glow discharge decomposing apparatus of capacitance coupling type and is maintained at 200 °C under the vacuum of 1×10^{-6} Torr. Then, SiH_4 gas (furnished by Komatsu Denshi) diluted by hydrogen to 10 % and NH_3 gas of 99.999 % purity are introduced into the apparatus at rates of 100 SCCM and 50 SCCM, respectively, so as to set the gas pressure at 0.4 Torr. Then, after setting the gas pressure at 0.4 Torr, a glow discharge is conducted for 1 hour with an RF (radio frequency) discharge power of 50 W, using a high-frequency source of 13.56 MHz, thus forming an SiNx : H insulating layer 11 of 3000 Å (10Å = 1nm). Thereafter, a desired pattern is formed using a posi-type photo-resist and a dry etching is conducted using the photo-resist as the mask, by RIE (reactive ion etching) method under the conditions of CF_4 gas supply rate of 20 SCCM, gas pressure of 0.1 Torr and RF power of 100 W. Subsequently, after removal of the photo-resist, a glow discharge is conducted for 3 hours under the conditions of 10 % SiH_4 supply rate of 40 SCCM, gas pressure of 0.1 Torr and RF discharge power of 50 W, thus forming a semiconductor layer 12 of, for example, amorphous silicon (a-Si) having a thickness of 5000 Å. Subsequently, a glow discharge is carried out for 1 hour by introducing 10 % SiH_4 at a rate of 40 SCCM and PH_3 gas diluted to 100 ppm by hydrogen and under the conditions of a gas pressure of 0.2 Torr, and RF discharge power of 200 W, thus forming an ohmic contact n^+ layer 13 having a thickness of 1000 Å. Then, a desired form of photo-resist pattern is formed with a posi-type photo-resist and a dry etching is conducted using tne photo-resist as a mask by RIE (Reactive Ion Etching) method, under the conditions of CF_4 gas supply rate of 20 SCCM, gas pressure of 0.1 Torr, and RF discharge power of 100 W, thereby removing unnecessary portions of the n^+ layer, semiconductor layer and the insulating layer. Then, Aℓ is deposited by sputtering to a thickness of 0.5 μm and, after forming a desired form of photo-resist pattern with a posi-type photo-resist, and etching is effected with a mixture liquid constituted by phosphoric acid (85 vol% aqueous solution), nitric acid (60 vol% aqueous solution), glacial acetic acid and water which are mixed at a volumetric ratio of 16 : 1 : 2 : 1, thereby forming the desired pattern.

Subsequently, after removal of the photo-resist, the unnecessary portion of the n^+ film is removed by dry etching RIE method similar to mentioned before, so that the photoelectric conversion device shown in Fig. 6A was obtained.

Figs. 9A and 9B show the construction of a further photoelectric conversion device of the kind to which the present invention may be applied.

More specifically, Fig. 9A is a plan view, while Fig. 9B is a sectional view taken along the line A-A'. In these Figures, the same reference numerals are used to denote the same parts as those in the arrangement shown in Figs. 6A and 6B.

Referring to Figs. 9A and 9B, a transparent gate electrode such as of ITO or SnO_2 is formed on a glass substrate 10. An n^+ layer 13 and an insulating film 11 are formed on the gate electrode 19. Then, a semiconductor layer 12 and an n^+ layer 13 are formed in sequence on these layers. In this arrangement, one of the electrodes of the photoelectric conversion section 20 used also as a source electrode 18, so that the area occupied by the photoelectric conversion section can be reduced advantageously.

Fig. 10 shows an equivalent circuit of the photoelectric conversion device of this arrangement. In this Figure, the same reference numerals are used to denote the same parts as those used in the equivalent circuit diagram shown in Fig. 7, and detailed description of such parts is omitted.

As will be understood from Fig. 10, in this arrangement, a common voltage V_D is applied both to one of the electrodes of the photoelectric conversion element 23 of the photoelectric conversion device 32 and the source electrode of the TFT 24. The operation of this arrangement of the photoelectric conversion device is the same as that of the processing embodiment, and can be expressed by the following formula.

$$V_g = \frac{G_1}{G_1 + G_2} V_D \ (V_D > 0)$$

Detailed description of operation is omitted because it is substantially the same as that of the preceding arrangement.

A description will be made hereinunder as to an example of the process for producing the photoelectric conversion device of the kind to which the present invention may be applied.

A glass substrate 10 (Coning No. 7059) is subjected to an ordinary washing with a neutral detergent. Then, ITO is deposited to a thickness of 0.1 μm by sputtering. After forming a photo-resist pattern of a desired form with a posi-type photo-resist (made of Shibure), the gate electrode 19 of the TFT is formed with the use of an aqueous solution of a mixture of hydrochloric acid and ferric chloride. Then, the n^+ layer 13 constituting the ohmic contact layer is formed and a photo-resist pattern for the photoelectric conversion section is formed by using a posi-type photo-resist. Thereafter, the pattern is formed by dry etching. After removal of the photo-resist, then, the insulating film 11 of SiNx : H is formed and a pattern of this layer is formed in the same manner as that for the n^+ layer 13. Subsequently, the semiconductor layer 12 of amorphous silicon (a-Si) and the n^+ layer 13 are superposed in the same manner as that in the preceding embodiment. After forming a photo-resist pattern using a posi-type photo-resist (OFPR-800 produced by Tokyo Ouka Kogyo), dry etching is carried out by using this photo-resist pattern as a mask, so as to remove the unnecessary portions of the insulating film, semiconductor layer and the n^+ layer on the gate electrode 19. Subsequently, the photo-resist is removed and electron beam evaporation deposition is effected so as to deposit Aℓ to a thickness of 0.5 μm. Then, the desired electrode pattern is formed in the same manner as that in the preceding embodiment, and unnecessary portion of the n^+ layer is removed by dry etching, whereby the photoelectric conversion device as shown in Figs. 9A and 9B is obtained.

As will be understood from the foregoing description, both the arrangement explained in connection with Figs. 6A and 6B and the arrangement explained in connection with Figs. 9A and 9B can remarkably reduce the number of steps of the production process because of the fact that the photoelectric conversion section and the transistor section are produced by the same film-forming steps. In consequence, the yield is improved and the production cost is lowered advantageously.

A first embodiment of the invention will now be described with reference to Figs. 11, 12 and 13.

Fig. 11 is a schematic illustration of this embodiment of the photoelectric conversion device, while Fig. 11 is a sectional view taken along the line A-A' of Fig. 11. Fig. 13 is a sectional view taken along the line B-B' of Fig. 11.

This embodiment of the photoelectric conversion device in accordance with the present invention has a photoelectric conversion section 101, a charge accumulating section 102 corresponding to the photoelectric conversion section 101, a switch element section 103 having one end connected to the charge accumulating section 102, and a signal processing section circuit 103 connected to the other end of the switch element section 103. A reference numeral 106 is a power supply connected to the photoelectric conversion section 1. The photoelectric conversion section, the charge accumulating section 102 and the switch element section 103 are formed in accordance with the following procedure.

As shown in Figs. 12 and 13, a common electrode 4 and the gate electrode 111 of the switch element section 3 are formed on a glass substrate 116. An insulating layer 112 is formed on the gate electrode 111 on which are formed a semiconductor layer 113 made of a photoelectric conversion material and an ohmic contact layer 114. On the ohmic contact layer 114 are formed a common electrode 108 of the photoelectric conversion section 101, independent electrodes 105 of the charge accumulating section 102 and the drain and source electrodes 109 and 110 of the switch element section 103. The semiconductor layer 113 and the ohmic contact layer 114 between the independent electrodes 105 and the common electrode 104 serve as a dielectric material, so that it is not removed by etching but remains in the charge accumulating section 102 as shown in Fig. 12. These layers, however, are divided by etching during formation of the independent electrodes 105. Therefore, there is no risk for the insulating layer 112 between the independent electrode and the common electrode 104 to be degraded due to pin holes or deformation.

In this embodiment, there is no height difference between the common electrode 108 and the independent electrode 108 in the region near the window of the photoelectric conversion section, so that the occurrence of troubles such as cutting of lines is suppressed.

The operation of this photoelectric conversion

device is as follows.

Fig. 17 is an illustration of the operation of the charge accumulating section in this embodiment, while Fig. 18 shows charge accumulating characteristic of the same.

As the photoelectric conversion section 101 is irradiated with light, a voltage is applied to the common electrode 108, so that the conductivity is increased in the region of the window in the semiconductor layer 113, so that charges are accumulated in the independent electrodes 105 of the charge accumulating section 102. Then, the power supply 115 is connected between the independent electrode 105 and the common electrode 104 such that the potential of the common electrode 104 becomes higher, as shown in Fig. 17, and a voltage higher than a predetermined level is applied between these electrodes 104 and 105. As a result of the application of this voltage, the capacitance C is increased so that the charge accumulating amount can be increased. The accumulated charges are transferred to the signal processing circuit 107 when the field effect transistor of the switch element section 103 is ON, so as to be converted into serial signal by the signal processing circuit 107 and delivered from the latter as an output.

A second embodiment of the photoelectric conversion device of the invention will be explained with reference to Figs. 14, 15 and 16. More specifically, Fig. 14 is a schematic illustration of this embodiment, Fig. 15 is a sectional view taken along the line A-A′ of Fig. 14, and Fig. 16 is a sectional view taken along the line B-B′ of Fig. 14.

In this embodiment, the arrangement of the common electrode 104 and the independent electrodes 105 in the charge accumulating section 102 is reverse to that in the preceding embodiment shown in Figs. 11 to 14.

In this embodiment, independent electrodes 105 of the charge accumulating section 102 and the gate electrode 111 of the switch element section 3 are formed on a glass substrate 116. Then, the insulating layer 112, the semiconductor layer 113 and the ohmic contact layer 114 are formed on the common electrode layer 105. Subsequently, portions of the insulating layer 112, semiconductor layer 113 and the ohmic contact layer 114 are removed except the portion for forming the common electrode. Then, a process is carried out so as to form the common electrode 108 and the grounding electrode 117 of the photoelectric conversion section 101, common electrode 104 of the charge accumulating section 102, and the drain electrode 109 and the source electrode 110 of the switch element section 103. In this embodiment also, the insulating layer 112 between the independent electrodes 105 and the common electrode 104 are left without being etched, so that the same advantages as those in the preceding embodiment shown in Figs. 11 to 13 are derived also from this embodiment.

In these two embodiments, the semiconductor layer formed on the insulating layer is the same as the semiconductor layer of the amorphous silicon which constitutes the photoelectric conversion material of the photoelectric conversion section 101. This, however, is not exclusive. A photoelectric conversion device of the type to which the present invention can be applied comprises the semiconductor layer on the insulating layer 112 which may be provided separately from the semiconductor layer of the amorphous silicon. For instance, the semiconductor layer on the insulating layer 112 may be an amorphous silicon germanium semiconductor layer.

As will be seen from the foregoing description, in the embodiments shown in Figs. 11 to 13 and Figs. 14 to 16, the production process is simplified and degradation of the insulating layer during the production is avoided, by virtue of the provision of the semiconductor layer on the insulating layer on at least the charge accumulating section.In consequence, any tendency for the accumulating capacity and the photoelectric conversion characteristic to fluctuate is remarkably suppressed.

Fig. 19 is a third embodiment of the line sensor as a photoelectric conversion device in accordance with the present invention. Referring to this Figure, a substrate 201 has a lower electrode wiring 206 of a wiring section 202, a lower electrode wiring 207 of a charge accumulating section 204, and a lower electrode wiring 208 constituting the gate electrode of a switch element section 205. An insulating layer 209 is formed on these lower electrode wirings 206, 207 and 208 and the portions of the substrate 201 between these wirings 206, 207 and 208. A photoelectric semiconductor layer 210 is formed on the insulating layer 209. Portions of the insulating layer 209 and the photoconductive semiconductor layer 210 on the wiring section 202 are provided with apertures for the purpose of connection. Upper electrode wirings 212, 213 and 214 are formed on the photoconductive semiconductor layer 210. The opened area between the upper electrode wiring 212 and the upper electrode wiring 213 constitutes the photoelectric conversion region of the photoelectric conversion section 203. The upper electrode wiring 213, photoelectric semiconductor layer 210, insulating layer 209, and the lower electrode wiring 207 in combination constitute a charge accumulating capacitor, while the end of the upper electrode wiring 213 adjacent to the switch 205 constitutes a drain electrode. On the other hand, the end of the upper electrode wiring adjacent to the switch section 205 constitutes a source electrode. Although not shown, a doping layer is formed between the upper electrode wirings 212, 213, 214 and the photoconductive semiconductor layer 210, so that an ohmic contact is achieved therebetween. In the described embodiment of the invention, each of the wiring section 202, photoelectric conversion section 203,

charge accumulating section 204 and the switch section 205 is provided with the insulating layer 209 and the photoconductive semiconductor layer 210. These layers for the sections 202 to 205 are formed in the same steps of process.

In the wiring section 202, the photoconductive semiconductor layer 210 exists besides the insulating layer 209, between the lower electrode wiring 206 and the upper electrode wiring 212. The presence of the semiconductor layer 212, however, does not produce any unfavorable effect because it is necessary only that a sufficient insulation is provided between the lower electrode wiring 206 and the upper electrode wiring 212.

The photoelectric conversion section 203 employs the photoconductive semiconductor layer 210 formed on the substrate 1 through the intermediary of the insulating layer 209. The presence of the photoconductive semiconductor layer 210 appears as a change in the energy level of the interface between the photoconductive semiconductor 210 and the insulating layer 209. This, however, does not cause any change which would impair the basic performance of the photoconductive material. In this case, it is possible to provide an electrode between the substrate 201 of the photoelectric conversions section 203 and the insulating layer 209 so as to control and optimize the energy level at the inter-surface of the photoconductive semiconductor layer 210.

In the charge accumulating section 204, a photoconductive semiconductor layer 210 provided on the insulating layer 209 affects the charge accumulating capacity. This effect has a dependency on bias of the capacitance. Thus, the electrostatic capacitance is changed in accordance with the degree of band bending of the semiconductor layer at the interface of the insulating surface. In the charging and discharging operation in this embodiment, however, the bias-dependency can be reduced to a negligible level by applying a negative bias to the electrode adjacent to the insulating layer 209.

The thickness of the photoconductive semiconductor layer 210 is selected such as to provide superior photoelectric conversion characteristic of the photoelectric conversion section 203 and the switching characteristic of the switch section 205.

A description will be made hereinunder as to the case where the switch section of the line sensor is constituted by a matrix-switch array.

Fig. 20 shows an equivalent circuit of a line sensor having a matrix switch array. In this Figure, S1, S2, ..., Sn (represented by SY1, hereinafter) denote photo-sensors which correspond to the photoelectric conversion section 203, charge accumulating capacitors C1, C2,..., CN (represented by CY1, hereinafter) corresponding to the charge accumulating section 204 and adapted for accumulating photo-currents in the photo-sensors SY1. ST1, ST2, ..., STN (represented by STY1, hereinafter) represent transfer switches for transferring the charges from the accumulating capacitors CY1 to the load capacitors CX1. SR1, SR2, ..., SRN (represented by SR1, hereinafter) are discharge switches for resetting the charges of the accumulating capacitor CY1. In this example, the switch section 205 is composed of a transfer switches STY1 and the discharging switches SRY1.

The photosensors S1, accumulating capacitor CY1, transfer switches ST1 and the discharge switches SRY1 are arranged in respective arrays and sectioned into N x M blocks. The gate electrodes of the transfer switches ST1 and discharge switches SR1 arranged in arrays are connected to a matrix wiring section 215. The gate electrodes of the transfer switches ST1 of each block are connected commonly to the gate electrodes of the transfer switches of corresponding orders of other blocks. On the other hand, the gate electrodes of the discharge switches SR1 are connected to the gate electrodes of the transfer switches of next orders in each block.

The common lines (gate driving lines G1, G2, ..., GN) of the matrix wiring section 215 are driven by the gate driving section 216. On the other hand, the output signals are delivered to a signal processing section 217 through signal deriving lines 218 (signal output lines D1, D2, ..., DN).

Fig. 21 is a timing chart illustrating the operation of the line sensor described above.

Selection pulses (VG1, VG2, VG3, ..., VGN) are applied successively to the gate driving lines (G1, G2, ..., GN) from the gate driving section 216. As the gate driving line G1 is selected first, the transfer switch ST1 is turned on and then the charges accumulated in the accumulating capacitor C1 are transferred to the load capacitor CX1. Then, the gate driving line G2 is selected so that the transfer switch ST2 are turned on, so that the charges accumulated in the accumulating capacitor C2 are transferred to the load capacitor CX1. At the same time, the discharge switch SR1 operates to reset the charge of the accumulating capacitor C1. Then, the gate driving lines G3, G4, ..., GN are successively selected, thus performing reading of information. In Fig. 21, symbols VC1, VC2, ..., VCN represent changes in the potentials of the charge accumulating capacitors CY1. The above-described operation is conducted for each block, and the output signals VX1, VX2, ..., VXN from the respective blocks are sent to inputs D1, D2, ..., DM of the signal processing section 217 so as to be converted into serial signals. The serial signals thus formed are output from the signal processing section 217.

Fig. 22 is a perspective view of the line sensor explained hereinabove.

Referring to Fig, 22, a reference numeral 201 designates a substrate on which are formed the matrix wiring section 215, photoelectric conversion section 203, charge accumulating section 204 for accu-

mulating the charges output from the photoelectric conversion section 203, array of transfer switches 219 for transferring the charges from the charge accumulating section 204 to the signal processing IC 21, and array of discharge switches 220 for resetting the charge accumulating section 204. The transfer switches 219 and the discharge switches 220 are sectioned into N x M blocks. The drain electrodes of the transfer switches 219 are connected to corresponding charge accumulating sections, while the source electrodes in each block are connected to a common line which in turn is connected to the load capacitor (not shown) and the signal processing IC 221.

On the other hand, the gate electrodes in each block are connected to the matrix wiring section 215 such that the gate electrode lines of the same order in each block are connected commonly. The common electrode of the matrix wiring section 215 is connected to the gate drive IC 222. The signal processing IC 221 is disposed on the central portion of the substrate 201 so as to minimize the length of the deriving line 218. Shield patterns (not shown) having grounding potential are disposed in the areas between adjacent deriving lines 218.

Fig. 23 is a plan view of a portion of the line sensor described above. In this Figure, there are shown the matrix wiring section 215, the photoelectric conversion section 203, the charge accumulating section 204, the transfer switch 219, the discharge switch 220 for resetting the charge of the charge accumulating section 204, the deriving line 218 for connecting the signals from the transfer switch to the signal processing IC, and the load capacitor 223 for accumulating and reading the charges transferred by the transfer switches 219.

In this embodiment, amorphous silicon (a-Si:H) film is used as the photoconductive semiconductor layer of the photoelectric conversion section 203, transfer switch 219 and the discharge switch 220. On the other hand, the insulating layer is constituted by a silicon nitride film (SiNH) formed by a glow discharge.

Fig. 23 shows, for the purpose of simplification of the drawings, only the upper and lower electrode wirings are shown, while the photoconductive semiconductor layer and the insulating layer are omitted. The photoconductive semiconductor layer and the insulating layer are formed in each of the photoelectric conversion section 203, charge accumulating section 204, transfer switch 219 and the discharge switch 220, as well as between the upper electrode wiring and the substrate. Furthermore, an a-SiH layer doped into n^+ type is formed at the interface between the upper electrode wire and the photoconductive semiconductor layer, thus providing an ohmic contact.

In the wiring pattern of the line sensor of this embodiment, the signal lines output from all the photoelectric conversion sections are laid so as not to intersect with pone another, thereby preventing generation of cross-talk between the signal components and the generation of induction noises from the gate electrode wirings.

Figs. 24A-24C are fragmentary longitudinal sectional views of the photoelectric conversion section 203, taken along the lines A-A', B-B' and C-C' of Fig. 23, respectively. Referring to Fig. 24A which is a longitudinal section of the photoelectric conversion section 203, there are shown the lower electrode wiring 224 connected to the gate electrode of the transfer switch 219, the insulating layer 209, the photoconductive semiconductor layer 210, and the upper electrode wirings 212, 213. The light impinging upon the line sensor causes a change in the conductivity of the a-Si:H layer constituting the photoelectric semiconductor layer 210, thereby causing a change in the electric current which flows between the upper electrode wirings 212, 213 which oppose in a comb-teeth form.

Fig. 24B shows the longitudinal section of the charge accumulating section 204. As will be seen from this Figure, the charge accumulating section 204 has the lower electrode wiring 207, the dielectric structure constituted by the insulating layer 209 formed on the lower electrode wiring 207 and the photoconductive semiconductor layer 210, and the upper electrode wiring 213 formed on the photoconductive semiconductor layer 210. This charge accumulating section 4 has a structure which is the same as that of MIS (Metal-Insulator-Semiconductor) capacitor, and can be used both under positive and negative biases. It is to be noted, however, stable capacitance and stable frequency characteristic can be obtained by using the line sensor such that a negative bias is always applied to the lower electrode wiring 207.

Fig. 24C is a longitudinal sectional view of the transfer switch 219 and the discharge switch 220. As will be seen from this Figure, the transfer switch 219 is composed of the lower electrode wiring 224 constituting the gate electrode, the insulating layer 209 constituting the gate insulating layer, the photoconductive semiconductor layer 210, the upper electrode wiring 214 constituting the source electrode, and the upper electrode wiring 213 constituting the drain electrode. The gate electrode and the photoconductive semiconductor layer of the discharge switch 220 are the same layers as the insulating layer 209 and the photoconductive semiconductor layer 210 mentioned before. The source electrode, the gate electrode and the drain electrode are constituted, respectively, by the upper electrode wiring 213, lower electrode wiring 227 and the upper electrode wiring 226. The transfer switch 219 and the discharge switch 220 in combination constitute a TFT.

As explained before, n^+ layer of a-Si:H is formed between each of the upper electrode wirings 213, 214 and 226 and the photosensitive semiconductor layer

210, so as to realize an ohmic contact.

It is an ordinary measure to form a passivation film of SiNH, SiO_2 silicon or another organic resin is formed on an upper portion of the TFT. Such a passivation film, however, is omitted from Fig. 24C.

As will be understood from the foregoing description, the line sensor of this embodiment, it possible to simultaneously form by the same process the photoelectric conversion section, charge accumulating section, transfer switch, discharge switch and the matrix wiring sections, because these sections commonly have a laminated structure constituted by a photoconductive semiconductor layer and the insulating layer.

Fig. 25 is a plan view of a portion of a line sensor as still further embodiment of the present invention. This line sensor is used as a so-called lens-less type photoelectric conversion device in which light impinges from the substrate-side so that the light reflected by the original held in contact with the photoelectric conversion section 203 is directly read by the photoelectric conversion section 203.

The photoelectric conversion section 203 is provided with a light shielding layer 225 for shielding the illuminating light emitting from the substrate side, as well as a window 228 through which the original is illuminated.

Figs. 26A and 26B are sectional views of the line sensor shown in Fig. 25, taken along the lines D-D' and E-E' of Fig. 25.

As will be seen from this Figure, the illuminating window 228 is constituted by an opening formed in the upper electrode wiring 212. This window, however, may be formed by the lower electrode wiring.

As will be seen from Fig. 26B, the light shielding layer 225 is formed by the lower electrode wiring. Usually, a negative bias is applied to this light shielding layer 225 and the bias is controlled such as to sufficiently attenuate the dark current.

Fig. 27 is a plan view of a portion of the output line 218 shown in Fig. 22.

Referring to this Figure, a ground pattern 229 is disposed between output lines 218 of the adjacent blocks. The ground pattern 229 effectively prevents any cross-talk which may otherwise be caused by a capacitance coupling between the adjacent deriving lines. The line capacitance formed between the output line 218 and the ground pattern 229 serves as a part of the load capacitor. Any difference in the capacitance due to difference in the length of the output lines can be eliminated by adjusting the area of the load capacitor 223, thus obtaining a substantially equal effective capacitance of the load capacitors in all the blocks. A numeral 230 designates a output terminal which is connected to the deriving line 218.

In this embodiment, the matrix wiring is formed by the gate electrodes of the switch section, and the source electrodes of the transfer switches in each block are merged into a common line. This arrangement, however, is not exclusive and may be modified in various forms. For instance, the matrix wiring may be formed by the source electrodes.

As will be understood from the foregoing description, in this embodiment of the photoelectric conversion device, at least the photoelectric conversion section, accumulating section and the switch section are provided with an insulating layer and a photoconductive semiconductor layer formed on the insulating layer.

This arrangement enables these sections of the photoelectric conversion device to be formed simultaneously, so that the production process can be simplified in connection with the formation of the layers and elements. In addition, this embodiment is suitable for integration because the constituent parts have a substantially identical construction, thus making it possible to obtain a small-sized photoelectric conversion device. In addition, any tendency for the insulating layer to be deteriorated during the production is suppressed, thus remarkably eliminating the risks of troubles such as short-circuiting in the capacitor section, fluctuation in the capacitance, degradation in the insulation at the crossing sections of the electrode wiring.

In consequence, this embodiment enables the photoelectric conversion device to be produced at low costs, with a higher degree of freedom of design and superior reliability.

When it is necessary to employ a laminated structure for the wiring section in the photoelectric conversion device of this embodiment, the insulating layer and the photoconductive semiconductor layer in combination serve as an inter-layer insulator. It will be seen that this inter-layer insulator can be formed by the same step as the formation of the photoelectric conversion section and the switch section.

Figs. 28A to 28E are longitudinal sectional views of this embodiment in different steps of the production process.

As the first step, Aℓ/Cr is deposited to a thickness of 0.1 μm by vacuum deposition method, on the surface of a rinsed glass substrate having a high degree of smoothness and serving as the substrate 301, as shown in Fig. 28A. Then, a resist pattern was deformed by photolithographic method, thereby to form lower electrode wirings 306, 307 and 308 in the matrix wiring section 302, charge accumulating section 304 and the transfer switch section constituting the switch section 305.

Then, as shown in Fig. 28B, an insulating layer 309 consisting of silicon nitride is deposited to a thickness of 0.3 μm by an RF glow discharge in accordance with plasma CVD method, using SiH_4 gas and NH_3 or N_2 gas as the material. Subsequently, a photoconductive semiconductor layer 310 as an amorphous silicon intrinsic layer is formed to a thickness

of 0.1 to 1 μm, by the same method using SiH_4 as the material. Thereafter, an n^+ layer 315 constituting the ohmic contact layer is deposited to a thickness of 0.1 μm using SiH_4 and PH_3 gas as the material.

Then, as shown in Fig. 28C, a resist pattern is formed by photo-lithography and dry etching is effected with this resist pattern while using CF_4 gas, so as to partially remove the n^+ layer, photoconductive semiconductor layer and the insulating layer thereby forming a contact hole 316. In this case, it is not necessary to effect a selective etching of the n^+ layer, photoconductive semiconductor layer and the insulating layer.

Then, as shown in Fig. 28D, Aℓ/Cr is deposited to a thickness of 1.0 to 1.5 μm by vacuum deposition. Then, a resist pattern is formed by photolithographic method and a wet etching is effected so as to partially remove the Aℓ/Cr layer and the n^+ layer, thereby forming the upper electrode wirings 311, 312, 313, 314. The electrical connection to the lower electrode wiring 306 and the upper electrode wiring 312 of the wiring section 302 arranged in the form of a matrix is made through the contact holes 316. The gap of the photoelectric conversion section 303 and the channel of the transfer transistor serving as the switch section 30 are also formed in this step of the production process.

Then, a resist pattern is formed by a photolithographic method as shown in Fig. 28E, and dry etching was effected by using CF_4 gas, whereby the n^+ layer, photoconductive semiconductor layer and the insulating layer are partially removed. In consequence, the elements which have been connected through the photoconductive semiconductor layer are isolated, so that electrical connections are formed only in the portions which require such connection.

Then, the line sensor is completed by forming a passivation film (not shown) by silicon nitride or an organic resin.

The line sensor shown in Fig. 25 also can be formed by the process explained in connection with Figs. 28A to 28E. In this case, however, it is necessary to form the light shielding layer 317 shown in Fig. 29 in each of the sections. To this end, the shielding layer 317 is formed simultaneously with the formation of the lower electrodes 306, 307 and 308 shown in Fig. 28A.

A description will be made here with reference to Figs. 30A to 30E as to a still further embodiment in which the patterns of the upper electrode and the lower electrode shown in Fig. 19 are replaced by each other. Namely, while the transfer transistor in the embodiment shown in Figs. 28A to 28E are of so-called lower-gate staggered type TFT, the embodiment shown in Figs. 30A to 30E employs a transfer transistor of so-called upper-gate staggered type.

More specifically, Figs. 30A to 30E are sectional views of this embodiment in different steps of the production process.

Referring to Fig. 30E, on the substrate 301 are formed a lower electrode wiring 306 of the wiring section 302, lower electrode wiring 307 of the charge accumulating section 304, and a lower electrode wiring accumulating section 304, and a lower electrode wiring 308 of the switch section 305. An n^+ layer 315 constituting an ohmic contact layer is formed on the lower electrode wirings 306, 307 and 308. A photoconductive semiconductor layer 310 is formed on the n^+ layer 15 and in the area between the lower electrode wirings of the photoelectric conversion section 303 and the switch section 305. On the semiconductor layer 310 are formed an insulating layer 309 and upper electrode wiring sections 312, 313, 314. In the switch section 305, the upper electrode wiring 314 constitutes the gate electrode, while the lower electrode wiring 308 constitutes a source electrode. One end of the lower electrode wiring 307 constitutes a drain electrode.

When light impinges upon the photoelectric conversion section 303, electric current is generated by the photoelectric effect and this electric current is supplied to the charge accumulating section 304 from the photoelectric conversion section 303 through the lower electrode wiring 307. As in the case of the embodiment explained in connection with Figs. 28A to 28E, the charge accumulating section 304 is composed of the lower electrode wiring 307, n^+ layer 315, photoconductive semiconductor layer 310, insulating layer 309, and the upper electrode wiring 313. The charges thus accumulated are successively transferred for the reading purpose, through the photoconductive semiconductor layer 310 and the lower electrode wiring 308, in response to the turning on and off of the gate electrode constituted by the upper electrode wiring 314 of the transfer transistor section serving as the switch section 305, in accordance with the signal successively delivered through the matrix wiring section 302.

A description will be made hereinunder as to an example of the process for producing the line sensor described above.

As the first step, Aℓ /Cr is deposited to a thickness of 0.1 μm by vacuum deposition method, on the surface of a rinsed glass substrate having a high degree of smoothness and serving as the substrate 301, as shown in Fig. 30A. Then, the n^+ layer 315 as the ohmic contact layer is formed by an RF glow discharge in accordance with plasma CVD method, using SiH_4 gas and PH_3 gas as the material, to a thickness of 0.1μ m. Subsequently, a resist pattern is formed by photolithographic method, and wet etching is conducted by using this resist pattern, thereby forming the lower electrode wirings 306, 307 and 308 of the matrix wiring section 302, charge accumulating section 304 and the transfer switch section 305, as well as the n^+ layer 315.

Then, as shown in Fig. 30B, the photoconductive

semiconductor layer 310 as an amorphous silicon intrinsic layer is deposited to a thickness of 0.1 to 1 μm by an RF glow discharge in accordance with plasma CVD method, using SiH_4 gas as the material. Subsequently, the insulating layer 309 of silicon nitride is formed by deposition to a thickness of 0.3 μm by the same method, using SiH_4 gas and NH_3 or N_2 gas as the material.

Subsequently, as shown in Fig. 30C, a resist pattern is formed by a photolithographic method and the dry etching is effected with this resist pattern while using CF_4 gas, so as to partially remove the insulating layer, photoconductive semiconductor layer and the n^+ layer, thus forming the contact hole 316. In this case, it is not necessary to selectively etch the insulating layer, photoconductive semiconductor layer and the n^+ layer.

Then, as shown in Fig. 30D, Aℓ/Cr to a thickness of 1.0 to 2.0 μm, by vacuum deposition method. Thereafter, a resist pattern is formed by photolithography, and wet etching is conducted to partially remove the Aℓ/Cr so as to form the upper electrode wirings 312, 313, 314. In this case, the lower electrode wirings 306 and the upper electrode wirings 312 of the wiring section arranged in the form of a matrix are electrically operated through the contact holes 316. In the transfer transistor section serving as the switch section 305, the upper electrode wiring 314 constitutes the gate electrode.

Then, as shown in Fig. 30E, a resist pattern is formed by photolithography and dry etching is effected by using CF_4 gas, thereby partially remove the insulating layer, photoconductive semiconductor layer and the n layer, so as to isolate the elements which have been electrically connected. Thus, electric connection is made only in the portions where such a connection is necessary. The line sensor of this embodiment is thus completed.

From the view point of electrical driving of the device, it is preferred that the photoelectric conversion section, charge accumulating sections and the switch sections of the line sensor in the form of array have uniform distributions of the electric characteristics. The electric characteristic distribution in turn is largely affected by the thickness distribution of the insulating layer and the photoconductive semiconductor layers.

In this embodiment, the thicknesses of the insulating layer and the photoconductive semiconductor layer are determined when they are formed by deposition in the step shown in Fig. 30B, and no change in the thicknesses is caused in the subsequent steps shown in Figs. 30C to 30E. It is, therefore, possible to uniformalize the distribution of the electric characteristics and, hence, to obtain a line sensor having a degree of uniformity of the operation characteristics, provided that a good condition is given for the deposition such as to uniformalize the thickness distribution.

A description will be made as to a still further embodiment of the invention.

Fig. 31 is a fragmentary sectional view of the a line sensor as the still further embodiment.

In this embodiment, a light-shielding layer 312' is formed on the upper portion of the photoelectric conversion section 303 of the preceding embodiment. Thus, this line sensor is of so-called lens-less type in which the light impinges from the element side of the substrate and the light reflected by an original held in contact with the reverse side of the substrate is directly read by the photoelectric conversion section. The illuminating light illuminates the original from the element side of the substrate. The light-shielding layer 312' effectively prevents the illuminating light from coming into the photoconductive semiconductor section of the photoelectric conversion section 303, thereby diminishing generation of noise currents.

The line sensor of this embodiment can be produced substantially by the same method as that explained in connection with Figs. 30A to 30E. In this embodiment; however, it is necessary to form the light-shielding layer 312'. This light-shielding layer 312' can be formed simultaneously with the formation of the upper electrode wirings 312, 313, 314 from the same material as that of these wirings.

As will be understood from Fig. 31, the light-shielding layer 312' is provided on the upper portion of the photoelectric conversion section, and has a function to sufficiently attenuate any dark current when it is supplied with a bias voltage which is usually negative. The light-shielding layer 312', which is provided in the described embodiment on the upper layer of the photoelectric conversion section 302, may be provided on a unit housing to which the line sensor of this embodiment is secured, so as to prevent the illuminating light from impinging upon the photoelectric conversion section. In this case, however, it is necessary to attain a positional alignment between the light-shielding layer on the unit housing and the line sensor.

In general, the line sensor of the lens-less type requires the original to be placed in the vicinity of the photoelectric conversion section 330. In this embodiment, the original is positioned on the reverse side of the substrate 301. The substrate 301 is usually constituted by a glass plate. The glass substrate exhibits superior optical characteristics and wear resistance, and can serve also as a spacer for fixing the positional relationship between the photoelectric conversion section 302 and the original.

Thus, in this embodiment of the present invention, it is possible to produce a line sensor of lens-lens type without requiring any specific members, by suitably designing the factors such as the thickness of the substrate, incident angle of the light, and so forth. Furthermore, in this embodiment, the photoelectric

conversion section is provided on the substrate so that the light reflected by the original surface is transmitted only two smooth inter-surfaces, i.e., the inter-surface between the original surface and the substrate surface and the inter-surface between the substrate surface and the surface of the photoelectric conversion section. This remarkably facilitates the optical design of the device. In addition, the described embodiment makes it possible to protect the photoconductive semiconductor layer, which is very important from the view point of characteristics of the photoelectric conversion section and the switch section, from damaging and contamination which may occur during the production.

A still further embodiment of the photoelectric conversion device, as well as a production process thereof, will be described hereinunder. This embodiment employs, in place of the n^+ layer of the embodiment explained in connection with Figs. 28A to 28E, an insulating layer of silicon nitride, and this silicon nitride layer is perforated to form a contact hole, thus attaining the electrical connection between the photoconductive semiconductor layer and the upper electrode wiring.

Figs. 32A to 32E are fragmentary sectional views of the line sensor in different steps of the production process.

As the first step, Aℓ /Cr is deposited to a thickness of 0.1 μm by vacuum deposition method, on the surface of a rinsed glass substrate having a high degree of smoothness, as shown in Fig. 32A. Then, a resist pattern is formed by Photolithographic method, and wet etching is conducted with this resist pattern thereby to form lower electrode wirings 306, 307 and 308 in the matrix wiring section 302, charge accumulating section 304 and the transfer switch section constituting the switch section 305.

Then, as shown in Fig. 32B, an insulating layer 309a consisting of silicon nitride is deposited to a thickness of 0.3 μm by an RF glow discharge in accordance with plasma CVD method, using SiH_4 gas and NH_3 or N_2 gas as the material. Subsequently, a photoconductive semiconductor layer 310 as an amorphous silicon intrinsic layer is formed to a thickness of 0.1 to 1 μm, by the same method using SiH_4 as the material. Thereafter, an insulating layer 309b of silicon nitride is deposited to a thickness of 0.3 μm by using SiH_4 gas and NH_3 or N_2 gas as the material.

Then, as shown in Fig. 32C, a resist pattern is formed by photo-lithography and dry etching is effected with this resist pattern while using CF_4 gas, so as to form an opening in the insulating layer 309b. Subsequently, an n^+ layer 315 as the ohmic contact layer is deposited to a thickness of 0.1 μm by using SiH_4 gas and PH_3 gas as.the material. Then, as shown in Fig. 32D, a resist pattern is formed by photolithography, and dry etching is effected by the CF_4 gas so as to partially remove the n^+ layer, the insulating layer, and the photoconductive semiconductor layer, thereby forming a contact hole 316. In this case, it is not necessary to effect a selective etching of the n^+ layer, photoconductive semiconductor layer and the insulating layer.

Then, Aℓ /Cr is deposited to a thickness of 1.0 to 1.5 μm by vacuum deposition. Then, a resist pattern is formed by photolithographic method and a wet etching is effected so as to partially remove the Aℓ/Cr layer and the n^+ layer, thereby forming the upper electrode wirings 312, 313 and 314. The electrical connection to the lower electrode wiring 306 and the upper electrode wiring 312 of the wiring section 302 arranged in the form of a matrix is made through the contact holes 316. The gap of the photoelectric conversion section 303 and the channel of the transfer transistor serving as the switch section 305 are also formed in this step of the production process.

Then, a resist pattern is formed by a photolithographic method as shown in Fig. 32E, and dry etching is effected by using CF_4 gas, whereby the n^+ layer, photoconductive semiconductor layer and the insulating layer are partially removed. In consequence, the elements which have been connected through the photoconductive semiconductor layer are isolated, so that electrical connections are formed only in the portions which require such connection.

Then, a passivation film (not shown) is formed from silicon nitride or an organic resin, thus completing the production of the line sensor.

It is preferred that the photoelectric conversion sections and the switch sections of the line sensor arranged in the form of array have uniform distribution of the electric characteristics. In this embodiment, the characteristic distribution can be uniformalized merely through the control of thickness distribution in the steps for forming layers. In this embodiment, the gap portions and the channel portions which are critical in the photoelectric conversion section and the switch section are protected by the insulating layer formed in the course of formation of the film, so that the gap portions and the channel portions are never affected by subsequent steps. In addition, since the layers are formed successively, it is possible to protect the interface between the semiconductor layer and the insulating layer against contamination by impurities. Furthermore, since the photoconductive semiconductor layer is already covered by the insulating film, the material of the final passivation film can have a large variety.

A description will be made hereinunder as to a still further embodiment of the invention. This embodiment is similar to the embodiment shown in Figs. 32A to 32E, except that a light-shielding layer 317 is formed on the lower part of the photoelectric conversions section 303 of the embodiment shown in Fig. 32. In operation, the light impinges from the substrate side, and the light reflected from an original contact-

ing the surface of the photoelectric conversion section is directly read by the photoelectric conversion section. Fig. 33 is a fragmentary sectional view of an example of this embodiment. As will be seen from this Figure, the light impinges upon the original from the same side as the substrate.

The process for producing the photoelectric conversion device of this embodiment is materially the same as that shown in Figs. 32A to 32E. In this embodiment, however, the light-shielding layer 317 is formed simultaneously with the formation of the lower electrode wirings 306, 307 and 308 from the same material as these wirings.

In the embodiments shown in Figs. 25 and 31, as well as the embodiment shown in Fig. 33, adopts such a construction that the light incident to the photoelectric conversions section impinges from the upper side, so that the photoelectric conversion characteristics are significantly attected by the state of the upper inter-surface of the photoconductive semiconductor layer in the gap portion of the photoelectric conversion section. In these embodiments, however, the inter-surface of the gap portion is formed by continuous film forming steps and is protected by the insulating layer in the subsequent steps. Therefore, the inter-surface is less likely to be affected and contaminated by impurities, as compared with the case where the gap portion is formed by, for example, etching process. In consequence, these embodiments offers an advantage that the operation characteristics of the photoelectric conversion device are remarkably stabilized. In addition, since the photoconductive semiconductor layer is already covered by the insulating layer, the material of the passivation film which is to be formed finally can have a wide selection.

As will be understood from the foregoing description, this embodiment of the present invention offers a production process in which an insulating layer and a photoconductive semiconductor layer on the insulating layer are formed in at least the photoelectric conversion section, charge accumulating section and the switch section, and then the insulating layer and the photoconductive semiconductor layer are patterned. With this process, it is possible to prevent the insulating layer from being degraded in the subsequent steps such as etching, and to suppress the occurrence of troubles such as short-circuiting in the charge accumulating section and in the areas where the upper and lower wirings intersect each other, fluctuation in the capacitance, and degradation of insulation in the area where the electrode wirings intersect each other, whereby the reliability is improved remarkably.

In addition, since the major constituents of the photoelectric conversion device can be formed simultaneously, the processes for the formation of layers and formation of elements can be simplified. Furthermore, since the constituents have the same basic construction, the device can be produced with a high scale of integration so that the size of the device can be reduced advantageously. For these reasons, it is possible to reduce the production costs and to increase the degree of freedom in the design of the photoelectric conversion device.

When a plurality of layers are to be formed in this embodiment, the insulating layer and the photoconductive semiconductor layer formed on this insulating layer are patterned and used as an inter-layer insulator. Thus, the inter-layer insulator can be formed in the same step as that for forming the photoelectric conversion section and the charge accumulating section.

Claims

1. An image reading device having, on a substrate (116, 301) a photoelectric conversion section (101, 303) comprising a thin film semiconductor layer (113, 310) to photoelectrically convert an image information, a charge accumulation section (102, 304) comprising a capacitor to accumulate an electric signal photoelectrically produced by said photoelectric conversion section, a switch section (103, 305) comprising a thin film transistor having a thin film semiconductor layer (113, 310) to output the charge accumulated in said charge accumulation section (102, 304), the photoelectric conversion section (101, 303) comprising at least a pair of electrodes (108, 105, 312', 313) spaced from each other and formed on the thin film semiconductor layer (113, 310), said capacitor of the charge accumulation section (102, 304) comprising a thin film semiconductor layer (113, 310) and an insulating layer (112, 309) both of which are sandwiched between at least a pair of electrodes (104, 105, 307, 313), said thin film transistor of the switching section (103, 305) comprising a gate electrode an insulating layer sandwiched between the gate electrode and the thin film semiconductor layer (111, 308), and source and drain electrodes (109, 110, 315) in electrical contact with the thin film semiconductor layer and spaced from each other said thin film semiconductor layers (113, 310) being made of the same semiconductor material.

2. An image reading device as claimed in claim 1, in which the photoelectric conversion section (101) is composed of a plurality of photoelectric conversion elements and the charge accumulating section (102) comprises a common electrode (104) which is used for accumulating electric signals produced by the plurality of photo electric conversion elements.

ing the surface of the photoelectric conversion section is directly read by the photoelectric conversion section. Fig. 33 is a fragmentary sectional view of an example of this embodiment. As will be seen from this Figure, the light impinges upon the original from the same side as the substrate.

The process for producing the photoelectric conversion device of this embodiment is materially the same as that shown in Figs. 32A to 32E. In this embodiment, however, the light-shielding layer 317 is formed simultaneously with the formation of the lower electrode wirings 306, 307 and 308 from the same material as these wirings.

In the embodiments shown in Figs. 25 and 31, as well as the embodiment shown in Fig. 33, adopts such a construction that the light incident to the photoelectric conversions section impinges from the upper side, so that the photoelectric conversion characteristics are significantly attected by the state of the upper inter-surface of the photoconductive semiconductor layer in the gap portion of the photoelectric conversion section. In these embodiments, however, the inter-surface of the gap portion is formed by continuous film forming steps and is protected by the insulating layer in the subsequent steps. Therefore, the inter-surface is less likely to be affected and contaminated by impuritles, as compared with the case where the gap portion is formed by, for example, etching process. In consequence, these embodiments offers an advantage that the operation characteristics of the photoelectric conversion device are remarkably stabilized. In addition, since the photoconductive semiconductor layer is already covered by the insulating layer, the material of the passivation film which is to be formed finally can have a wide selection.

As will be understood from the foregoing description, this embodiment of the present invention offers a production process in which an insulating layer and a photoconductive semiconductor layer on the insulating layer are formed in at least the photoelectric conversion section, charge accumulating section and the switch section, and then the insulating layer and the photoconductive semiconductor layer are patterned. With this process, it is possible to prevent the insulating layer from being degraded in the subsequent steps such as etching, and to suppress the occurrence of troubles such as short-circuiting in the charge accumulating section and in the areas where the upper and lower wirings intersect each other, fluctuation in the capacitance, and degradation of insulation in the area where the electrode wirings intersect each other, whereby the reliability is improved remarkably.

In addition, since the major constituents of the photoelectric conversion device can be formed simultaneously, the processes for the formation of layers and formation of elements can be simplified. Furthermore, since the constituents have the same basic construction, the device can be produced with a high scale of integration so that the size of the device can be reduced advantageously. For these reasons, it is possible to reduce the production costs and to increase the degree of freedom in the design of the photoelectric conversion device.

When a plurality of layers are to be formed in this embodiment, the insulating layer and the photoconductive semiconductor layer formed on this insulating layer are patterned and used as an inter-layer insulator. Thus, the inter-layer insulator can be formed in the same step as that for forming the photoelectric conversion section and the charge accumulating section.

Claims

1. An image reading device having, on a substrate (116, 301) a photoelectric conversion section (101, 303) comprising a thin film semiconductor layer (113, 310) to photoelectrically convert an image information, a charge accumulation section (102, 304) comprising a capacitor to accumulate an electric signal photoelectrically produced by said photoelectric conversion section, a switch section (103, 305) comprising a thin film transistor having a thin film semiconductor layer (113, 310) to output the charge accumulated in said charge accumulation section (102, 304), the photoelectric conversion section (101, 303) comprising at least a pair of electrodes (108, 105, 312', 313) spaced from each other and formed on the thin film semiconductor layer (113, 310), said capacitor of the charge accumulation section (102, 304) comprising a thin film semiconductor layer (113, 310) and an insulating layer (112, 309) both of which are sandwiched between at least a pair of electrodes (104, 105, 307, 313), said thin film transistor of the switching section (103, 305) comprising a gate electrode an insulating layer sandwiched between the gate electrode and the thin film semiconductor layer (111, 308), and source and drain electrodes (109, 110, 315) in electrical contact with the thin film semiconductor layer and spaced from each other said thin film semiconductor layers (113, 310) being made of the same semiconductor material.

2. An image reading device as claimed in claim 1, in which the photoelectric conversion section (101) is composed of a plurality of photoelectric conversion elements and the charge accumulating section (102) comprises a common electrode (104) which is used for accumulating electric signals produced by the plurality of photo electric conversion elements.

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3. An image reading device as claimed in claim 1 or 2, in which one of the pair of electrodes (203) in the photoelectric conversion section and one of the pair of electrodes in the charge accumulation section constitute a common electrode.

4. An image reading device as claimed in any one of claims 1 to 3 in which the thickness of the semiconductor layer (113, 310) of the switch section (103, 305) is less than the thickness of the semiconductor layer (113, 310) of the photoelectric conversion section (101, 303).

5. A device or method as claimed in claim 4 in which the semiconductor layer (113, 310) is made of hydrogenated amorphous silicon.

6. An image reading device as claimed in any one of claims 1 to 5, further comprising a matrix wiring section (302) to connect the photoelectric conversion device with an external circuit, wherein, the semiconductor layer (113, 310) which is common to the photoelectric conversion section (101, 303), the charge accumulating section (102, 304) and the switch section (103, 305) is sandwiched between the upper (312, 313, 314) and lower (306, 307, 308) wiring sections.

7. An image reading device as claimed in any previous claim, wherein an n^+ type semiconductor layer (315) is provided at least between the semiconductor layer (113, 310) and a said electrode (312, 313, 314).

8. A method of producing a image reading device as claimed in claim 1, which includes forming a photoelectric conversion section (101, 303), a charge accumulating section comprising a capacitor (102, 304) to accumulate an output of said photoelectric conversion section, and a switch section comprising a thin film transistor, to output the charge accumulated in the charge accumulation section (103, 305) each section being provided with an insulating layer (112, 309) and a thin film semiconductor layer (113, 310) wherein the semiconductor layer (310) of the three said sections is formed from the same material during a single manufacturing step.

9. A method of producing an image reading device as claimed in claim 8, which includes the step of consecutively laminating the insulating layer (112,309) and the semiconductor layer (113, 310) and then effecting a patterning of the insulating layer (112, 309) and the semiconductor layer (113, 310).

10. A method of producing an image reading device as claimed in claim 8, comprising the further step of etching the semiconductor layer (113, 310) to form the switch section (103, 305) and the photoelectric conversion section (101, 303).

11. A method as claimed in any one of claims 8 to 10, further comprising the step of providing a matrix wiring section (302) connecting the photoelectric conversion device with an external circuit, wherein, between lower and upper electrodes of the matrix wiring section, the insulating layer and the semiconductor layer common to ones of the photoelectric conversion section, the charge accumulating section and the thin film transistor section are provided.

12. A method as claimed in any one of claims 8 to 11, in which n^+ type semiconductor layer (315) is provided at least between the semiconductor layer (113, 310) and a said electrode (312, 313, 314).

Patentansprüche

1. Bildleseeinrichtung, die auf einem Substrat (116, 301) einen photoelektrischer Wandlerabschnitt (101, 303) mit einer Dünnfilm- Halbleiterschicht (113, 310) zur photoelektrischen Wandlung einer Bildinformation, einen Ladeakkumulationsabschnitt (102, 304) mit einem Kondensator zur Akkumulation eines photoelektrisch von dem photoelektrischen Wandlerabschnitt erzeugten elektrischen Signals, und einen Schalterabschnitt (103, 305) mit einem Dünnfilmtransistor mit einer Dünnfilm-Halbleiterschicht (113, 310) zur Ausgabe der in dem Ladeakkumulationsabschnitt (102, 304) akkumulierten Ladung trägt, wobei der photoelektrische Wandlerabschnitt (101, 303) wenigstens ein Elektrodenpaar (108, 105, 312', 313) enthält, deren Eletroden durch die Dünnfilm-Halbleiterschicht (113, 310) voneinander beabstandet und auf dieser gebildet sind, wobei der Kondensator des Ladeakkumulationsabschnitts (102, 304) eine Dünnfilm- Halbleiterschicht (113, 310) und eine Isolationsschicht (112, 309) umfaßt, dessen beide Schichten zwischen wenigstens einem Elektrodenpaar (104, 105, 307, 313) geschichtet angeordnet sind, wobei der Dünnfilmtransistor des Schalterabschnitts (103, 305) eine Gate- Elektrode (111, 308), eine zwischen der Gate- Elektrode und der Dünnfilm-Halbleiterschicht eine geschichtet angeordnete Isolationsschicht und elektrisch mit der Halbleiterschicht verbundene, voneinander beabstandete Source- und Drain- Elektroden (109, 110, 315) aufweist, wobei die Dünnfilm- Halbleiterschichten (113, 310) aus dem gleichen Halbleitermaterial bestehen.

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2. Bildleseeinrichtung nach Anspruch 1, deren photoelektrischer Wandlerabschnitt (101) aus einer Vielzahl photoelektrischer Wandlerelemente und dem Ladeakkumulationsabschnitt (102) zusammengesetzt ist, der eine gemeinsame Elektrode (104) enthält, die zur Akkumulation der durch die Vielzahl photoelektrischer Wandlerelemente erzeugten elektrischen Ladungen dient.

3. Bildleseeinrichtung nach Anspruch 1 oder 2, in der eine Elektrode des Elektrodenpaares (203) in dem photoelektrischen Wandlerabschnitt und eine Elektrode des Elektrodenpaares in dem Ladeakkumulationsabschnitt eine gemeinsame Elektrode bilden.

4. Bildleseeinrichtung nach einem der Ansprüche 1 bis 3, in der die Stärke der Halbleiterschicht (113, 310) des Schalterabschnitts (103, 305) geringer ist als die Stärke der Halbleiterschicht (113, 310) des photoelektrischen Wandlerabschnitts (101, 303).

5. Vorrichtung oder Verfahren nach Anspruch 4, wobei die Halbleiterschicht (113, 310) aus einem hydrierten nichtkristallinem Silizium besteht.

6. Bildleseeinrichtung nach einem der Ansprüche 1 bis 5, die des weiteren einen Matrixleitungsführungsabschnitt (302) zur Verbindung des photoelektrischen Wandlers mit einer Außenschaltung enthält, wobei die dem photoelektrischen Wandlerabschnitt (101, 303), dem Ladeakkumulationsabschnitt (102, 304) und dem Schalterabschnitt (103, 305) gemeinsame Halbleiterschicht (113, 310) zwischen dem oberen (312, 313, 314) und dem unteren (306, 307, 308) Leitungsführungsabschnitt geschichtet angeordnet ist.

7. Bildleseeinrichtung nach einem der vorstehenden Ansprüche, bei der eine Halbleiterschicht (315) des n^+- Typs wenigstens zwischen der Halbleiterschicht (113, 310) und der Elektrode (312, 313, 314) vorgesehen ist.

8. Verfahren zur Herstellung einer Bildleseeinrichtung nach Anspruch 1, mit folgenden Verfahrensschritten: Bilden eines photoelektrischen Wandlerabschnitts (101, 303), eines Ladeakkumulationsabschnitts (102, 304) mit einem Kondensator zum Akkumulieren eines Ausgangssignals des photoelektrischen Wandlerabschnitts und eines Schalterabschnitts (103, 305) mit einem Dünnfilmtransistor, der die in dem Ladeakkumulationsabschnitt akkumulierte Ladung ausgibt, wobei jeder Abschnitt mit einer Isolationsschicht (112, 309) und einer Dünnfilm- Halbleiterschicht (113, 310) vorgesehen ist, wobei die Halbleiterschicht (310) mit den drei Abschnitten aus gleichem Material in einem einzigen Herstellschritt hergestellt wird.

9. Verfahren zur Herstellung einer Bildleseeinrichtung nach Anspruch 8, das den Verfahrensschritt aufeinanderfolgender Laminierung der Isolationsschicht (112, 309) und der Halbleiterschicht (113, 310), und dann den Verfahrensschritt einer Musterbildung für die Isolationsschicht (112, 309) und die Halbleiterschicht (113, 310) umfaßt.

10. Verfahren zur Herstellung einer Bildleseeinrichtung nach Anspruch 8, mit dem weiteren Verfahrensschritt: Ätzen der Halbleiterschicht (113, 310) zur Bildung des Schalterabschnitts (103, 305) und des photoelektrischen Wandlerabschnitts (101, 303).

11. Verfahren nach einem der Ansprüche 8 bis 10, mit dem weiteren Verfahrensschritt: Vorsehen eines die photoelektrische Wandlereinrichtung mit einer externen Schaltung verbindenden Matrixleitungsführungsabschnitts (302), worin die untere und obere Elektrode des Matrixleitungsführungsabschnitts, die Isolationsschicht und die Halbleiterschicht, die dem photoelektrischen Wandlerabschnitt gemeinsam sind, der Ladeakkumulationsabschnitt und der Dünnfilm- Transistorabschnitt vorgesehen sind.

12. Verfahren nach einem der Ansprüche 8 bis 11, das eine Halbleiterschicht (315) des n^+- Typs wenigstens zwischen der Halbleiterschicht (113, 310) und der Elektrode (312, 313, 314) vorsieht.

Revendications

1. Un dispositif de lecture d'image comportant, sur un substrat (116, 301), une section de conversion photoélectrique (101, 303) comportant une couche mince de semiconducteur (113, 310) pour convertir de façon photoélectrique une information d'image, une section d'accumulation de charge (102, 304) comprenant un condensateur pour accumuler un signal électrique qui est produit de façon photoélectrique par la section de conversion photoélectrique, une section d'élément de commutation (103, 305) comprenant un transistor à couche mince ayant une couche mince de semiconducteur (113, 310) pour émettre une charge accumulée dans la section d'accumulation de charge (102, 304), la section de conversion photoélectrique (101, 303) comprenant au moins une paire d'électrodes (108, 105, 312', 313) mutuellement espacées et formées sur la couche mince de semiconducteur (113, 310), le

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condensateur de la section d'accumulation de charge (102, 304) comprenant une couche mince de semiconducteur (113, 310) et une couche isolante (112, 309), toutes deux étant intercalées entre au moins une paire d'électrodes (104, 105, 307, 313), le transistor à couche mince de la section d'élément de commutation (103, 305) comprenant une électrode de grille (111, 308), une couche isolante intercalée entre l'électrode de grille et la couche mince de semiconducteur, et des électrodes de source et de drain (109, 110, 315) en contact électrique avec la couche mince de semiconducteur, et mutuellement espacées, les couches minces de semiconducteur (113, 310) étant formées par le même matériau semiconducteur.

2. Un dispositif de lecture d'image selon la revendication 1, dans lequel la section de conversion photoélectrique (101) est constituée par un ensemble d'éléments de conversion photoélectrique, et la section d'accumulation de charge (102) comprend une électrode commune (104) qui est utilisée pour accumuler des signaux électriques qui sont produits par l'ensemble d'éléments de conversion photoélectrique.

3. Un dispositif de lecture d'image selon la revendication 1 ou 2, dans lequel l'une des électrodes de la paire d'électrodes (203) dans la section de conversion photoélectrique et l'une des électrodes de la paire d'électrodes dans la section d'accumulation de charge constituent une électrode commune.

4. Un dispositif de lecture d'image selon l'une quelconque des revendications 1 à 3, dans lequel l'épaisseur de la couche de semiconducteur (113, 310) de la section d'élément de commutation (103, 305) est inférieure à l'épaisseur de la couche de semiconducteur (113, 310) de la section de conversion photoélectrique (101, 303).

5. Un dispositif ou procédé selon la revendication 4, dans lequel la couche de semiconducteur (113, 310) est formée par du silicium amorphe hydrogéné.

6. Un dispositif de lecture d'image selon l'une quelconque des revendications 1 à 5, comprenant en outre une section d'interconnexion matricielle (302) pour connecter le dispositif de conversion photoélectrique à un circuit externe, dans lequel la couche de semiconducteur (113, 310) qui est commune à la section de conversion photoélectrique (101, 303), à la section d'accumulation de charge (102, 304) et à la section d'élément de commutation (103, 305), est intercalée entre les sections d'interconnexion supérieure (312, 313, 314) et inférieure (306, 307, 308).

7. Un dispositif de lecture d'image selon l'une quelconque des revendications précédentes, dans lequel une couche de semiconducteur de type n^+ (315) est formée au moins entre la couche de semiconducteur (113, 310) et une électrode précitée (312, 313, 314).

8. Un procédé de fabrication d'un dispositif de lecture d'image selon la revendication 1, comprenant la formation d'une section de conversion photoélectrique (101, 303), d'une section d'accumulation de charge comprenant un condensateur (102, 304) pour accumuler un signal de sortie de la section de conversion photoélectrique, et d'une section d'élément de commutation (103, 305) comprenant un transistor à couche mince, pour fournir en sortie la charge qui est accumulée dans la section d'accumulation de charge, chaque section étant munie d'une couche isolante (112, 309) et d'une couche mince de semiconducteur (113, 310), dans lequel la couche de semiconducteur (310) des trois sections précitées est formée avec la même matière au cours d'une seule étape de fabrication.

9. Un procédé de fabrication d'un dispositif de lecture d'image selon la revendication 8, comprenant l'étape qui consiste à déposer consécutivement la couche isolante (112, 309) et la couche de semiconducteur (113, 310) et à définir ensuite un motif dans la couche isolante (112, 309) et dans la couche de semiconducteur (113, 310).

10. Un procédé de fabrication d'un dispositif de lecture d'image selon la revendication 8, comprenant l'étape supplémentaire qui consiste à graver la couche de semiconducteur (113, 310) pour former la section d'élément de commutation (103, 305) et la section de conversion photoélectrique (101, 303).

11. Un procédé selon l'une quelconque des revendications 8 à 10, comprenant en outre l'étape qui consiste à former une section d'interconnexion matricielle (302) connectant le dispositif de conversion photoélectrique à un circuit externe, dans lequel la couche isolante et la couche de semiconducteur communes à certaines sections parmi la section de conversion photoélectrique, la section d'accumulation de charge et la section de transistor à couche mince, sont formées entre des électrodes supérieure et inférieure de la section d'interconnexion matricielle.

12. Un procédé selon l'une quelconque des revendi-

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cations 8 à 11, dans lequel une couche de semiconducteur de type n^+ (315) est formée au moins entre la couche de semiconducteur (113, 310) et une électrode précitée (312, 313, 314).