WHAT IS CLAIMED IS:

1. An electronic device comprising a semiconductor memory, wherein the semiconductor memory comprises:

row lines each extending in a first direction;

column lines each extending in a second direction crossing the first direction;

memory cells positioned at intersections of the row lines and the column lines, and including first sidewalls facing in the first direction and second sidewalls facing in the second direction;

first protective layers respectively formed on the second sidewalls of the memory cells; and

second protective layers respectively formed on the first sidewalls of the memory cells,

wherein the second protective layers are in contact with at least a portion of a corresponding one of the column lines, and

wherein the first protective layers are spaced apart from the second protective layers.

2. The electronic device of claim 1, wherein the first protective layers and the second protective layers are disposed adjacent to each other at corners of each of the memory cells without wrapping around the corners.

3. The electronic device of claim 1, wherein the first

protective layers are separated from each other in the first direction and the second direction, and

wherein the second protective layers are separated from each other in the first direction and the second direction.

4. The electronic device of claim 1, wherein each of the first protective layers and each of the second protective layers are formed to have substantially the same thickness, and the first protective layers and the second protective layers include silicon nitride.

5. The electronic device of claim 1, wherein each of the first protective layers and each of the second protective layers have substantially the same thickness.

6. The electronic device of claim 1, wherein the corresponding one of the column lines includes first portions overlapping the memory cells and second portions each overlapping a space between an adjacent pair of the memory cells, and

wherein the second protective layers cover the first portions and expose the second portions.

7. The electronic device of claim 1, further comprising:

an insulating layer buried in a space between an adjacent pair of the memory cells.

8. The electronic device of claim 7, wherein the insulating layer includes a low-K material having thermal conductivity lower than that of the first and second protective layers.

9. The electronic device of claim 7, wherein the insulating layer includes an SiOC material.

10. The electronic device of claim 9, wherein the insulating layer further includes hydrogen or nitrogen.

11. The electronic device of claim 1, wherein each of the memory cells includes two or more layers stacked in a vertical direction, and

wherein the two or more layers include a variable resistance layer.

12. A method of manufacturing an electronic device, the method comprising:

forming a plurality of stack structures including a plurality of row lines and a plurality of variable resistance layers, respectively, each of the plurality of stack structures extending in

a first direction;

forming a first protective layer on sidewalls of the plurality of stack structures;

forming a first insulating layer between the plurality of stack structures;

forming column lines crossing the row lines on the first insulating layer;

forming a plurality of stack patterns including memory cells positioned at intersections of the row lines and the column lines by etching the first insulating layer, the first protective layer, and the plurality of stack structures;

forming a second protective layer on sidewalls of the plurality of stack patterns;

forming a second insulating layer between the plurality of stack patterns;

forming a mask pattern overlapping one or more of the column lines and one or more of the row lines on the second insulating layer; and

etching the second protective layer using the mask pattern as an etch barrier to separate the second protective layer from the first protective layer.

13. The method of claim 12, wherein etching the second protective layer comprises etching a portion of the second

protective layer that does not overlap a corresponding one of the row lines.

14. The method of claim 12, wherein the mask pattern includes a plurality of open regions, and the plurality of open regions are arranged in a matrix form.

15. The method of claim 12, further comprising:

filling a third insulating layer between the plurality of stack patterns, after etching the second protective layer.

16. The method of claim 12, wherein the first protective layer and the second protective layer are formed of silicon nitride.

17. The method of claim 12, wherein the first insulating layer and the second insulating layer include a SiOC material, and

wherein the first insulating layer and the second insulating layer further include hydrogen or nitrogen.

18. The method of claim 12, wherein the first insulating layer and the second insulating layer include a material having thermal conductivity lower than that of the first and second protective layers.

19. A method of manufacturing an electronic device, the method comprising:

forming a plurality of stack structures including a plurality of first lines and a plurality of variable resistance layers, each of the plurality of stack structures extending in a first direction;

forming a first protective layer on sidewalls of the plurality of stack structures;

forming a first insulating layer between the plurality of stack structures;

forming second lines extending in a second direction crossing the first direction on the first insulating layer;

forming a plurality of stack patterns including memory cells positioned at intersections of the first lines and the second lines by etching the first insulating layer, the first protective layer, and the plurality of stack structures;

forming a second protective layer on sidewalls of the plurality of stack patterns;

forming a second insulating layer between the plurality of stack patterns;

forming a mask pattern overlapping a corresponding one of the first lines on the second insulating layer; and

etching the second protective layer using the mask pattern and the second lines as an etch barrier so that the second protective layer does not protrude beyond the first protective layer

in the second direction.

20. The method of claim 19, wherein etching the second protective layer comprises etching a portion of the second protective layer that does not overlap a corresponding one of the first lines.

21. The method of claim 19, wherein in etching the second protective layer, a thickness of the first protective layer formed on the sidewalls of the plurality of stack patterns is reduced.

22. The method of claim 19, wherein the first insulating layer and the second insulating layer include a material having thermal conductivity lower than that of the first protective layer and the second protective layer.